Design and Simulation of Source-engineered TFETs for Low-power Applications

Chaliti Fikadu Wakwaya

A Thesis Submitted to

The Department of Electronics and Communication Engineering

School of Electrical Engineering and Computing

Presented in Partial Fulfillment of the Requirement for the Degree Master's in Electronics and Communication Engineering (Communication Engineering)

Office of Graduate Studies

Adama Science and Technology University

June, 2024

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Advisor: Dr. Davinder Singh Rathee

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DECLARATION

I hereby declare that this Master Thesis entitled **"Design and simulation of source-engineered TFETs for low-power applications"** is my original work. That is, it has not been submitted for the award of any academic degree, diploma, or certificate in any other university. All sources of materials that are used for this thesis have been duly acknowledged through citation.

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We, the advisors of this thesis, hereby certify that we have read the revised version of the thesis entitled **"Design and simulation of source-engineered TFETs for low-power applications"** prepared under our guidance by Chaliti Fikadu submitted in partial fulfillment of the requirements for the degree of Master of Science in Electronics and Communication Engineering. Therefore, we recommend the submission of the revised version of the thesis to the department following the applicable procedures.

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Co-Advisor name	Signature	Date

APPROVAL PAGE OF M.SC. THESIS

We, the advisors of the thesis entitled **"Design and simulation of source-engineered TFETs for low-power applications"** and developed by Chaliti Fikadu, hereby certify that the recommendation and suggestions made by the board of examiners are appropriately incorporated into the final version of the thesis.

Major Advisor	Signature	Date
Co-advisor	Signature	Date

We, the undersigned, members of the Board of Examiners of the thesis by Chaliti Fikadu have read and evaluated the thesis entitled **"Design and simulation of source-engineered TFETs for low-power applications"** and examined the candidate during open defense. This is, therefore, to certify that the thesis is accepted for partial fulfillment of the requirement of the degree of Master of Science in Electronics and Communication Engineering.

Chairperson	Signature	Date
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External Examiner	Signature	Date

Finally, approval and acceptance of the thesis are contingent upon the submission of its final copy to the Office of Postgraduate Studies (OPGS) through the Department Graduate Council (DGC) and School Graduate Committee (SGC).

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ABBREVIATIONS

BGN	Band Gap Narrowing
BGTFET	Broken-Gate Tunnel Field-Effect Transistor
BJT	Bipolar Junction Transistor
BQB	Bit Quantization Bandwidth
BTBT	Band to Band Tunneling
CMOS	Complementary metal–oxide–semiconductor
CONMOB	Concentration Mobility
DGTFETs	Double Gate tunnel field effect transistor
DIBL	Drain-Induced Barrier Lowering
DLTFETs	Doping-less Tunnel Field-Effect Transistor
FET	Field-Effect Transistor
FLDMOB,	Field-Effect Mobility
FoMs	Figure of Merits
GBP	Gain-Bandwidth Product
Ge-BGTFET	Germanium-Source BG-TFET
Ge-S N+ Pocket BG-TFET	Germanium- source N+ pocket Broken-Gate Tunnel-field Effect Transistor
GAS	Germanium-around-source
MOSFET	Metal-oxide-semiconductor field effect transistor
SRH	Shockley-Read-Hall
SCEs	Short-Channel Effects
SOI TFET	Silicon-On-Insulator Tunnel Field-Effect Transistor
SGTFET	Single Gate tunnel field effect transistor
SS	Subthreshold slope
TCAD	Technology Computer-Aided Design
TFET TM-DG TFET	Triple-material double gate Tunnel Field Effect Transistor
TFET	Tunnel field effect transistor
VT-FETs	Vertical Tunneling Field-Effect Transistor

ABSTRACT

The thesis addresses the imperative need for low-power electronic devices, which is crucial in today's technology landscape where energy efficiency and portability are paramount. Traditional MOSFETs, while prevalent, face significant challenges when scaled down for low power applications, particularly due to high leakage currents and suboptimal performance at lower voltages. Tunnel Field-Effect Transistors (TFETs) emerge as a viable solution due to their ability to achieve steeper subthreshold slopes (SS), enabling lower operational voltages and reduced power consumption. However, TFETs inherently suffer from limitations such as low ON-current (I_{ON}) and ambipolarity, which hinder their widespread adoption. To mitigate these issues, this research explores advanced source engineering techniques to enhance TFET performance. The study begins with the double gate TFETs (DGTFET), followed by an investigation into broken gate TFETs (BG-TFET), focusing on optimizing parameters such as drain doping concentration, gate-drain underlap, and drain split configurations. A significant advancement is achieved by introducing a Germanium source in the broken gate TFET (Ge-BG-TFET), aimed at improving the I_{ON}. Subsequently, a novel N+ Pocket broken gate TFET (N+ Pocket BG-TFET) is proposed to address the limitations observed in the Ge-BG-TFET. The culmination of this research is the development of a novel Germanium-Source N^+ Pocket broken gate TFET (Ge-S N^+ Pocket BG-TFET) structure. This innovative design, combining the advantages of both Germanium source and N^+ Pocket engineering, exhibits remarkable performance metrics. Simulations conducted using SILVACO ATLAS TCAD software demonstrate an I_{ON} of 1.82×10^{-4}A/µm, I_{OFF} of 4.33×10^{-18} A/µm, an I_{ON}/I_{OFF} ratio of 4.21×10^{13}, a SS of 29.19 mV/decade, and a V_{th} of 0.37534 V. These results indicate a substantial improvement in device efficiency, effectively overcoming the low I_{ON} challenge of traditional TFETs while maintaining low power operation.

Furthermore, the applicability of the proposed TFET structure is validated through its application in biosensing, showcasing its potential in scenarios. This comprehensive approach underscores the importance of source engineering, particularly material and shape engineering, in developing high-performance, low-power TFETs. The thesis provides a robust framework for the design and simulation of next-generation TFETs, contributing significantly to the advancement of low-power electronics

Keywords: BTBT, TFET, Ge-S N+ Pocket BG-TFET, N+ pocket, germanium source

CHAPTER ONE

1 INTRODUCTION

1.1 Background of the Study

A revolution in the semiconductor industry began in 1947 when Walter Brattain, John Bardeen, and William Shockley developed the bipolar junction transistor (BJT) at Bell Laboratory. Since then, electronics specialists have connected hundreds or thousands of discrete electronic parts, such as transistors, diodes, rectifiers, and capacitors, to build ever-more complex electronic circuits and systems. However, Kahng and Atalla's 1960 practical implementation and characterization of a distinct kind of low-power, high-speed transistor known as the metal-oxide-semiconductor field effect transistor (MOSFET) served as the main impetus for the advancement in integrated circuit technology (M. M. Atalla, 1960).

Since then, MOSFETs which have the potential to have higher drive currents, shorter charge carrier transit times, faster operating speeds, superior switching characteristics, and greater viability for size miniaturization through scaling have displaced BJTs as the more widely used active component in high-performance IC technology.

The integration of p-type and n-type MOSFETs, known as complementary metal-oxide semiconductor (CMOS) technology, has revolutionized the construction of modern microprocessors, microcontrollers, static RAM, and other digital logic circuits. This technology, widely used in ICs, has driven the development of sophisticated multifunctional microprocessor systems. The continuous pursuit of high-performance computing and communication applications has prompted the miniaturization of MOSFETs through scaling, allowing billions of CMOS circuits to be integrated into a single wafer.

Ideally, scaling MOSFET transistors involves shrinking their size without compromising functionality. To achieve optimal performance, this process requires adjustments to other device characteristics, including oxide thickness, channel thickness, applied bias voltages, threshold voltages, and doping concentration, alongside reducing the gate length.

The growing need for better transistor density that is, more transistors per unit area in contemporary complicated multifunctional integrated circuit technology is what is driving the scaling of CMOS technology. However, because of the increased active power and subthreshold

power losses that result from this scaling, power management in ICs is severely challenged (Gudjónsson et al., 2006).

Billions of transistors have been integrated into ICs thanks to the reduction of MOSFET gate lengths brought about by technology scaling. However, this has also resulted in a notable rise in static or subthreshold power (P_{sub}) loss because of the degradation of the threshold voltage (V_{th}), which has reduced the increase in off-state current (I_{OFF}). Moreover, the subthreshold slope (SS) of 60 mV/decade at room temperature in typical bulk MOSFETs poses a challenge to enhancing the switching performance of contemporary high-speed CMOS circuits. Thus, when gate lengths drop, it is crucial to consider non-conventional MOSFET architectures that can reduce threshold voltage degradation. These MOS devices also need to be modified structurally or materially to attain high I_{ON}/I_{OFF} ratios and SS values below 60 mV/decade. The tunnel field effect transistor (TFET) is one such non-conventional MOS device, inherently capable of achieving an SS of less than 60 mV/decade (Nagavarapu et al., 2008).

However, TFETs have notable disadvantages, including low I_{ON} and ambipolar behavior in current conduction, since carrier transfer from the source to the channel is based on BTBT (M. Kumar & Jit, 2015). Figure 1.1 shows the difference between n-type MOSFET and TFET. A MOSFET consists of a source, drain, gate, and body (or substrate). The gate is separated from the substrate by a thin layer of insulating oxide. Similar to MOSFETs, TFETs have a source, drain, gate, and body. However, they often use a different material for the source and drain to create a steep band-to-band tunneling junction.

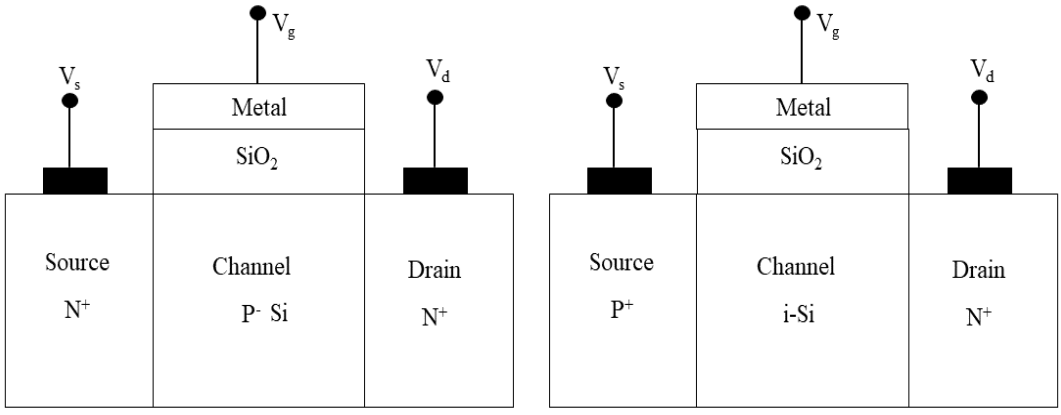


Figure 1.1 n-channel a) MOSFET b) TFET

The current mechanism for both devices is shown in Figure 1.2. MOSFET relies on the formation of a conductive channel by electric field (voltage-controlled), operates in linear and saturation regions, and is based on thermionic emission of carriers whereas TFET relies on quantum tunneling of carriers through an energy barrier, has the potential for lower SS (steeper on-off transitions), and is aimed at low-power applications

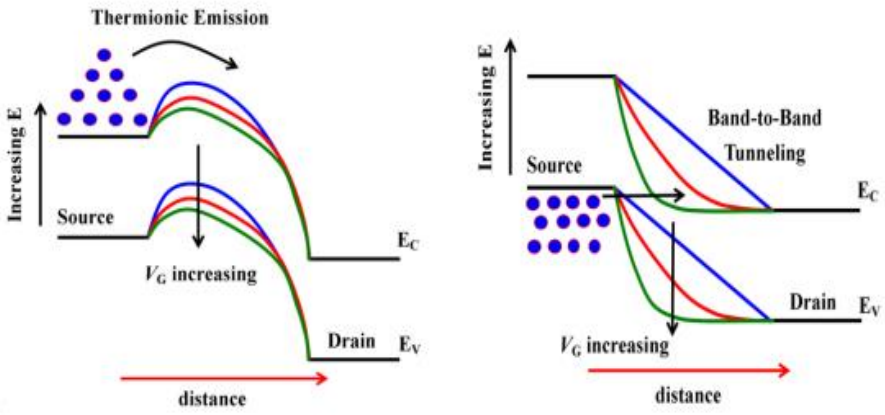


Figure 1.2 The current mechanism of (a) MOS device and (b) Tunnel FET (S.H. Kim, 2012)

1.2 Statement of the Problem

It has been suggested that TFET technology, which provides a higher I_{ON}/I_{OFF} ratio, lower leakage current, and a steeper SS, be used to alleviate the poor performance of traditional MOSFETs, which have a large SS, short channel effects (SCEs), and leakage current. TFETs do, however, have an Achilles' heel, particularly concerning low I_{ON}. A variety of methods, including work function engineering, hetero-structure, dielectric pocket, and gate dielectric engineering, can be applied to enhance the I_{ON} in TFETs. However, they greatly increase I_{ON} at the expense of other performance indicators for the device. In this study, it has been suggested that source engineering be used to enhance TFET performance in low-power applications. By doing this, the devices would be able to work with both present-day and emerging technologies, which would make them appropriate for use in low-power circuit designs.

1.3 Objectives

1.3.1 General Objective

The general objective of this thesis is to design and simulate source-engineered TFETs for low-power applications.

1.4.2 Specific Objectives

- To create and assess a source-engineered TFET, focusing on key performance metrics like SS, Electric field ratio, and current-voltage behavior.
- To increase the BTBT area and hence tunneling current to achieve better drive current and I_{ON}/I_{OFF} ratio.
- To perform the analytical model for the surface potential of the Source-engineered TFET structure.

1.4 Scope of the Thesis

The scope of this thesis encompasses the design, and simulation of advanced TFETs for low-power applications. It includes an extensive investigation of various TFET configurations, focusing on structures such as DGTFET, BG-TFET, Ge-BG-TFET and specifically the Ge-S N+ Pocket BG-TFET. The research delves into key parameters like doping concentrations and structural modifications to enhance device performance. Furthermore, the thesis explores the application of these optimized TFETs in biosensing, demonstrating their potential in low-power electronic devices. The scope also involves using advanced simulation tools, specifically SILVACO ATLAS TCAD, to provide a comprehensive framework for evaluating and advancing semiconductor technologies.

1.5 Significance of the Thesis

The importance of this thesis is found in its innovative contributions to semiconductor technology, especially in advancing the development of low-power TFETs. By introducing and optimizing novel TFET structures, such as the Ge-S N+ Pocket BG-TFET, the research achieves remarkable improvements in key performance metrics critical for reducing power consumption and enhancing device efficiency. The methodologies and innovations presented in this thesis not only address current challenges in semiconductor device engineering but also pave the way for future advancements, contributing to the evolution of energy-efficient electronics and fostering further research and development in this crucial area.

1.6 Contribution of the Thesis

This thesis significantly advances the field of low-power semiconductor devices through the design and simulation of various TFET structures. Initially, it explores and optimizes BG-TFET configurations, focusing on key parameters such as drain doping concentration, gate-drain underlap, and drain split. These investigations pave the way for the development of more efficient and effective TFET designs.

One of the major contributions is the creation of a novel Ge-S N+ Pocket BG-TFET. Germanium is chosen due to its superior electrical properties compared to traditional silicon, which leads to enhanced performance characteristics in the TFET. The research further innovates by incorporating source-pocket doping techniques into the Ge-BG-TFET, resulting in a new hybrid structure known as the Ge-S N+ Pocket BG-TFET. This hybrid approach combines the benefits of both the Germanium-source and the N^+ pocket designs, achieving superior performance metrics.

The thesis reports significant improvements in critical performance parameters for this novel TFET structure. These include a higher I_{ON}, low I_{OFF}, an exceptional I_{ON}/I_{OFF} ratio, a steep SS, and an optimal V_{th}. These metrics are crucial for low-power applications, demonstrating the effectiveness of the proposed design in reducing power consumption.

Overall, the thesis lays a strong foundation for future research and development, offering valuable insights and innovations that can drive the evolution of energy-efficient semiconductor technologies.

1.7 Limitation of the Thesis

The proposed designs involve precise doping concentrations and profiles, which may be challenging to achieve consistently in practical fabrication processes, potentially leading to variations in device performance. Additionally, the novel TFET structures, particularly those involving complex doping profiles and broken-gate configurations, may pose significant fabrication challenges. The feasibility of manufacturing these devices at scale is not addressed. And also, the research primarily relies on simulations using SILVACO ATLAS TCAD, which, while powerful, may not capture all real-world complexities and variations present in physical devices. Experimental validation is necessary to confirm the simulated outcomes.

1.8 Organization of the Thesis

This thesis is organized into five chapters, each with a distinct purpose. Chapter 1 presents essential background information on transistor technologies, detailing the research problem, objectives, significance, study scope, and motivation behind the research. Chapter 2 offers an extensive literature review, more crucial than the other chapters, providing a thorough overview of the topic and discussing relevant prior research. Chapter 3 describes the materials and methods used in the study, outlining the approach and techniques to tackle the research problem. Chapter 4 showcases the research results and discusses them in detail. Finally, Chapter 5 summarizes the findings and suggests directions for future research in the field.

CHAPTER TWO

2 LITERATURE REVIEW

2.1 Overview

This section provides a broad overview of the research conducted to enhance the characteristics of TFETs and introduces diverse configurations developed to enhance the I_{ON} and diminish the I_{OFF} in these devices. This is a critical component of the thesis as it provides context and background information relevant to the research topic. Through an extensive analysis of previously conducted studies by other researchers, this chapter aims to identify gaps, limitations, and areas that require further investigation. The literature review serves as the foundation for the current research, demonstrating its significance in the context of the existing body of knowledge, and providing valuable insights to guide subsequent chapters.

2.2 Tunnel Field Effect Transistor (TFET)

2.2.1 Structure of TFET

The primary differences between a TFET and a MOSFET are in their basic structures, except the doping applied to the source and drain terminals, which is what sets TFETs apart. A typical TFET device structure is a P-I-N junction, where a gate terminal regulates the intrinsic region's electrostatic potential, and reverse bias is used to operate the device (Turkana & Kureshi, 2016).

MOSFETs get their source of carrier injection from thermal injection, whereas TFETs get theirs from the BTBT. The source, gate, and drain are the three parts of a TFET's fundamental construction. The drain current is influenced by the majority carrier as it travels from the source to the drain (which is dependent on the number of majority carriers that reach the drain). The majority of carriers are supplied by the source terminal, transported out by the drain terminal, and regulated by the gate terminal. A channel forms between the p-type and n-type regions. The gate oxide acts as an insulator, preventing current leakage from the channel and allowing the gate to regulate the electrostatic pressure. One of the best options for ultra-low power applications is a tunnel FET because of its ability to generate a sub-thermal subthreshold slope. This is possible because the carrier injection method that TFETs use, inter-band tunneling, is temperature independent. Regretfully, defects in the semiconductor area and at the interface might cause serious problems with TFETs. The temperature-dependent trap-assisted tunneling (TAT) mechanism is causing BTBT while the device is supposed to be turned off. This leads to a generation current that weakens

the SS. This explains why so few experimental TFETs attain an SS of less than 60 mV/dec (Tamak & Mehra, 2017). TFET structure can be modified through processes to get better performance. Figure 2.1 shows conventional single Gate TFET (SGTFET) which uses a single-gate electrode to control tunneling in a channel. It operates by modulating the electric field, lowering the tunneling barrier. It offers a simpler fabrication process and lower manufacturing costs but may have less effective control over the channel and lower drive current.

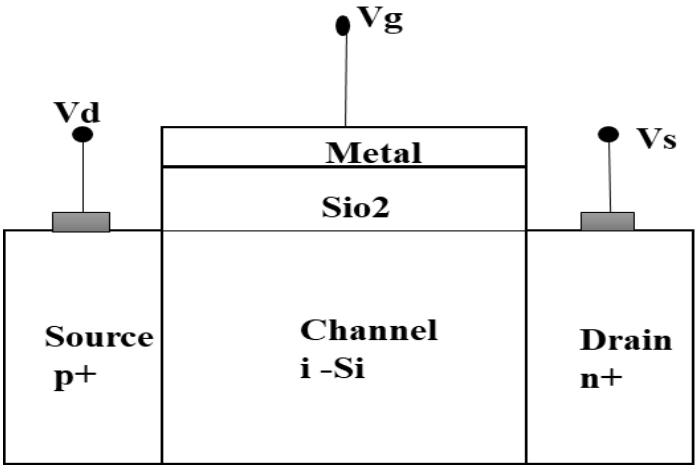


Figure 2.1 Single Gate TFET structure

Several structural modifications have been proposed to rectify the problems with the fundamental TFET structure.

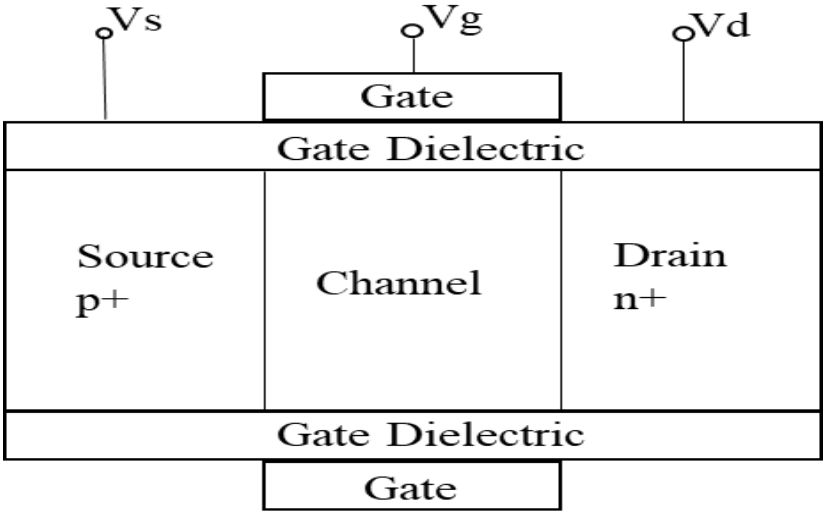


Figure 2.2 Double Gate TFET device structure

Implementation of DGTFET is one of the structural modifications. Figure 2.2 illustrates DGTFET a structure with two gate electrodes that sandwich the channel region, providing better electrostatic control. It offers enhanced control over the channel potential, lower leakage currents, higher drive currents, and reduced short-channel effects. Double Gates are preferred for high-performance applications requiring low leakage currents, high drive currents, and excellent subthreshold swings. They are more power-efficient due to better control over off-state current and reduced leakage.

Though each implementation of a TFET structure is unique, all of them have the same operational basis. A multitude of device factors, including work function, drain-source doping concentration, dielectric constant, body thickness, and gate-dielectric thickness, influence significant aspects of the electrical characteristics of different architectures (Guarango, 2022).

TFETs have high input impedance, power gain capabilities, and are unipolar devices with two device types and two-channel types. Applications include microprocessors, power devices, memories, and analog/RF systems.

2.2.2 TFET Transfer Characteristics

The characteristics of the current that passes through the device under various biased situations characterize the device's behavior. The most crucial aspects of a transistor are its transfer characteristics. This section will cover TFET behavior and how biasing impacts a TFET's drain current as seen by the TFETs' band diagrams in different biasing scenarios (Tamak & Mehra, 2017).

2.2.2.1 Off-State Characteristics

Charge carriers in the channel's conduction band tend to drift toward the drain in the off-state (VGS=0, VDS>0), which produces a current. There aren't as many electrons in the conduction band as there are in the p-type source, which restricts the number of electrons that can be injected into the channel and causes some IOFF. There is a free electron in the conduction band of an n-type MOSFET source. A tiny number of these electrons will be injected into the channel above the potential barrier at the source-channel junction because of the MOSFET concept of thermionic emission. As a result, a MOSFET's IOFF is higher than a TFET's.

2.2.2.2 On-State Characteristics

Charge carriers must be injected into the channel's conduction band when it is in the ON-state (VGS > 0, VDS > 0) in order for current to flow through the device. In TFETs, tiny free electrons

from the valence band of the source emerge as charge carriers in the conduction band of the p-type source area. The channel's energy bands move in relation to the source when the gate voltage rises. The valence band of the source and the channel lineup at a positive gate voltage (Karthik & Pandey, 2023). There were no accessible energy levels in the channel for electrons in the valence band of the source to tunnel into when it was off-stated. Electrons are now able to tunnel into the channel and pass over the potential barrier.

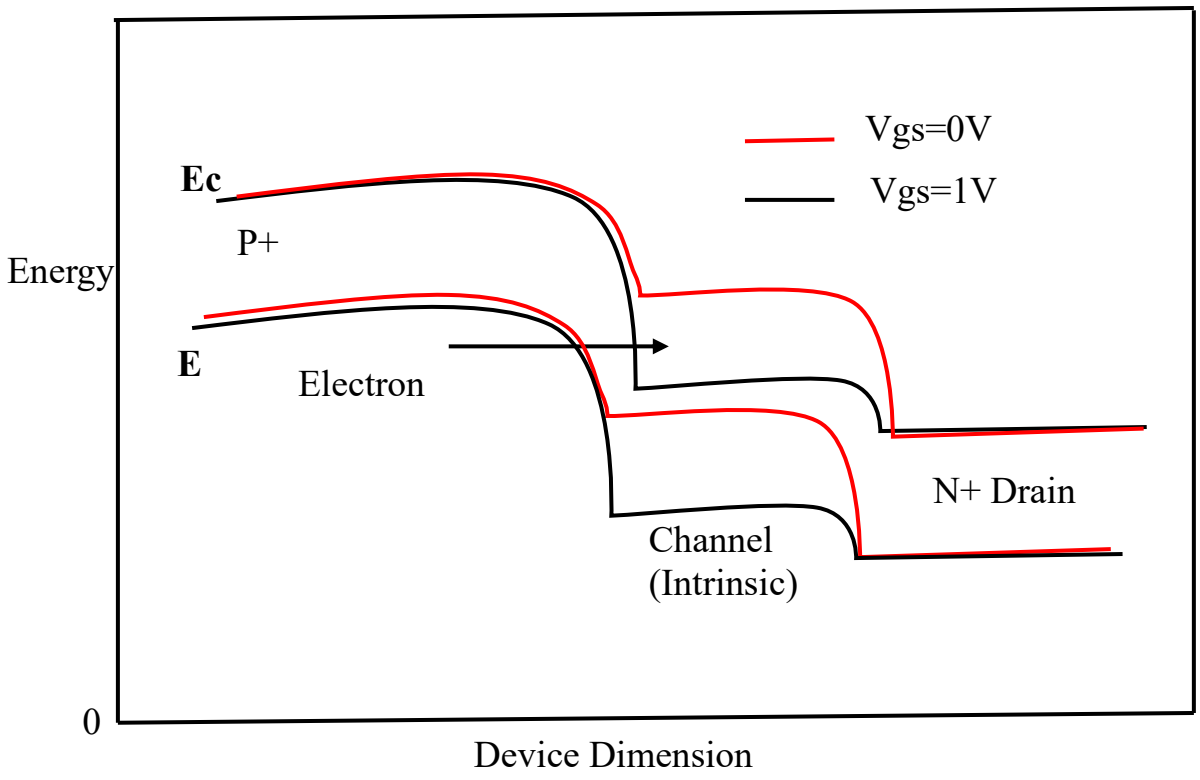


Figure 2.3 Energy band diagram of TFETs in off and on states

Figure 2.3 shows how the gate voltage in TFETs enables carriers to tunnel into the channel through the potential barrier via the BTBT operating principle. In the OFF-state of a TFET, a high channel barrier blocks current flow. However, due to the thermal distribution of carriers, there is a small, non-zero leakage current between the source and drain regions.

2.2.2.3 Ambipolar Characteristics

When the drain voltage (VDS > 0), a positive gate voltage was applied. Let's now talk about how a negative gate voltage (VGS < 0) affects a TFET. The channel's energy band rises toward the source area when the gate voltage is lowered below 0V. When VGS = 0, no electron can transfer

from the source valence band to the channel conduction band. The number of states in the channel valence band that can be tunneled to the drain's conduction band grows as the negative gate bias increases, as does the tunneling length at the channel-drain junction. These factors combined result in a significant rise in drain current, a phenomenon known as ambipolar conduction (Tiwari & Saha, 2022).

2.2.2.4 Band Diagram

Figure 2.4 depicts the energy levels of conduction and valence bands for both MOSFETs and N-TFETs. Because MOSFETs have low source barriers when they are in the on-state ($V_{GS} > V_{DS} > 0V$), they can emit thermionic carriers. On the other hand, the p-n junction barrier at the source restricts conduction in the off-state ($V_{GS} = 0V$, $V_{DS} > 1V$) by stopping thermionic carrier emission. By comparison, TFETs feature a low electric field and a broad source-to-channel tunnel junction barrier, which leads to a very low I_{OFF} because of the low transmission probability. Because of the width of the tunnel barrier, carriers can tunnel into the channel while it is in the on-state.

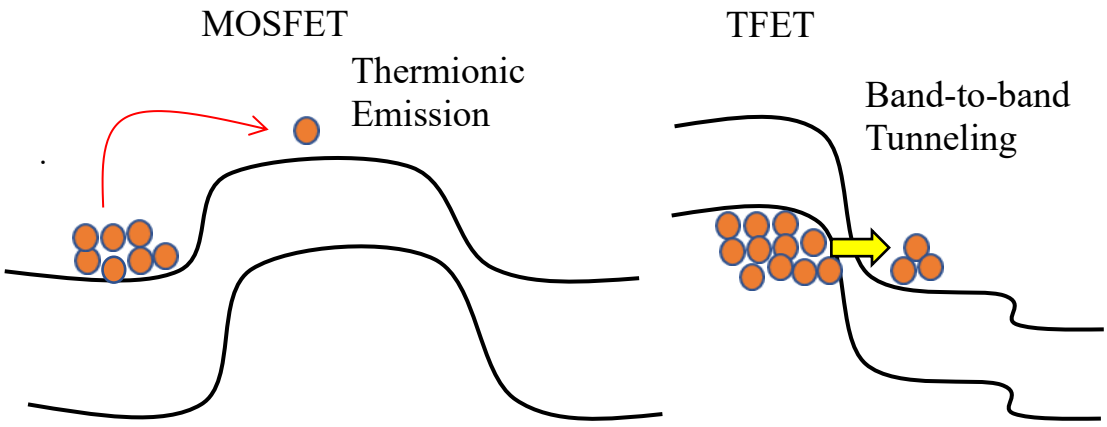


Figure 2.4 Working principle of the MOSFETs and TFETs

TFETs must fulfil several criteria to replace traditional MOSFETs and meet the demands of future VLSI technology (Karthik & Pandey, 2023). These criteria include achieving a high I_{ON}, an SS below 60mV/decade, a low I_{OFF} (leakage current), and a high I_{ON}/I_{OFF}. However, TFETs encounter challenges related to their I_{ON} and leakage current, which are less pronounced than in BTBT devices due to limitations stemming from a wide material band gap, thick dielectric gate, and low-k dielectric materials. The reduced I_{ON} leads to lower transconductance, thereby limiting the gain-bandwidth product (GBP) and maximum cut-off frequency. To address this, optimization

techniques have been explored, including reducing body and oxide thickness, engineering the metal work-function, heavily doping the source region, and employing high-k dielectrics in the gate oxide. In our research, we have focused on reducing the tunnelling barrier length at the source-channel junction through a device-level approach based on gate dielectric manipulation (Sravani et al., 2022), (Tajally & Karami, 2019). Essentially, those approach aims to enhance the strong electric field at the source/channel interface. Additionally, TFETs pose challenges related to their ambipolar conduction, increased miller capacitances (gate-to-source and gate-to-drain), and high leakage current.

2.2.3 Different Optimization Techniques of TFET

Several optimization techniques can be used to improve the performance of TFETs (Boucart & Ionescu, 2007; Tajally & Karami, 2019; N et al., 2020; Xie et al., 2021; Goyal et al., 2022; Karthik & Pandey, 2023).

- **Gate Work Function Engineering**

Is a method for precisely adjusting the work function of the gate material in semiconductor devices to maximize the performance of field-effect transistors (FETs). The energy needed to transfer an electron from a material's Fermi level to its vacuum level is known as the work function. The threshold voltage (Vth) in the context of FETs is greatly influenced by the gate work function, and this in turn influences the device's performance attributes, including switching speed, power consumption, and leakage current.

- **Hetero-Dielectric Engineering**

Incorporating a hetero-dielectric structure, like a high-k dielectric material in the gate stack, can enhance TFET performance. This strategy has been investigated to improve both the device characteristics and its analog/RF performance.

- **Structural Engineering**

Modifying the TFET structure can help optimize the device. These geometrical changes impact the tunneling barrier shape at the source/channel and drain/channel junctions, leading to improved electrical parameters.

- **Drain Engineering**

Suppressing the ambipolar current in TFETs can be achieved through methods such as drain doping engineering and the use of a field plate. Additionally, managing the tunneling width on the drain side is effective in reducing the ambipolar current.

- **Interface Trap Engineering**

Interface trap charges can affect the characteristics of a TFET. By meticulously engineering these interface traps with techniques like Gaussian or uniform doping profiles, the ambipolar current can be reduced, enhancing overall performance.

By combining these optimization techniques, such as gate work function engineering, hetero-dielectric engineering, and structural engineering, significant improvements in TFET performance, including increased on-current, reduced off-current, and suppressed ambipolar current, can be achieved

2.3 Related Works

The low-power dream team, TFETs, offer near-zero leakage and superior efficiency compared to MOSFETs. However, their Achilles' heel is limited current output, which could cripple their role in next-generation VLSI circuits. Addressing this bottleneck is key to unleashing their true potential (Verreck *et* al., 2016).

BTBT in TFETs bypasses the SS limitations of MOSFETs, offering significant promise for low-power applications. However, high bandgap silicon (Si) hinders I_{ON}. To address this, various strategies are employed, including high-κ spacers, double-gate structures, and low-band gap source materials. These designs enhance BTBT current while maintaining negligible I_{OFF} via an optimized tunnel region. High-κ spacers and gate dielectrics further improve electrostatic control within the device (N *et* al., 2020).

The dominant current control mechanism in conventional TFETs is a gate-modulated tunneling diode. However, the inherent limitations of silicon, notably its high bandgap and large carrier mass, restrict the achievable I_{ON}. DGTFETs present a compelling solution by potentially circumventing these constraints and offering an improved SS and reduced leakage current. To push the boundaries of I_{ON} even further, various strategies are under investigation, including heterojunction structures, work function engineering, dielectric pocket incorporation, and gate dielectric optimization. The long-term reliability, scalability, and manufacturing challenges of integrating this complex heterostructure into existing semiconductor processes have not been addressed (Chen *et* al., 2023). Several factors plague modern transistor performance, ambipolar conduction, excessive standby power, steep subthreshold slopes hindering speed, and insufficient on-state current limiting operational efficiency. Numerous device architecture strategies aim to reduce ambipolar behavior,

including low-k spacers, gate-drain underlaps, and lateral heterostructures with high bandgap drain regions. Tunnel FETs, however, face the additional challenge of a low on-state tunneling current due to inefficient BTBT. This inefficiency stems from factors like high carrier mass, wide tunneling width, indirect bandgap, high bandgap value, and weak lateral electric field. While introducing a hetero-dielectric BOX under the source region can combat ambipolar conduction, it increases fabrication complexity and reduces on-state current, necessitating alternative architecture approaches. Strategies like low drain doping, incorporating lower bandgap materials, and using PNPN TFET structures are explored, but each harbors limitation hindering significant on-state current improvements. The simulation results are based on idealized conditions, ignoring defects and interface traps, which can affect the actual performance of the device. Additionally, the proposed architecture may not be scalable to smaller dimensions due to the limitations of the 2-D ATLAS simulations used. Furthermore, the impact of the high-k dielectric BOX on the device's reliability and long-term stability is not fully explored (S. Kumar et al., 2022).

Ambipolar conduction in TFETs hinders their application in complementary circuits. (Shan *et* al., 2023) reported on PNPN TFETs with an N+ pocket for enhanced current, steeper subthreshold slope, and better reliability. Building on this, they introduced an "in-built N+ pocket electrically doped (ED)" structure, simplifying fabrication complexity by exploiting polarity bias to form the PNPN structure and eliminating the need for additional doping. The relentless pursuit of miniaturization and energy efficiency in electronic devices has propelled the quest for novel transistor technologies

Inspired by (S. Kumar et al., 2022), this work introduces a novel N+ Pocket architecture for TFETs, featuring a laterally divided high-low doping profile within a fixed width. This design reduces tunneling width, enhancing lateral electric field and suppressing horizontal field, leading to increased tunneling probability, rate, and on-state current at lower power consumption. However, extending the N+ Pocket beyond 4nm compromises SS and degrades the I_{ON}/I_{OFF} ratio.

Employing TCAD simulations, (Cecil et al., 2022) introduce a unique doping-less n-type TFET with a stacked source structure and raised source/drain regions. This design exhibits enhanced subthreshold characteristics, notably a three-order reduction in ambipolar current, due to the stacked Ge/Si source and raised regions. It also exhibits better DC characteristics than conventional DLTFETs (Doping-less TFETs), which position it as a viable option for energy-

efficient switches with steeper SS and fA-range leakage currents. Moreover, the charge-plasma based doping-less architecture provides immunity against random oscillations in dopants and simplifies production. To evaluate the effect of less tunneling on the device's overall performance, more research is necessary.

Employing GaSb/GaAs heterojunction and dual-material gates with distinct work functions, (Xie et al., 2021), introduce a unique dual-material gate heterogeneous dielectric vertical TFET (DMG-HD-VTFET) architecture. Simulations reveal its superiority over conventional Vertical TFETs (VTFETs) in both DC and RF characteristics, demonstrating an impressive subthreshold swing, high $I_{ON,}$ and improved transconductance at low drain voltage. Furthermore, the DMG-HD-VTFET boasts a remarkable maximum frequency potential of 459 GHz with a high gain bandwidth. However, while exceeding standard TFETs in several aspects, it exhibits a trade-off: increased I_{OFF}, reduced current ratio, and degraded SS and I_{ON} beyond a 6nm source pocket thickness

The paper in the literature (Shokry et al., 2020) provides a TFET structure design that extends a portion of the channel into the source and makes use of a germanium source. This structure's DC performance was assessed by measuring its SS, $I_{ON,}$ and I_{ON}/I_{OFF} ratio. Both the unit-gain cutoff frequency and transconductance (gm) were examined about the high-frequency performance. Their results demonstrate that by properly designing the proposed structure, both the I_{ON} and cut-off frequency can be improved simultaneously. However, they cannot determine the effect of increasing I_{ON} and decreasing SS in the I_{OFF}.

A two-dimensional model of a triple-material double gate Tunnel Field Effect Transistor (TM-DG TFET) is presented by (Vimala et al., 2019). In this model, silicon dioxide (SiO_2) and halogen dioxide (HfO_2) serve as dielectric materials, and germanium and silicon materials form a hetero-junction at the source channel junction. The study illustrates a number of electrical properties, including transconductance, drain current, electric field, and surface potential. Furthermore, the research examines the differences in drain current or I_{ON} in relation to the channel length (L), thickness (T_{si}), and effective oxide layer thickness (T_{ox}) of the device. According to the results, the suggested TM-DG TFET structure performs better than TFETs made of single or double materials. Additionally, the study shows how the tunneling barrier width is affected by the Germanium/Silicon hetero-junction. However, the authors do not explain how doping concentration impacts device performance.

(Das & Chakraborty, 2022) present a new n+ pocket-doped SOI TFET design incorporating a dielectric pocket at the channel/drain junction. This design enhances both lateral and vertical tunneling by leveraging the n+ pocket in the gate-source overlap region, resulting in increased I_{ON} and a sharper SS. Furthermore, the inclusion of the dielectric pocket depletes the drain region, reducing the tunneling width and mitigating ambipolar conduction. The study examines the effects of high temperature on various RF parameters, revealing enhancements in cutoff frequency and reductions in intrinsic delay. However, the impact of the n+ pocket on other device characteristics, such as electric field, surface potential, and I_{OFF}, remains unexplored.

(Kavi et al., 2024) developed a mathematical model to predict the electrical current in pocket hetero-dielectric double-gate tunnel FETs. This model aims to maintain efficient ON/OFF switching while improving overall performance. By applying Poisson's equations, the model calculates the current and electric field within the transistor, considering the length of the source pocket, a unique feature influencing current flow. Their findings show that transistors with a Source pocket perform significantly better than those without one. This enhanced transistor design with a source pocket is a promising option for applications that require fast switching, low operating voltage, and low power consumption. The model operates under idealized assumptions, ignoring flaws and interface traps that may have a big influence on the device's real performance. Furthermore, thermal variations, which can have an impact on both the tunneling rate and the overall performance of the device, are not taken into consideration by the model. Additionally, the model ignores factors that could be crucial for device optimization, such as the source pocket length and doping concentration's effects on device performance.

(Raad et al., 2018) introduces tunnel field-effect transistors (TFETs) designed to improve current flow, reduce turn-on voltage, and enhance high-frequency performance. This design features heavily doped source regions and metal electrodes on top, forming a sharper "tunnel junction" that facilitates easier current flow. Simulations indicate increased I_{ON}, lowered turn-on voltage, and better analog/RF performance compared to other methods. Additionally, the device's robustness against trap charges and manufacturing imperfections enhances its reliability and makes it well-suited for practical applications. This design also provides a lower threshold voltage and greater resistance to manufacturing defects. However, the impact of trap charges under the source electrode is also not fully explored, and the reliability of the device under high-density trap charges is not thoroughly investigated.

(Joshi et al., 2020) investigates the performance of a special type of transistor, the DGTFET with an extended source, for radio and high-frequency applications. The transistor employs two different gate materials, and the researchers studied how varying the length of the extended source impacts current flow, internal electrical fields, and signal amplification. As transistors become smaller in emerging technologies, this design seeks to enhance performance by optimizing electron tunneling within the device. They discovered that adjusting the source length can significantly improve several critical aspects of the transistor's operation. Overall, the primary limitation of this work is the reliance on 2-D simulations and the lack of experimental validation, which limits the ability to fully assess the practical viability and performance of the proposed ESDG-TFET device.

(Priyadarshani et al., 2022) presents a comparative and analytical analysis of the analog performance of a germanium pocket dual metal DGTFET with a hetero dielectric gate stack. The impact on the transconductance factor, intrinsic gain, cut-off frequency, drain current (ID), transconductance (gm), and other important Analog Figure of Merits (FoMs) is assessed in the study. The TFET architecture under study exhibits promising results when compared to typical MOSFETs, which exhibit poorer performance due to impurity dispersion in short-channel devices resulting to heat generation and losses. Simulation outcomes suggest that incorporating a germanium pocket at the source side enhances the I_{ON}/I_{OFF} ratio by approximately fourfold, while utilizing dual metal with a hetero dielectric gate stack proves to be an effective approach for controlling the device's transfer characteristics. Moreover, the study does not account for potential variability in material properties and the impact of manufacturing imperfections, which could affect device performance and reliability.

The paper in literature (Khan et al., 2020) aims to examine the performance impact of a symmetric underlapped double-gate heterojunction TFET with a metallic drain. As FETs scale down and the demand for compact, high-performance technologies rises, new devices are needed to meet these requirements. The study explores short-channel effects and parasitic effects in MOS-FETs, with a particular focus on temperature dependence in SOI technologies. Additionally, it investigates how the device behaves under varying ambipolar currents to the underlap length. The on-state drain current fluctuated more significantly when the metallic drain's work function was changed. A Germanium Source-Double Gate Tunnel-field Effect Transistor with a metallic drain (GS-DGTFET-MD) is proposed and simulated in the study. The work on double gate tunnel field effect

transistor (DG-TFET) design has limitations, including the use of a metallic drain, the introduction of an underlap region, reliance on simulations for performance improvements, and the need for optimization of parameters. While the proposed solution effectively suppresses ambipolar current, further research is needed to address these drawbacks and validate its effectiveness in practical applications.

(Dutta & Sarkar, 2019) report on a redesigned TFET structure with a 21 nm gate length in this study. The suggested framework has undergone optimization and analytical modeling. The broken gate transistor (BG-TFET) has I_{ON} that are equivalent to modern architectures of comparable size, excellent SS, and extremely low ambipolar current. The 2-D Poisson's equation is solved to simulate the device's internal electric field and surface potential. The analysis's findings are verified against simulations based on the Synopsys Centaurus TCAD nonlocal tunneling model. However, they did not analyze the effect of other performance parameters on this broken-gate TFET.

In comparison to previous research, (Chowdhury et al., 2022) present a unique analytical model for a BG-TFET-based biosensor and it shows respectable performance in sensitivity studies conducted using the conventional current variability method. The model demonstrates that a rectangular fill profile performs better than a slant profile, taking into consideration the steric hindrance effect to account for real-world conditions. The limitation of this model is that it has primarily been validated through sensitivity analyses and simulations, which may not fully capture the complexities and variabilities encountered in real-world applications. Additionally, while the model incorporates the steric hindrance effect and accounts for a wide range of biomolecules, it may require further refinement and experimental validation to ensure its accuracy and reliability under diverse operating conditions and with different bio-materials.

Table 2.1 An overview of related works

Authors	Year	Title	Techniques	Gap
Shokry et al.,	2020	Design of Extended Channel Ge-source TFET for Low Power Applications	Channel-engineering	But they cannot determine the effect of increasing I_{ON} and decreasing SS in the I_{OFF}.
Xie et al.,	2021	Study of a gate-engineered vertical TFET with GaSb/GaAs0.5Sb0.5 heterojunction	Gate-engineering, Heterostructures	The proposed system has increased I_{OFF}, decreased I_{ON}/I_{OFF} ratio
Das & Chakraborty,	2022	Effect of dielectric pocket for controlling ambipolar conduction in TFET and analysis of noise and temperature sensitivity	Dielectric pocket, gate-source overlap	Can't examine the effect of n+ pocket in the gate-source overlap region on the other device characteristics
Dutta & Sarkar	2019	Analytical Modeling and Simulation-Based Optimization of Broken Gate TFET Structure for Low Power Applications.	Structural Modification	They did not analyze the effect of other performance parameters on this broken-gate TFET.
Chowdhury et al.,	2022	Analytical modeling of dielectrically modulated broken-gate tunnel FET biosensor considering partial hybridization effect	Structural modification and analytical modeling	It may require further refinement and experimental validation to ensure its accuracy and reliability under diverse operating

				conditions and with different bio-materials.
S. Kumar et al.,	2022	Controlling Ambipolar Current and Enhancement of on-State	Source-pocket	Extending the source pocket beyond 4nm compromises subthreshold slope and degrades the I_{ON}/I_{OFF} ratio.
Raad et al.,	2018	Source engineered tunnel FET for enhanced device electrostatics with trap charges reliability.	Source engineering	However, the impact of trap charges under the source electrode is also not fully explored, and the reliability of the device under high-density trap charges is not thoroughly investigated.
Vimala et al.,	2019	Performance enhancement of triple material double gate TFET with heterojunction and heterodielectric	Material engineering	Do not explain how doping concentration impacts device performance.

CHAPTER THREE

3 METHODOLOGY AND STRUCTURE DESCRIPTION

This section will provide comprehensive insights into the software utilized, outlining its functionalities and relevance to the research. Additionally, it will elucidate the step-by-step design methodology employed, elucidating how the project was conceptualized and executed. Furthermore, a thorough description of the structural aspects will be provided, outlining the framework and architecture employed in the research process.

3.1 Design Methodology

3.1.1 Simulation Procedures and Devices

This procedure provides a simplified overview of the typical steps involved in running simulations with Atlas in the form of a flowchart. Each step may involve detailed sub-steps depending on the specific requirements and complexity of the simulation being conducted.

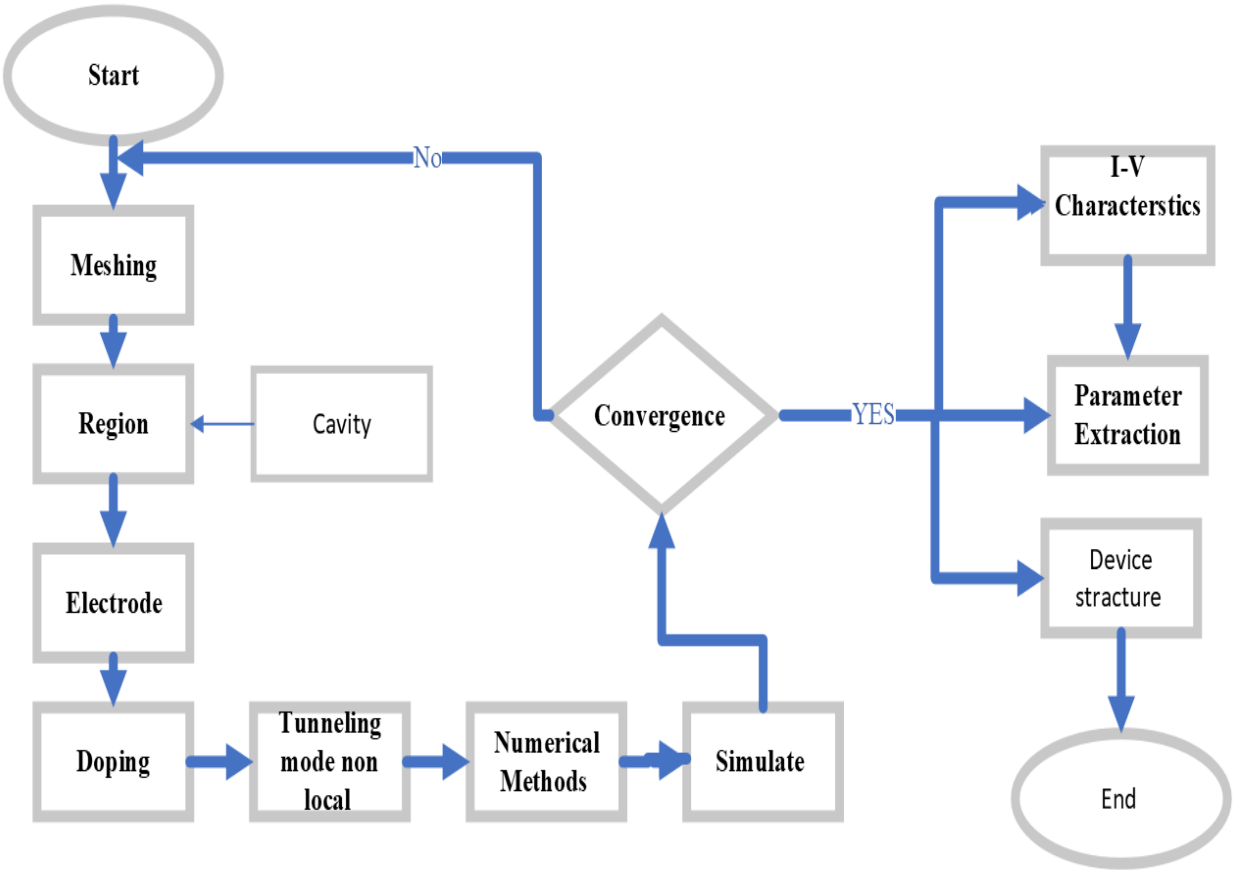


Figure 3.1 Atlas resolution algorithm of Ge-S N+ Pocket BG-TFET

3.1.1.1 Structure Specification

This step includes defining the mesh, regions, materials, electrodes, and doping profiles within the input file. The MESH, REGION, ELECTRODE, and DOPING statements are used for this purpose (Clara, 2019).

I. Meshing

Meshing in Atlas is the process of dividing a simulated device structure into mesh cells, which serve as the computational domain for solving physical equations describing semiconductor device behavior, covering the entire device structure. Here we are simulating the 2-D device structure in Cartesian, by using the x-axis mesh X.mesh for the left to right dimension of the device and the y-axis mesh Y.mesh for the top to bottom dimension of the device. In our structure, we are using an x-axis dimension of 0-0.047µm and a y-axis dimension of 0-0.022µm.

x.mesh location = <value> spacing = <value>

y.mesh location = <value> spacing = <value>

II. Regions

In Atlas, "regions" refer to distinct sections or areas within the simulated semiconductor device structure that have specific material properties, doping profiles, or physical characteristics. These regions are defined in the input file and play a fundamental role in specifying the device geometry and composition for simulation purposes.

region <region number> <location parameter> name=<material>

III. Electrode

In Atlas, "electrodes" represent conductive terminals or contact regions within a semiconductor device where external electrical connections are made to apply voltages, inject or extract carriers, or measure device characteristics. Electrodes play a crucial role in defining the device geometry, specifying boundary conditions, and controlling the flow of current through the device.

electrode <location parameter> name=<electrode name>

The location parameter can be determined as x.min, x.max, y.min, and y.max with the value in µm.

IV. Doping

In Atlas, "doping" refers to the intentional introduction of impurity atoms into semiconductor materials to modify their electrical properties. Doping plays a crucial role in semiconductor device fabrication by controlling the concentration and distribution of charge carriers (electrons or holes) within the material. Doping regions within the device structure specify the doping type and location. Doping affects the electrical properties of semiconductor materials by introducing impurity energy levels, modifying the Fermi level, and creating excess charge carriers.

doping <distribution type><dopant type><position parameter>

The above statement is used to define doping in the atlas. Different doping profiles are there in the simulation software in our work we use uniform doping profiles.

3.1.1.2 Material and Models Specification

While the MODELS statement defines material models, the MATERIAL statement specifies material qualities. CONTACT and INTERFACE statements are used to specify contact and interface properties. Contacts in Atlas represent the regions where external electrical connections are made to the semiconductor device. We used two types of contacts namely source and drain contacts to inject and extract carriers from the semiconductor channel and Gate contacts to control the flow of carriers in the channel by applying a voltage to modulate the channel conductivity.

contact name=<contact name> common=<contact name>

In the design and modeling of semiconductor devices, theoretical models like AUGER, FLDMOB, BQB, NON-LOCAL BTBT, SRH, and CONMOB are used. FLDMOB and CONMOB are two concentration-dependent mobility models, with FLDMOB focusing on low electric field mobility and CONMOB taking into consideration the impacts of high electric fields.

Charge carriers flow over the bandgap of a semiconductor material according to a band-to-band tunneling model known as BQB. NON-LOCAL BTBT is an additional tunneling model that considers the impact of non-local scattering on the tunneling procedure. The SRH recombination model predicts the rate of charge carrier recombination in a material.

The impact ionization model AUGER describes the process of electrons accumulating energy and generating extra electron-hole pairs in a material, which leads to enhanced current flow. For a variety of applications, these models are used to accurately simulate and improve the performance of semiconductor devices, such as TFETs. The models used in the simulation are summarized in Table 3.1.

Table 3.1 Summary of models used in the simulation

Model	Syntax	Comments
Shockley-Read-Hall	SRH	Initiated generation-recombination; used to maintain a stable minority carrier lifetime.
Band Gap Narrowing	BGN	Significant in the area with high doping (signify band-gap narrowing model).
Lombardi (CVT) model	CVT	To take into account the effects of high-field mobility
Band to band tunneling	BBT.NONLOCAL	Enables the modeling of both forward and reverse tunneling
Concentration mobility	CONMOB	Employed to relate low-field mobility to impurity concentration.
Auger transition	AUGER	Crucial at high current densities.
Field dependent mobility	FLDMOB	Used in field mobility.

3.1.1.3 Selection of Numerical Method

The METHOD statement is used to select the numerical method for the simulation process. The method applied in our work is the Newton trap, expressed as

Method Newton trap

3.1.1.4 Solution Specification

In this step, the solution procedure is specified. This includes loading and storing solution files, establishing the log file, and solving for bias points. For this, the statements LOG, SOLVE, LOAD, and SAVE are utilized. All terminal characteristics produced by a solution statement can be saved to a file using the LOG statement. The bias points that must be used to generate an output are specified in the SOLVE statement. To store all node point data into an output file, use the store statement. (.LOG) can be plotted with tonyplot; to open a log file and SAVE OUTF =, use the statement <LOG OUTF=>.Following the solution statement, the terminal attributes are saved using STR.

3.1.1.5 Results Analysis

The EXTRACT statement is used for data extraction and plotting, allowing users to extract device parameters and construct specific routines for analysis. TONYPLOT is used for plotting simulation results. Overall simulation procedures are expressed in Table 3.2. By following these steps in the ATLAS simulation flowchart, users can effectively set up and run simulations for semiconductor device analysis and optimization.

Table 3.2 Summary of simulation procedures

Group	**Statements**
Structure Details	Mesh, Region, Electrode, Doping
Specifications for Material Models	Material, , Interface Contact, Model
Selection of Numerical Methods	Method
Solution Details	Solve, Load, Log, Save
Analysis of the Result	Extract Tony plot

3.2 Description of Simulation Software

Silvaco Atlas TCAD: This is the main software for simulating the behavior of the device under study. It likely uses a computer model to mimic how the device would function in real life.

Origin: This software is for data analysis and visualization. It likely takes the simulation results (data) from Silvaco Atlas and allows the user to create graphs and charts to understand the data better.

3.2.1 Silvaco TCAD Atlas Tools

The TCAD software suite from Silvaco Technology includes the Atlas Tools for TCAD, which are specifically designed for simulating semiconductor devices. These tools help with the design and optimization of electronic components by offering a wide range of capabilities for modeling and evaluating semiconductor devices. Numerous features are included in the package, including interactive tools, automation tools, and solutions for typical simulation problems. With the help of these tools, users may build intricate device structures using up to 50 distinct materials, add new

materials to simulations, and alter material properties. Additionally, the program enables thorough material characterization, giving researchers and engineers the ability to accurately simulate the behavior of semiconductor devices (The ATLAS Collaboration, 2010).

3.2.1.1 Atlas Inputs and Outputs

Three main kinds of output files are produced by Atlas, a program included in the Silvaco TCAD software suite when semiconductor device simulations are running.

Structure file: This file contains the mesh, regions, and materials, as well as any 2D or 3D data of the device's structure. It can be used as a starting point for further simulations and visualization.

Log file: The log file contains all of the terminal voltages and currents from the device analysis. It is utilized with programs like TONYPLOT for data extraction and charting.

Solution file: This file contains the values of the device's solution variables at a specific bias point, including potential, carrier concentrations, and current densities. It can be used as a starting point for further simulations and visualization.

The Atlas input file outlines the simulation setup, detailing the device structure, materials, doping profiles, and simulation options. It begins with comments marked by the '#' character for documentation and explanations. The file specifies material properties, doping profiles, device structure, simulation options, contacts, and boundary conditions. To execute Atlas simulations, this input file is passed as a command-line argument following the "atlas" command. Atlas allows the incorporation of new materials, including conductors, semiconductors, and insulators, into the simulation environment (Clara, 2019).

3.3 Device Structure

This section introduces the structure of the DGTFET, BG-TFET, Ge-BG-TFET, N+ POCKET BG-TFET, and Ge-S N+ Pocket BG-TFET. The resulting device exhibits superior I_{ON} and more distinct subthreshold characteristics compared to silicon-based DGTFET and BG-TFET structures while maintaining current unidirectionality. The physical model utilized to realize the structures has been discussed. This study also focuses on optimizing device dimensions and doping concentrations to enhance SS and I_{ON}, while keeping other parameters intact and applied for biosensing application.

3.3.1 Double Gate Tunnel FET (DGTFET)

The structure of the DGTFET in this thesis consists of a p++ doped source region, an n- doped channel, and an n+ doped drain region, creating an asymmetric source and drain configuration. The device features two gates flanking the channel on either side in which high-k dielectric material HfO_2 is used as the gate oxide.

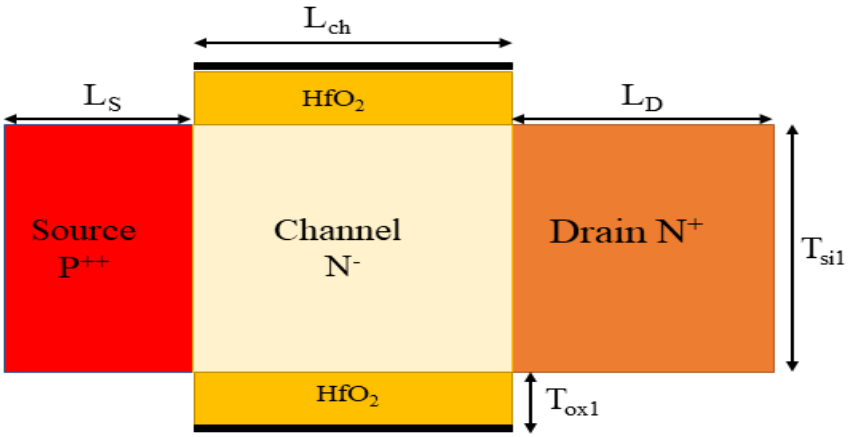


Figure 3.2 Double Gate TFET Structure

3.3.2 Broken Gate Tunnel FET (BG-TFET)

Figure 3.3 depicts the device structure for the BG-TFET in which we have taken the layout. There are two gates on top and two below, making up its four distinct gates. This design is based on a modified DGTFET structure in which a quick change in the channel thickness causes each top and bottom gate to split into two.

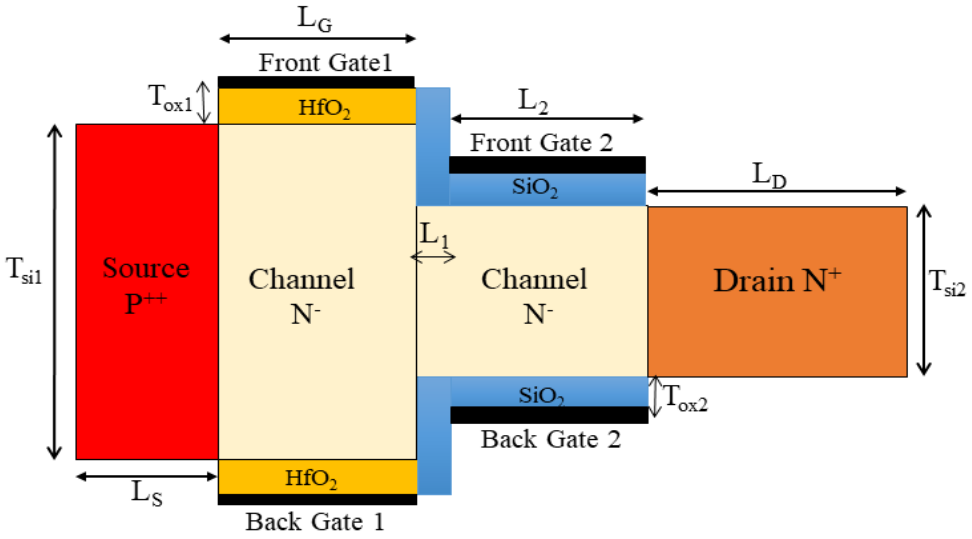
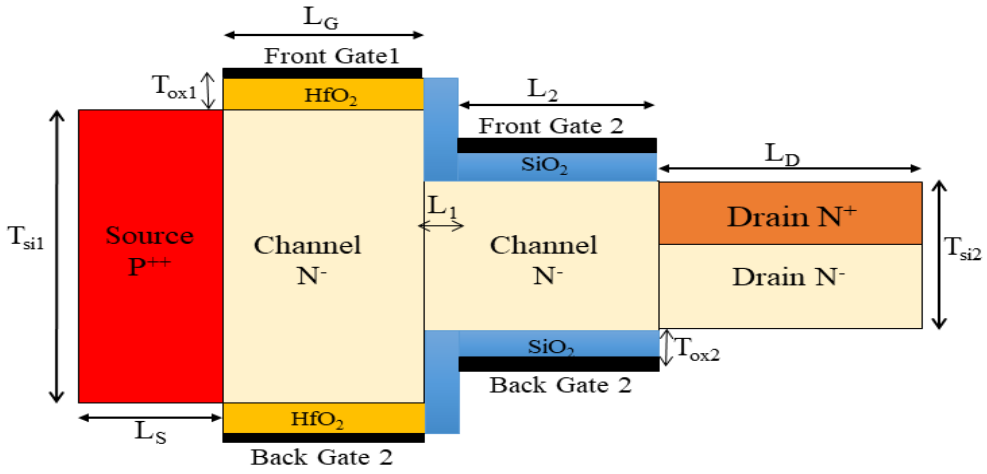


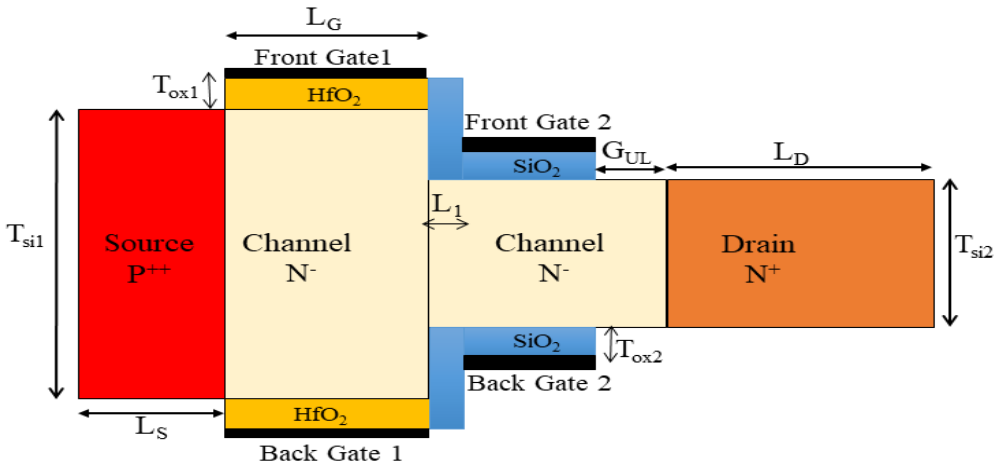
Figure 3.3 Structure of Broken Gate TFET

This work includes analyses and simulations in which the gates receive the same external gate voltage at the same time. Aluminum is used for gate metal connections in simulations. Near the source region, hafnium dioxide HfO_2 acts as the gate dielectric, whereas SiO_2 near the drain end. The channel is weakly doped p-type, and the drain is doped with an n^+-type dopant at a lower concentration than the source. P^+-type dopant is strongly doped in the source.

This BG-TFET structure further analyzed with drain-split where the drain of the BG-TFET is divided into two parts. The upper part of the drain with doping concentration of $5e^{18}$ /cm^3 and lower part $1e^{17}$/cm^3. Then gate-drain underlap with different underlap length is done as the structure is illustrated in Figure 3.4.



a) Device structure of BG-TFET with drain split



b) Device structure of BG-TFET with Gate under-lap

Figure 3.4 a) Device structure of BG-TFET with drain split b) Device structure of BG-TFET with Gate under-lap

3.3.3 Germanium Source Broken Gate Tunnel FET (Ge-BG-TFET)

Figure 3.5 illustrates the structure of germanium source broken gate TFET which is only the source material difference with the BG-TFET of Figure 3.3. The source material selection is done to the BG-TFET structure for improvement.

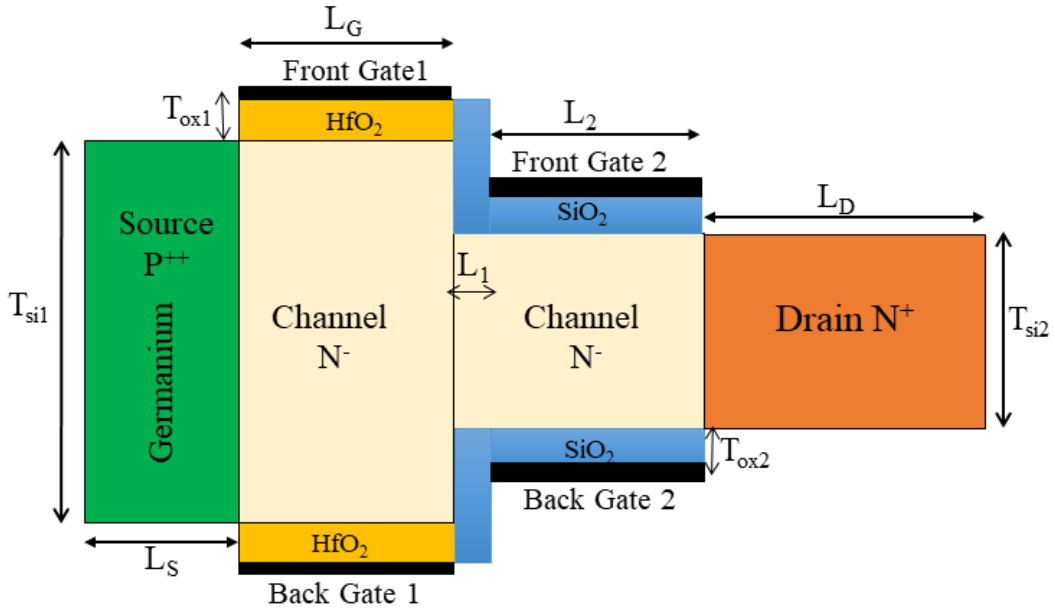


Figure 3.5 Structure of germanium-source broken gate TFET

3.3.4 N^+ Pocket Broken Gate Tunnel FET (N+ Pocket BG-TFET)

Figure 3.6 introduces a highly doped N+ Pocket near the source-channel junction. This can be achieved through specifically targeting the region adjacent to the p++ source.

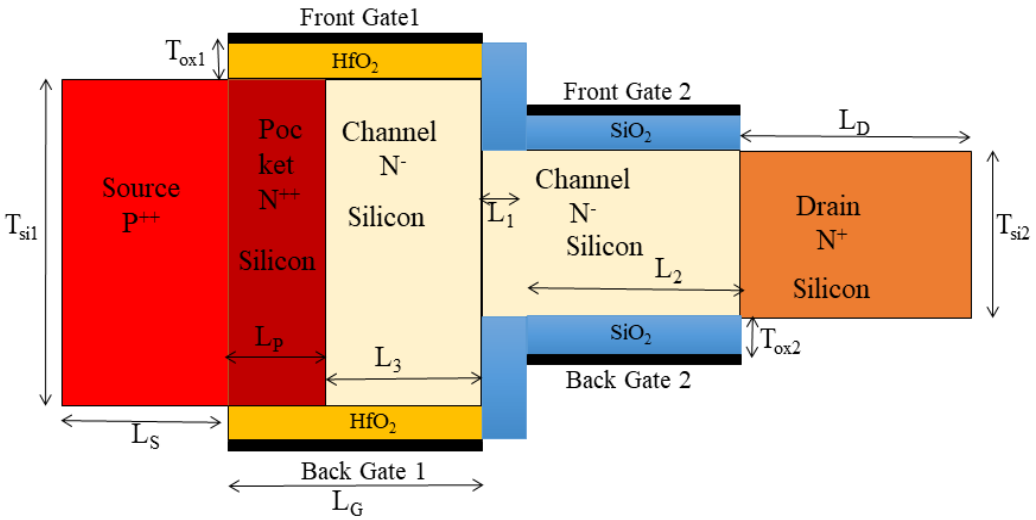


Figure 3.6 N+ Pocket based broken gate TFET device structure

The doping concentration for the N+ Pocket should be higher than that of the channel but lower than the p++ source doping to create a smooth transition in the electric field.

3.3.5 Germanium-Source N+ Pocket BG-TFET (Ge-S N+ Pocket BG-TFET)

Figure 3.7 predicts Germanium-source N^+ pocket broken-gate TFET structure, which amalgamates features from both the Germanium-source broken-gate TFET and the N^+ pocket broken-gate TFET. Initially, the device structure includes a Germanium source integrated into the broken-gate TFET configuration, where the gate is split into two segments, flanking the channel. Subsequently, a highly doped N^+ Pocket is introduced near the source-channel junction. The parameters detailed in this work, gate oxide thickness, channel length, work function, etc are summarized in Table 3.3

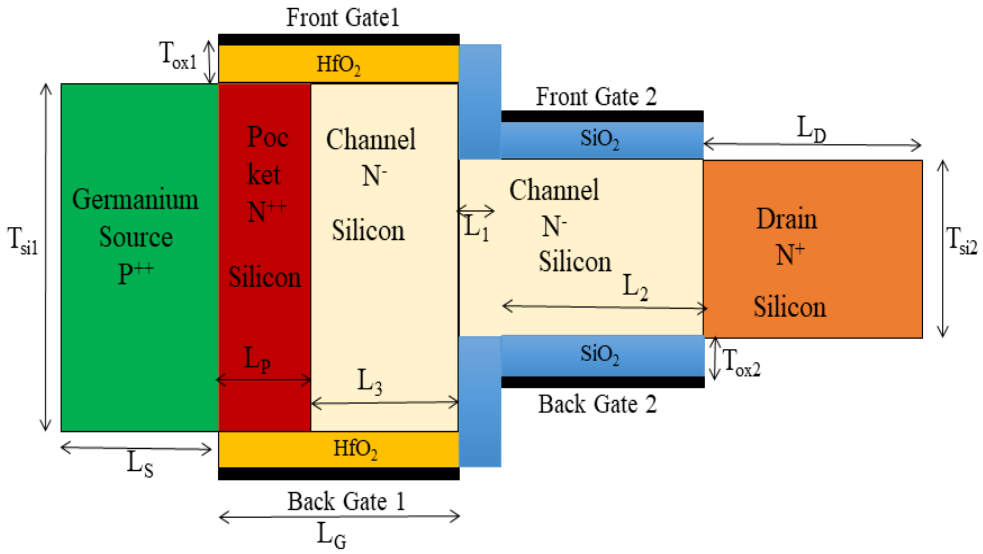


Figure 3.7 Structure of Germanium-Source N+ Pocket Broken-Gate TFET

Table 3.3 Parameters used for simulation

Parameters	DGTFET	BG-TFET	Ge-BG-TFET	N+ Pocket BG-TFET	Ge-S N+ Pocket BG-TFET
L_1, L_2, L_3, (nm)	L_{ch}=21	2, 8, 8	2, 8, 8	2, 8, 8	2, 8, 8
T_{ox1}, T_{ox2} (nm)	2	2, 2	2, 2	2, 2	2, 2
T_{si1}, T_{si2} (nm)	18	18, 10	18, 10	18, 10	18, 10

Source Length (L_S) (nm)	10	10	10	10	10
Drain Length (L_D) (nm)	16	16	16	16	16
Pocket Length (Lp) (nm)	-	-	-	4	4
Channel Doping conc. (/cm^3)	1e17	1e17	1e17	1e17	1e17
Drain Doping conc. /cm^3	5e18	5e18	5e18	5e18	5e18
Source Doping conc. /cm^3	5e20	5e20	5e20	5e20	5e20
Pocket Doping conc. /cm^3	-	-	-	2e19	2e19
Work Function of Gate 1 (eV)	4.06	4.06	4.06	4.06	4.06
Work Function of Gate 2 (eV)	-	4.26	4.26	4.26	4.26

3.3.6 Overview of Fabrication Process

The fabrication process for the Germanium-Source N+ Pocket Broken Gate TFET structure, as shown in the Figure 3.7, involves several key steps to form the various regions and layers of the device. Here is an overview of the fabrication process:

1. **Substrate Preparation:**
   - Start with a silicon substrate that will form the base for the device.
2. **Germanium Source Region Formation:**

- Deposit a layer of Germanium (Ge) on the silicon substrate.
- Dope the Ge layer with a high concentration of P-type dopants to form the P++ source region (L_S)

3. **N+ Pocket Formation:**
   - Perform localized ion implantation or epitaxial growth to create the N+ pocket region adjacent to the Germanium source.
   - Ensure precise control of the doping concentration (N++) and the pocket length (Lp)
4. **Channel Formation:**
   - Form the N- channel region next to the N+ pocket by either ion implantation or epitaxial growth with a lower concentration of N-type dopants.
   - This region includes the lengths L_1, L_2 and L_3 as depicted in the Figure 3.7.
5. **Oxide Layer Deposition:**
   - Deposit high-k dielectric material, such as HfO_2, on the surface of the channel and source regions to form the gate dielectric layers T_{ox1} and $T_{ox2.}$
6. **Gate Formation:**
   - Pattern and etch to form the front gate (Front Gate 1) and back gate (Back Gate 1) over the high-k dielectric layer near the source region.
   - Use a similar process to form the second front gate (Front Gate 2) and back gate (Back Gate 2) over the high-k dielectric layer near the drain region.
7. **Drain Formation:**
   - Deposit silicon material on the substrate where the drain region will be formed.
   - Dope this silicon region with a high concentration of N-type dopants to form the N+ drain region.
8. **Oxide Layer Deposition (SiO_2):**
   - Deposit silicon dioxide (SiO_2) layers near the drain end and also on the second front and back gate regions for additional insulation.
9. **Patterning and Etching:**
   - Use photolithography and etching techniques to define and isolate the various regions of the device, ensuring the correct alignment and dimensions.
10. **Metal Contacts Formation:**

- Deposit metal layers to form electrical contacts to the source, drain, and gate regions. Aluminum is typically used for these connections.

11. **Finalization:**
    - Anneal the device to activate the dopants and repair any damage caused during ion implantation.
    - Perform final passivation and encapsulation to protect the device from environmental factors.

This detailed process ensures that each region of the TFET is accurately formed, and the materials and doping profiles are precisely controlled to achieve the desired electrical characteristics and performance metrics.

3.5 Germanium-Source N+ Pocket Broken-Gate TFET Based Biosensor

The depicted 2D cross-sectional illustration of the Ge-S N+ Pocket BG-TFET biosensor, as shown in Figure 3.8, provides a comprehensive depiction of the spatial arrangement of the biosensor. The biomolecules targeted for detection, situated beneath the overlapped gate-on-source oxide within the nanocavity, exhibit a curled configuration. Within the nanocavity area covered by the overlapping gate-on-source structure, the biomolecules are absorbed and affixed by a 2 nm thick layer of oxide (HfO_2). The simulation parameters are listed in Table 3.4 and other parameters are the same as the previous section.

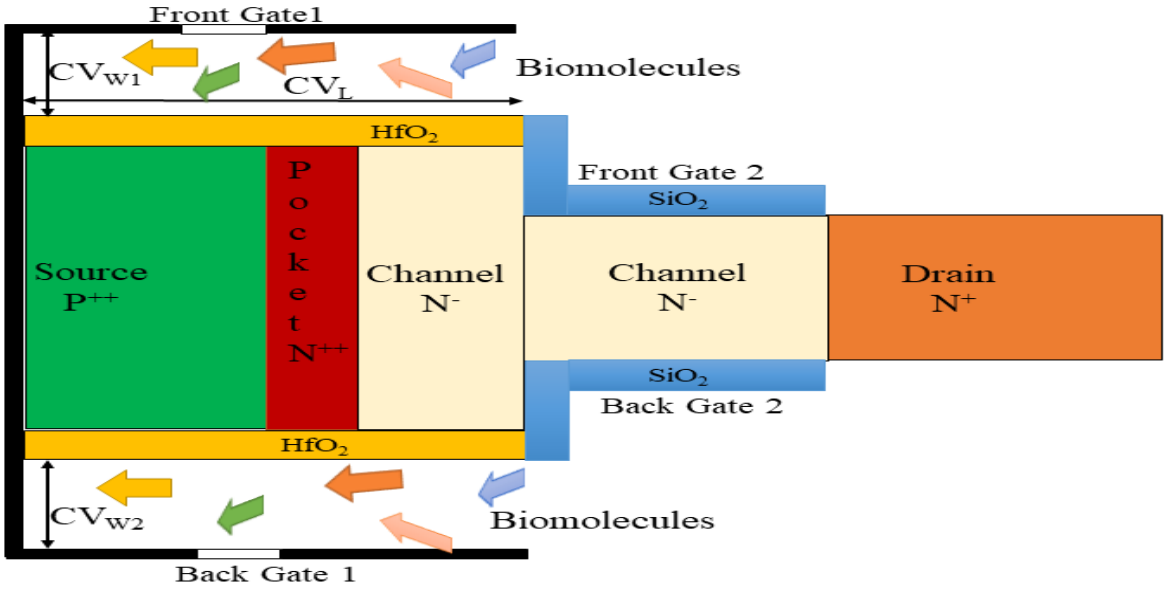


Figure 3.8 Device structure of Ge-S N+ Pocket BG-TFET based biosensor

Table 3.4 Parameters used for simulation of biosensor

Parameters	Values
L_1, L_2, L_3 (nm)	2, 8, 8
T_{ox1}, T_{ox2} (nm)	2, 2
T_{si1}, T_{si2} (nm)	18, 10
Source Length (L_S) (nm)	10
Drain Length (L_D) (nm)	16
Pocket Length (Lp) (nm)	4
Channel Doping conc. (/cm^3)	1e17
Drain Doping conc. (/cm^3)	5e18
Source Doping conc. (/cm^3)	5e120
Pocket Doping conc. (/cm^3)	2e19
Work Function of Gate 1 (eV)	4.06
Work Function of Gate 2 (eV)	4.26
Cavity Length (CV_L) (nm)	31
Cavity Width (CV_{W1}, CV_{W2}) (nm)	10, 10

CHAPTER FOUR

4 RESULT AND DISCUSSION

In order to maximize the flow of current throughout the optimization process, four main aspects have to be in balance: I_{ON}, minimizing I_{OFF}, decreasing the undesired flow of both positive and negative charges, and attaining a favorable SS. Since these traits usually conflict (e.g., decreasing ambipolarity can limit I_{ON} and boosting I_{ON} frequently raises I_{OFF}), the final design selections, including size and doping levels, were determined by finding a middle ground that considers all four properties.

4.1 Comparison of Transfer Characteristics of Double Gate and Broken Gate TFET

The BG-TFET performs better than DGTFETs in terms of I_{ON} and ambipolarity at 1V and 0.5V of drain voltage, respectively as shown in Figure 4.1 and Figure 4.2. The double-gate TFETs offer better control over short-channel effects and improved subthreshold performance compared to single-gate TFETs, but still there are some limitations, as higher leakage currents and less effective suppression of ambipolar behavior.

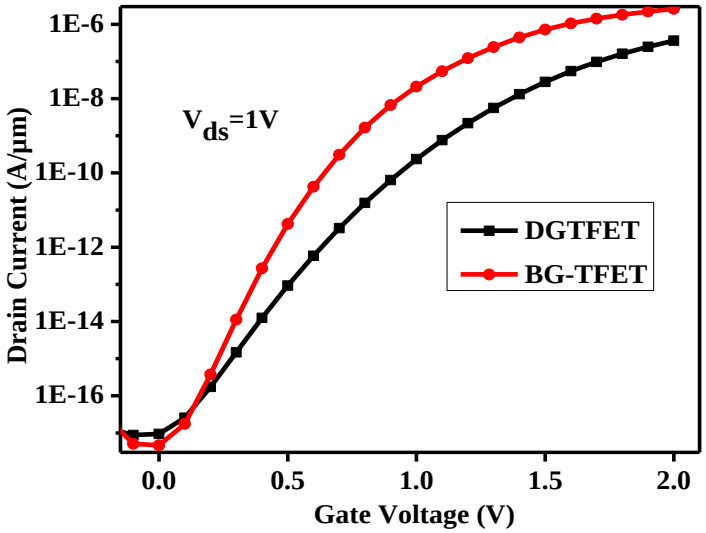


Figure 4.1 Transfer characteristics of Double Gate TFET and Broken Gate TFET

The broken-gate TFET addresses these issues by introducing a discontinuity in the gate, which helps to modulate the electric field more effectively, reducing leakage currents and improving the I_{ON}/I_{OFF} ratio. By concentrating the electric field at the source-channel junction, its design improves

the efficiency of BTBT. By reducing undesired tunneling at the drain side, it also successfully reduces ambipolarity. Even though they can control the gate, double gate transistors disperse the electric field more evenly, which lowers I_{ON} and may even increase ambipolarity.

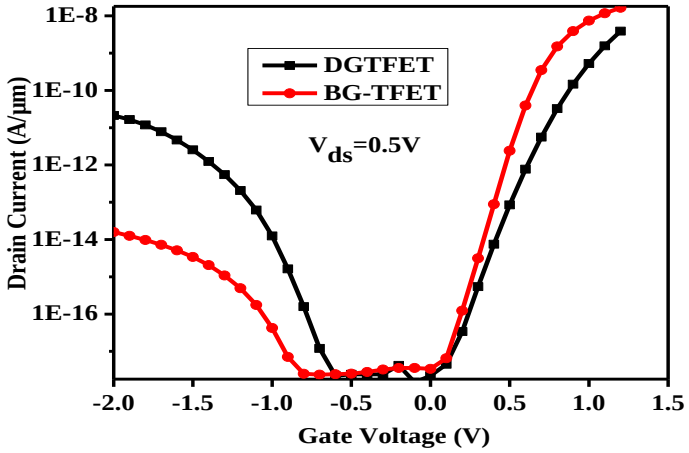


Figure 4.2 Ambipolar behavior of DGTFET and BG-TFET

In comparison to the DGTFET, the BG-TFET exhibits a more noticeable and acute band bending at the source, as seen in the Figure 4.3. The tunneling width between the valance band of the source side and the conduction band of the drain side is decreasing in BG-TFET.

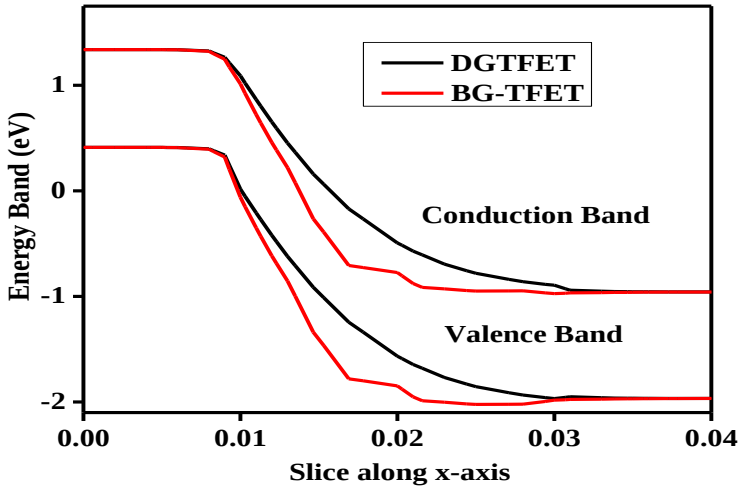


Figure 4.3 Energy Band diagram of DGTFET&BG-TFET in OFF-state

Moreover, the BG-TFET's conduction and valence bands swiftly smooth out following the first abrupt bend, suggesting that ambipolarity is suppressed by minimizing undesirable tunneling at the drain. The electric field's influence is depicted in the Figure 4.4, with the BG-TFET displaying

a higher electric field. A greater electric field is indicated by the BG-TFET's abrupt bending, which improves BTBT efficiency and raises I_{ON}.

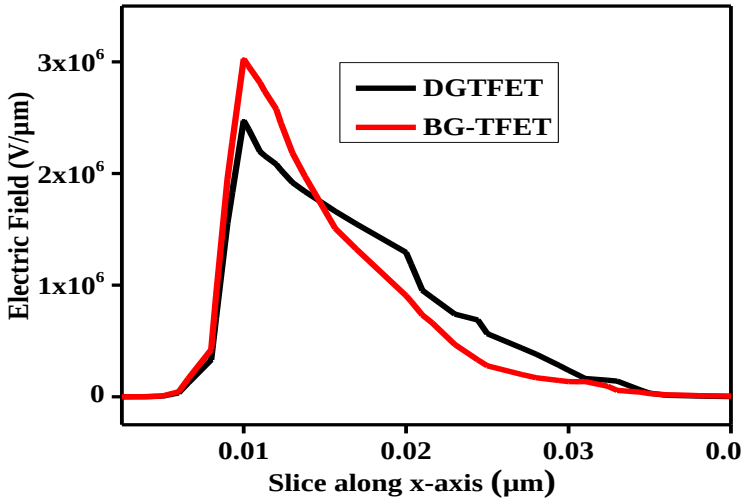


Figure 4.4 Electric Field of DGTFET and BG-TFET

BTBT is an important component in TFETs. A unique model is used in the simulations to explain this tunneling. When the device is turned off, this type reduces leakage current and enhances current flow. This is accomplished by enabling controlled tunneling over a predetermined length of time.

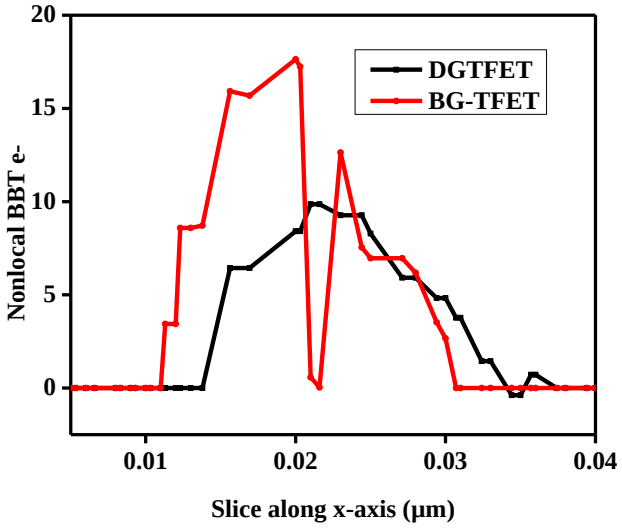


Figure 4.5 e- Non-local BTBT

Notably, in Figure 4.5 the nonlocal BBT rate is depicted, from the figure it is observed that at BG-TFET the tunneling rate is very high comparable to others, which suggests that they could be used in low-power applications.

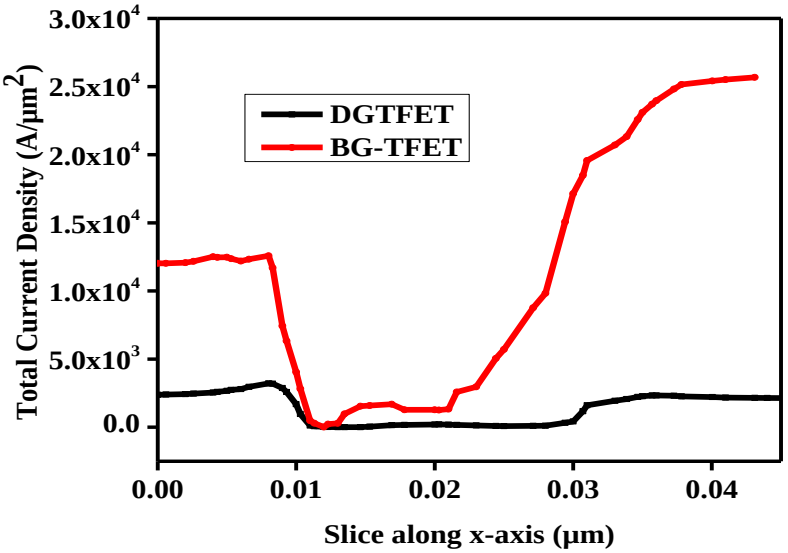
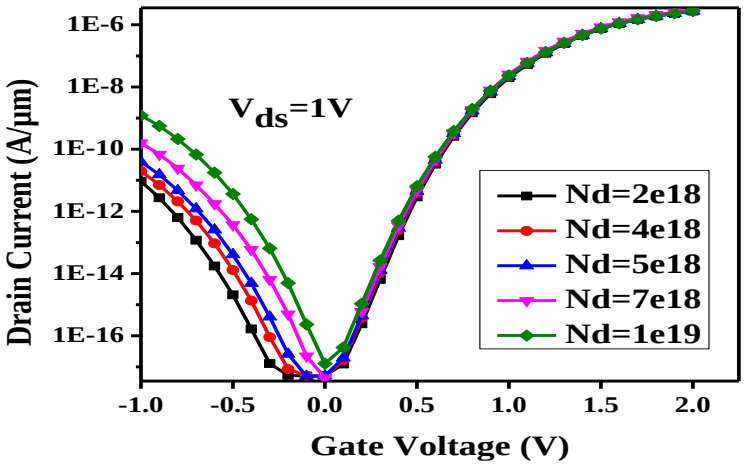


Figure 4.6 Total Current Density along X-axis

Figure 4.6 illustrates the comparison in current density profiles between the BG-TFET and the DGTFET. The BG-TFET demonstrates a more intricate current density pattern, with a notable rise towards the device's end, due to the enhanced electric field modulation from the broken gate structure.

4.1.1 Effect of drain doping concentration analysis

Doping concentration affects the flow of current through a transistor, with higher doping allowing more current to flow. BG-TFETs have a gate designed to control current flow more precisely. However, higher doping increases I_{OFF}, this leads to increased ambipolarity as illustrated in Figure 4.7 and Figure 4.8. A balance must be struck between achieving high I_{ON} and minimizing ambipolarity, as higher doping can make it harder to turn off the transistor.



*Fi*gure 4.7 Drain doping concentration analysis at Vds=1V

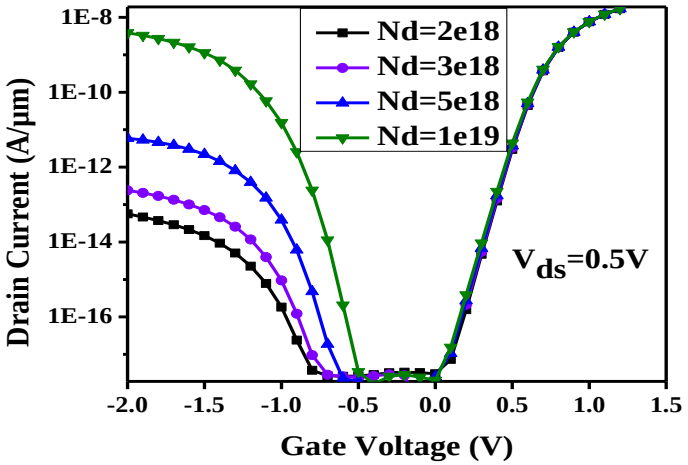


Figure 4.8 Drain doping concentration analysis at Vds=0.5V

4.1.2 Effect of split drain on BG-TFET

To reduce the ambipolar behavior of the devices the split drain design is incorporated into the proposed BG-TFET structure. By splitting the TFET's drain region into two regions, the design serves to improve device performance by lowering ambipolarity and increasing the tunneling width at the channel-drain interface. Here we can apply the high doping concentration of $5e^{18}/cm^3$ to the upper part and lower doping concentration $1e^{17}$ $/cm^3$ to the lower part of the drain (as in Figure 3.4a) with V_{ds} of 1V. As it is observed from the Figure 4.9 applying the split drain to the BG-TFET improves it's ambipolarity without affecting the other parameters.

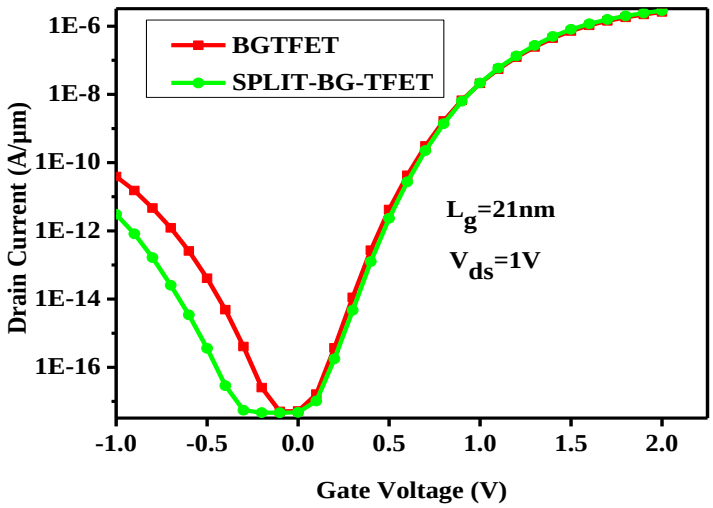


Figure 4.9 Effect of split drain on BG-TFET

The effect of altering the split drain's higher doping concentration portion on the device at Vds=1V is depicted in Figure 4.10. It has been demonstrated that raising the split drain's higher doping concentration component enhances the device's capacity to conduct in both the ON and OFF states, making switching more appropriate.

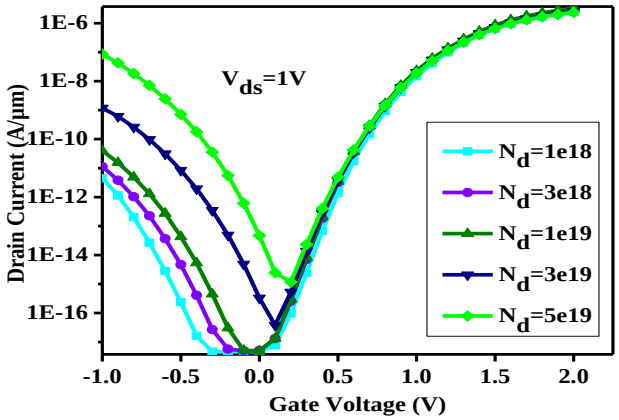


Figure 4.10 High doping concentration analysis of Split-drain BG-TFET

4.1.3 Impact of gate on drain underlap

Figure 4.11 illustrates the analysis of the BG-TFET's ambipolar conduction in relation to the underlap length (G_{UDL}). In underlap structure the gate electrode shorten than the dielectric oxide region and due to which the overlap capacitance is going to be improved. The graph shows that the I_{ON} stays constant as the G_{UDL} is increased from 3 nm to 7 nm due to the BG-TFET's narrow channel. The underlap length grows as the source/drain areas and the gate get farther apart. This results in a lowering of the electric field strength at the channel-drain connections. Ambipolar conduction decreases because the electric field can no longer efficiently facilitate carrier

movement from the channel to the drain zone. It is significant to remember that although the I_{ON} has a significant influence on ambipolar conduction, it is independent of the underlap length.

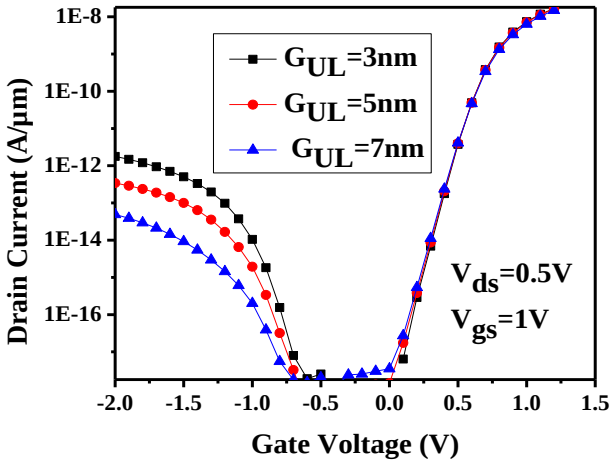


Figure 4.11 Impact of gate on drain underlap

4.2 Germanium-Source Broken Gate TFET (Ge-BG-TFET) Analysis

Germanium-TFETs have a smaller band gap and higher electron mobility compared to silicon-based TFETs. This allows for better tunneling and I_{ON}, while Si-source TFETs rely more on lateral tunneling. Germanium-TFETs often use a germanium-around-source (GAS) structure for better gate control and tunneling. They generally exhibit higher I_{ON}, lower SS, and better overall performance compared to silicon-based TFETs. As illustrated in Figure 4.12 the Ge-BGTFT outperforms the Silicon BGTFT in terms of drain current, threshold voltage, and SS, offering higher I_{ON}, lower gate voltage, and faster switching for low power applications.

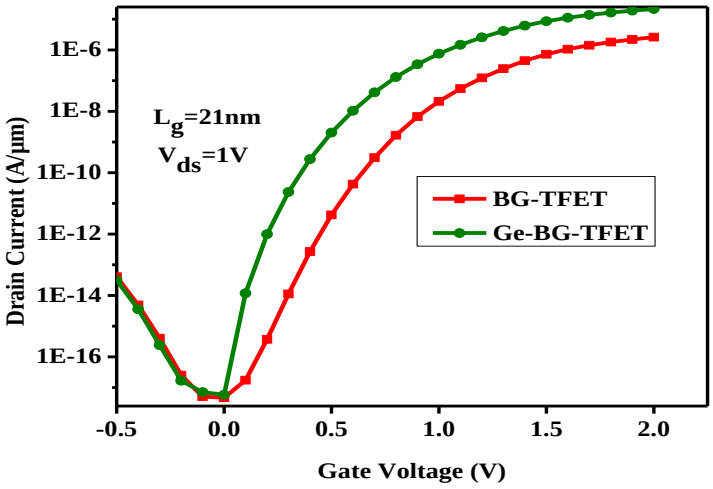


Figure 4.12 Transfer characteristics of silicon-BG-TFET and Germanium-BG-TFET

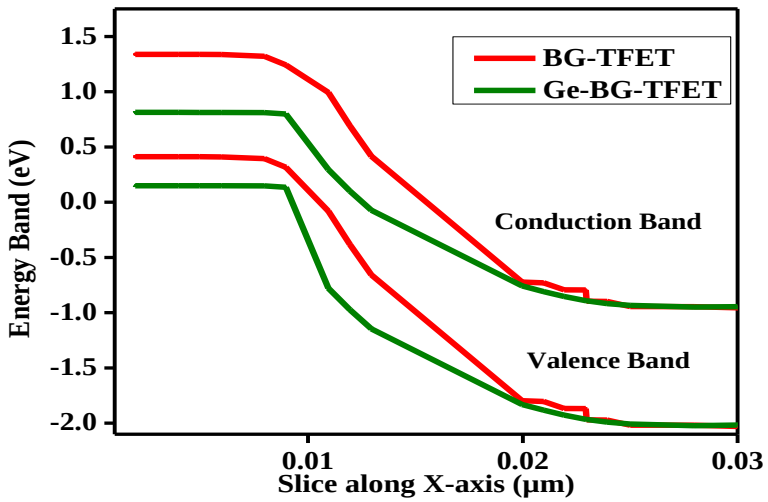


Figure 4.13 Energy band of Si-BG-TFET and Ge-BG-TFET in OFF-state

Figure 4.13 shows the comparison of Si-BG-TFET and Ge-BG-TFET significant differences in energy band diagrams. Ge-BG-TFET has a narrower bandgap due to Germanium's intrinsic properties, higher tunneling efficiency, and stronger band bending.

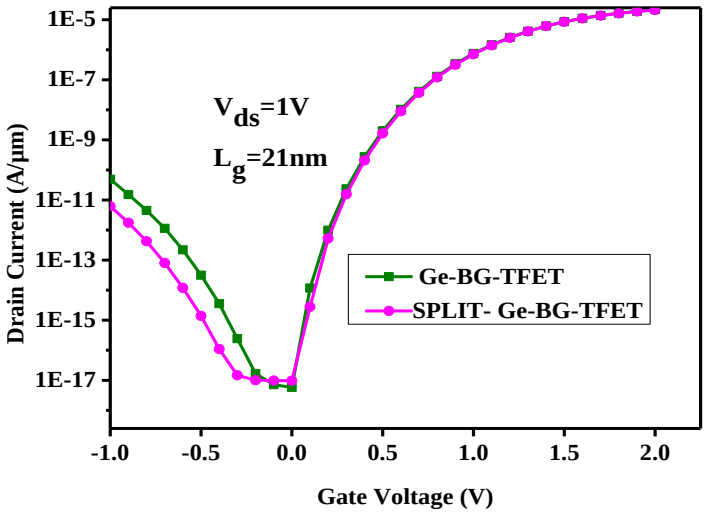


Figure 4.14 The effect of split drain on Ge-BG-TFET

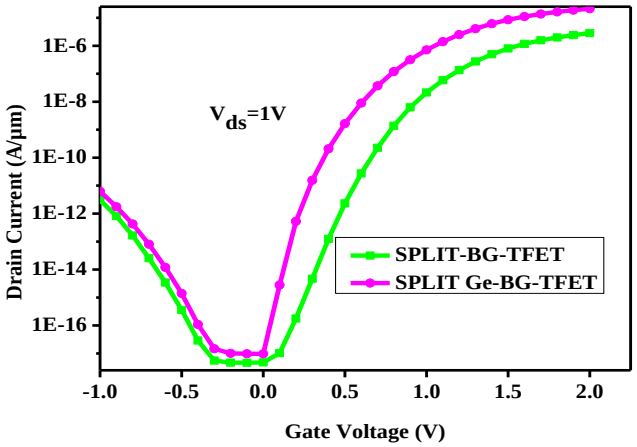


Figure 4.15 Effect of Ge-source on split drain BG-TFET

Figure 4.14 shows the impact of split drain i.e., upper part has higher doping while lower part has lower doping on Id-Vg of Germanium source Broken gate TFET and broken gate TFET and Figure 4.15 shows that the Id-Vg comparison of drain split on the performance of Ge-BG-TFET and Split BG-TFET. From the figure it is observed on decreasing the doping of the upper part the drain current at negative x axis is going to be decreased.

4.3 N^+ Pocket Broken Gate TFET (N^+ Pocket BG-TFET) Analysis

This sub-section blends a broken gate structure with a N^+ Pocket at Vds=1V as illustrated in Figure 4.16. The broken gate structure affects channel control and current flow, whereas the N^+ Pocket improves tunneling and drive capability. By carefully coupling the N^+ Pocket with the broken gate structure, this design affects SS, leakage current, optimizing tunneling characteristics and efficiency.

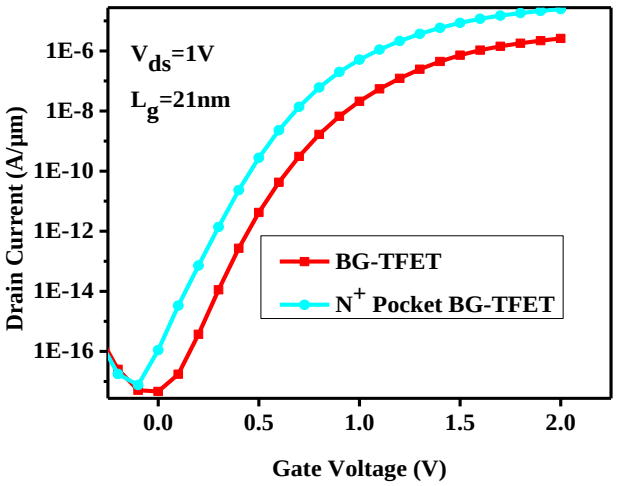


Figure 4.16 Transfer characteristics of source pocketed broken gate TFET & BG-TFET

Figure 4.17 displays the drain current vs. gate voltage curves for three different types of TFETs at a constant Vds of 1V. A N^+ Pocket BG-TFET, BG-TFET, and DGTFET are the devices that are being compared. In the N^+ Pocket BG-TFET, the pocket's length (L_p) is taken as 4 nm.

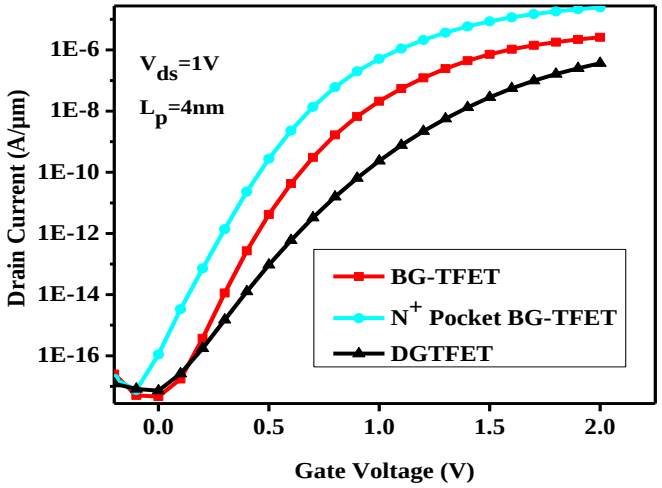


Figure 4. 17 Comparison of DGTFET, BG-TFET & N+ Pocket BG-TFET

The maximum drain current is displayed by the N^+ Pocket BG-TFET device over the whole gate voltage range. By efficiently adjusting the electric field, the N^+ pocket's existence aids in enhancing the tunneling rate.

4.3.1 Analysis of Varying Pocket Length on Performance of N^+ Pocket BG-TFET

As seen from the Figure 4.18 increasing pocket length can increase the I_{ON} of BG-TFET at the cost of leakage current. So, for better improvement of the device, pocket length of 4nm is used at Vds=1V and performance of the device is improved compared to BG-TFET. On increasing the pocket length actually due to the different band gap of silicon germanium the strain is induced near the pocket region that's the way the current is going to be increased.

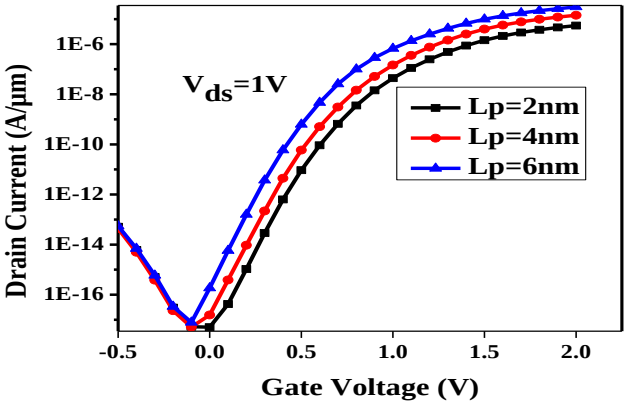


Figure 4.18 Pocket length analysis of N+ Pocket BG-TFET

4.3.2 Effect of pocket doping concentration on N+ Pocket BG-TFET

The performance of a N^+ pocket BG-TFET is highly dependent on the doping concentration in its pocket region. It impacts Drain-Induced Barrier Lowering (DIBL), SS, V_{th} regulation, and tunneling barrier.

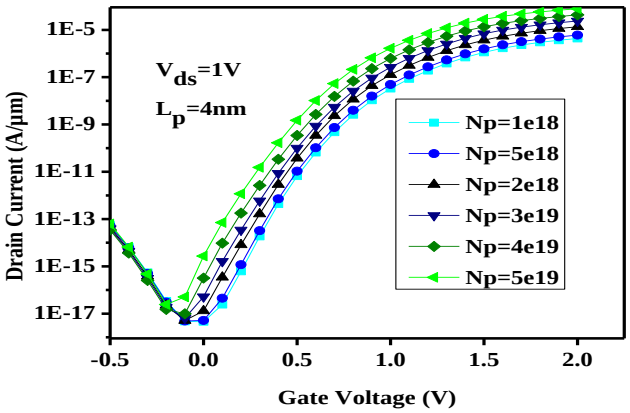


Figure 4.19 N+ Pocket-doping concentration analysis

Increased doping concentrations improve I_{ON} by causing tunneling barriers to become smaller and lower. Increased doping concentrations also lessen subthreshold slope and enhance V_{th} regulation as observed from Figure 4.19 with little change in leakage current of the device.

Figure 4.20 displays nearly identical electric field profiles for both devices, with a peak in the electric field close to the source region (around 0.01 μm). For effective BTBT, a high electric field concentration is indicated by the sharp peak. The fact that the electric field profiles are comparable indicates that both systems concentrate the electric field at the source-channel junction in order to achieve efficient tunneling. Given that the devices' electric field distribution performance is comparable, any discrepancies in on-current and ambipolarity performance between them are most likely the result of additional structural optimizations in the source-pocketed TFET or material properties.

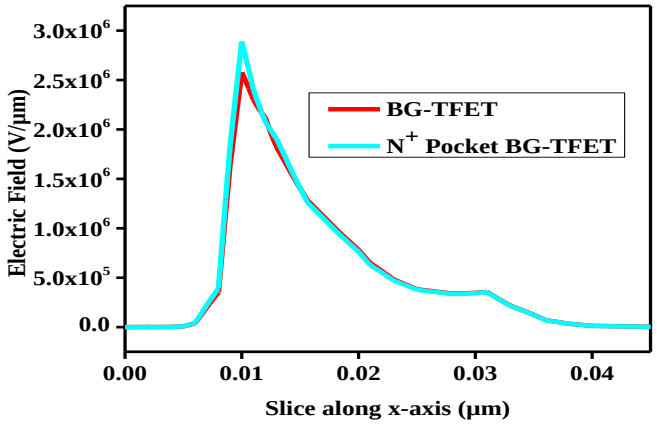


Figure 4.20 Electric Field of BG-TFET & N+ Pocket BG-TFET

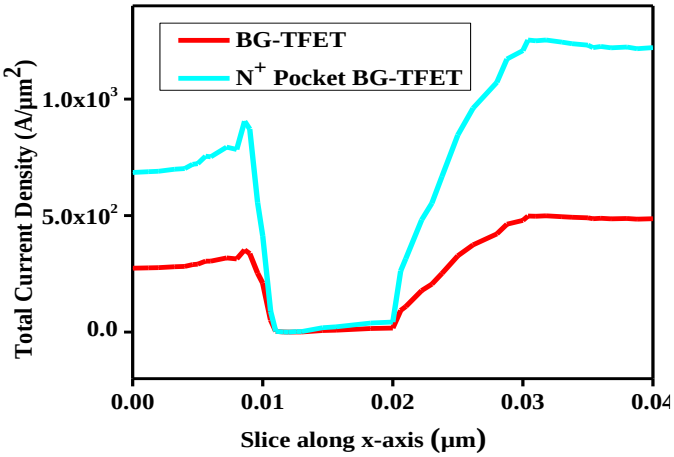


Figure 4.21 Total Current Density of BG-TFET & N^+ Pocket BG-TFET

Figure 4.21 indicates that the incorporation of the N^+ pocket in the N^+ Pocket BG-TFET structure effectively enhances carrier injection and band-to-band tunneling, resulting in a higher total current density and improved overall device performance

4.4 Germanium-Source N^+ Pocket Broken Gate TFET (Ge-S N^+ Pocket BG-TFET)

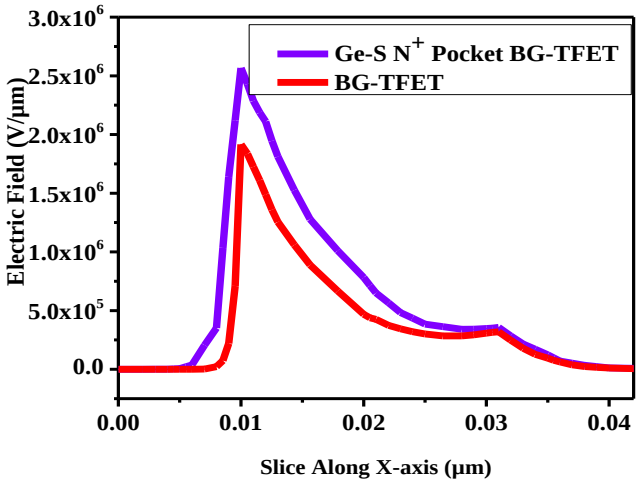


Figure 4.22 Electric Field comparison Ge-S N+ Pocket BG-TFET & BG-TFET

In Figure 4.22 the increased electric field is a result of incorporating the Germanium source and N+ pocket, which enhances the BTBT process, thereby improving the overall performance of the device. The higher electric field in the Ge-S N+ Pocket BG-TFET indicates more efficient carrier injection and contributes to a higher ON-current, validating the effectiveness of the modifications in the TFET structure.

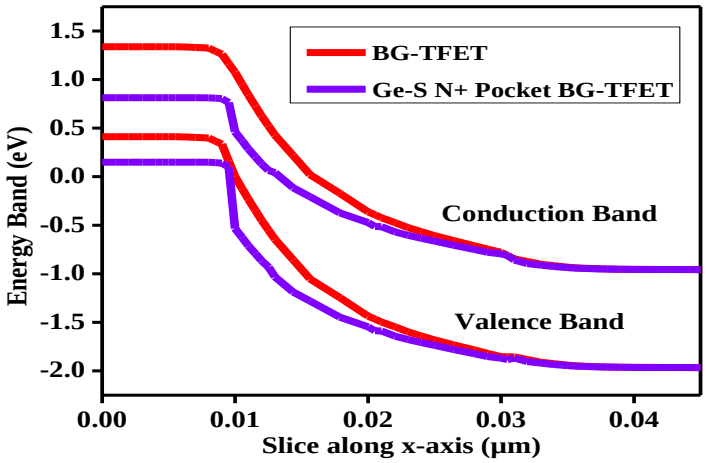


Figure 4.23 Band Diagram of BG-TFET & Ge-S N+ Pocket BG-TFET

The energy band diagram in Figure 4.23 indicates the conduction band and valence band edges for both structures. The Ge-S N^+ Pocket BG-TFET exhibits a steeper and narrower energy bandgap near the source-channel junction compared to the BG-TFET

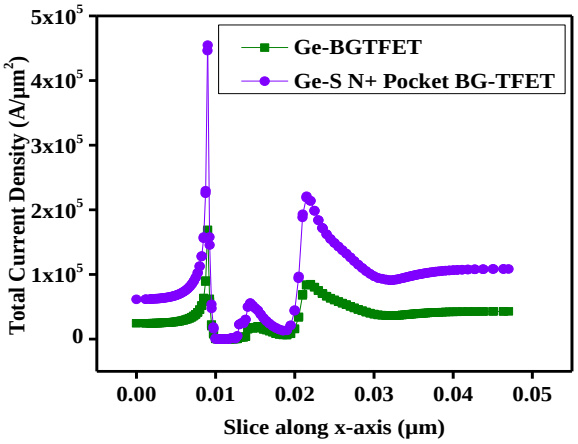


Figure 4.24 Total Current Density of Ge-BG-TFET & Ge-S N+ Pocket BG-TFET

Figure 4.24 shows that the Ge-S N+ Pocket BG-TFET has higher peak current densities and a more uniform current density along its length compared to the Ge-BG-TFET. This suggests that the N+ Pocket in the Ge-S N+ Pocket BG-TFET enhances electric field modulation, resulting in higher and more localized current densities, suggesting a trade-off between peak performance and consistent current densities.

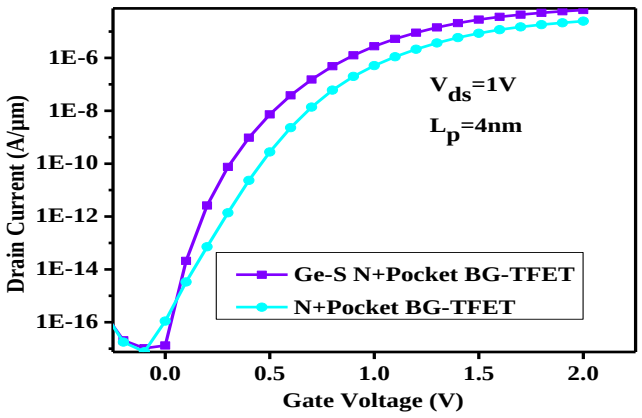


Figure 4.25 Si N+ Pocket BG-TFET vs Ge-S N+ Pocket BG -TFETμ

Figure 4.25 compares drain current and gate voltage for standard N+ Pocket BG-TFET and Ge-S N+ Pocket BG-TFET. Both devices show an increase in drain current with gate voltage. Ge-S N+ Pocket BG-TFET consistently shows higher drain current values compared to N+ Pocket BG-TFET at the same gate voltages. The germanium source with N+ Pocket structure improves device performance interms of I_{ON}, SS and V_{th}

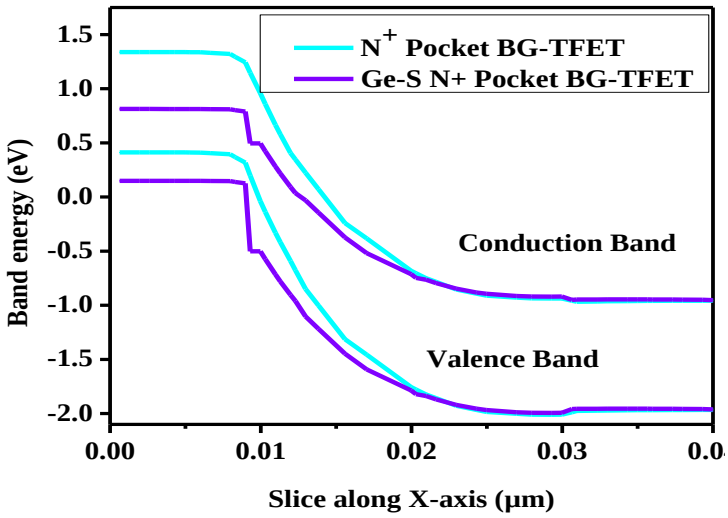


Figure 4.26 Energy band of Si N+ Pocket BG-TFET and Ge-S N+ Pocket BG-TFET

Figure 4.26 shows the comparison of Si N^+ Pocket BG-TFET and Ge-S N^+ Pocket BG-TFET shows significant differences in energy band diagrams. Ge-S N^+ Pocket BG-TFET has a narrower bandgap due to Germanium's intrinsic properties, higher tunneling efficiency, and stronger band bending. Both devices show similar band alignment, with lower energy levels in the Ge-S N^+ Pocket BG-TFET indicating germanium incorporation enhancing carrier injection and performance.

Because of the combined advantages of two structures, the Ge-S N^+ Pocket BG-TFET is the most favorable option for low-power applications. By reducing the energy barrier for electron tunneling, this arrangement uses germanium at the source to obtain the maximum tunneling efficiency. In order to reduce leakage currents and achieve low-power operation, the N+ Pocket further sharpens the band bending, boosting the SS and providing more control over the tunneling process.

While the Ge-BG-TFET does not have the N^+ pocket's additional electric field modulation, it nevertheless has good I_{ON} and efficiency. Although it has less leakage and excellent control over the electric field, the germanium's short bandgap does not help the N^+ Pocket BG-TFET. Consequently, the ideal option for low-power applications is the hybrid Ge-S N^+ Pocket BG-TFET design, which offers an excellent compromise between high performance and low power consumption. The comparison of the whole structure is presented in Table 4.1.

Table 4.1 Comparison of the proposed structure with existed work for different parameters

Structures	Parameters				
	I_{ON} (A/µm)	I_{OFF} (A/µm)	I_{ON}/I_{OFF}	SS (mV/decade)	V_{th} (V)
DGTFET	3.68e-07	7.25e-018	5.1e+010	59.1	1.18
BG-TFET (Dutta & Sarkar)	1.07e-06	2.77e-018	3.87e+011	45.55	0.52
Ge-BG-TFET (This work)	6.52e-05	4.49e-018	1.45e+013	29.36	0.47
N^+ Pocket BG-TFET (This work)	1.09e-04	3.97e-018	2.75e+013	57	0.295
Ge-S N^+ Pocket BG-TFET (This work)	1.82e-04	4.03e-018	4.51e+013	29.12	0.375

4.4.1 Comparison of Novel Structure with Different Works

In this section we have put the comparison of different works on source engineered with the novel structure we have proposed for more clarity. It is summarized in Table 4.2.

Table 4.2 Comparison with different works

Structures	Parameters				
	I_{ON} (A/µm)	I_{OFF} (A/µm)	I_{ON}/I_{OFF}	SS (mV/decade)	V_{th} (V)
High-K SC-TFET (S. Kumar et al., 2020)	1.36×10^{-4}	2.47×10^{-16}	5.53×10^{11}	15	1
PNPN TFET (S. Kumar et al., 2022)	4.78×10^{-4}	1.92×10^{-14}	9.38	24	0.23
HJ-HD-P-DGTFET (Chen et al., 2023)	7.8×10^{-5}	8.2×10^{-18}	10^{12}	19	-
Ge-S N^+ Pocket BG-TFET (This work)	1.82e-04	4.03e-018	4.51e+013	29.12	0.375

4.5 Utilizing Ge-S N^+ Pocket BG-TFET for Biosensing Application

Evaluating a biosensor's performance often involves comparing the device's behavior with cavities that are either empty or filled. An empty cavity, has a relative permittivity of 1. In contrast, a filled cavity contains biomolecules with a relative permittivity greater than 1 (Vimala et al., 2022).

Table 4.3 Dielectric values of different biomolecules

Biomolecules	K-values
Air	1
Urease	1.64
Biotin	2.64
Ferrocytochrome	4.7
Bacteriophage	6.3
Keratin	8
Gelatin	12

The higher relative permittivity in a filled cavity increases the capacitance between the gate and the channel, enhancing the coupling and resulting in a stronger electric field at the tunneling junction.

Figure 4.27 illustrates a Ge-S N+ Pocket BG-TFET biosensor when comparing an empty cavity (K=1, air) to filled cavities with various dielectric constants (K).

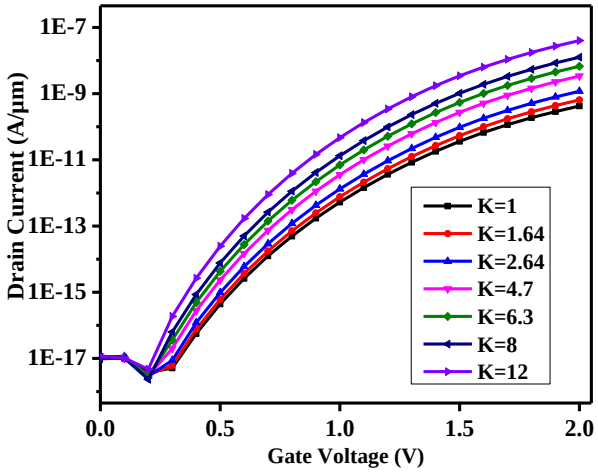


Figure 4.27 Drain current of different biomolecules and empty cavity

As the dielectric constant K increases from 1 to 12, the Drain current for a given Gate voltage also increases. This trend is observed because higher dielectric constants within the cavity enhance the capacitance between the gate and the channel, improving the coupling efficiency. Consequently, the biosensor shows higher sensitivity with filled cavities, indicating its effectiveness in detecting biomolecules with varying dielectric properties.

In this work drain current in on-state can be used as a sensitivity parameter. The mathematical expression for the sensitivity can be expressed as follows,

$$S_I = \frac{I_{D(biomolecules)} - I_{D(air)}}{I_{D(air)}}$$

Figure 4.28 shows the sensitivity of a Ge-S N+ Pocket BG-TFET biosensor, as the dielectric constant increases from 1.64 (urease) to 12 (gelatin), the sensitivity of the biosensor also increases. This indicates a direct correlation between the dielectric constant of the biomolecules and the sensor's sensitivity.

Specifically, biomolecules with higher dielectric constants, result in significantly higher sensitivity compared to those with lower dielectric constants. This enhancement in sensitivity is due to the increased capacitance and improved coupling between the gate and the channel, leading to a stronger electric field and a higher ON-current. The Ge-S N+ Pocket BG-TFET biosensor demonstrates greater sensitivity for detecting biomolecules with higher dielectric constants.

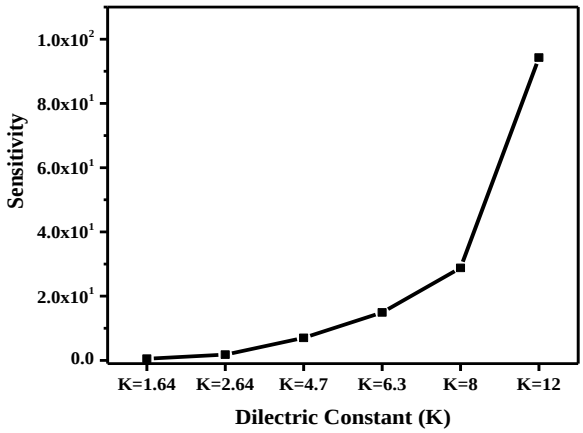


Figure 4.28 Sensitivity vs Dielectric Constant of Biomolecules

Since the electric field and the dielectric value are directly correlated, we can see from the Figure 4.29 the electric field across the device grows as the dielectric constant value rises. This is because

the work function is modulated by the dielectric modulation effect when biomolecules become immobile in the cavity area.

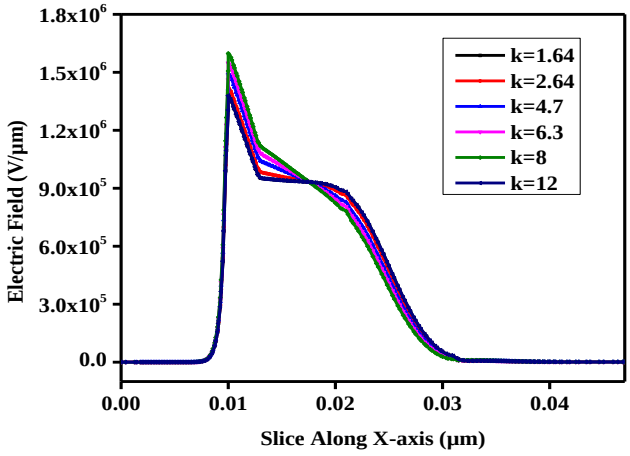


Figure 4.29 Electric field of Biosensor for different biomolecules

The energy band diagram for the different biomolecules in the biosensor of this suggested device construction is shown in Figure 4.30 for the biomolecules with different dielectric constants. To move from one lower energy level to a higher energy level, electrons require energy. Prior to tunneling, the bandgap is about 0.5 eV. Various biomolecules exhibit distinct energy levels in the valance and conduction bands during tunneling.

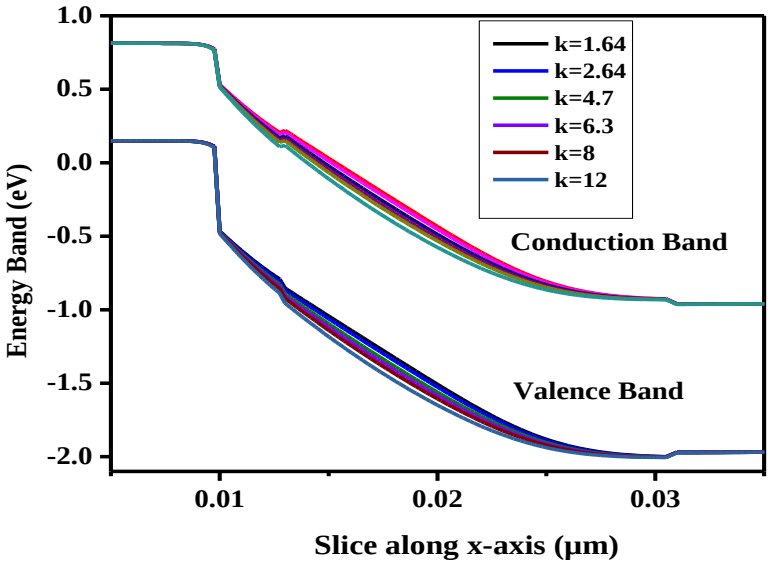


Figure 4. 30 Energy band diagram of various biomolecules

Figure 4.31 indicate how the current density varies spatially within the biosensor. At K=12 current density significantly increases, peaking sharply after 0.04 µm, suggesting a strong dependence on this parameter.

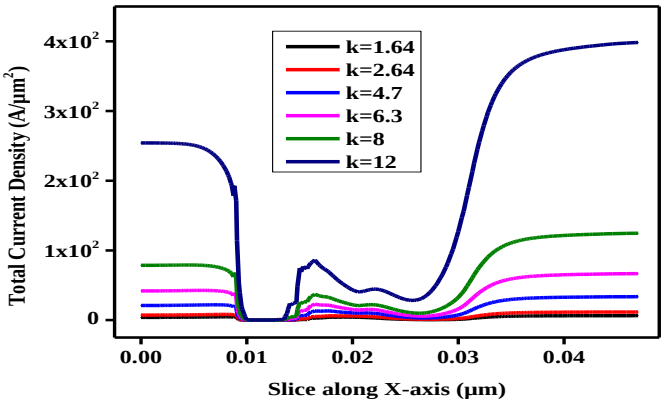


Figure 4.31 Total current density of various biomolecules

Other values of K, such as 1.64 (black) and 2.64 (red), show much lower and relatively stable current densities. The green (K=8), magenta (K=6.3), and pink (K=4.7) curves exhibit intermediate behaviors, with slight increases in current density around the 0.02 to 0.04 µm range. These variations underscore the influence of K on the biosensor's performance, affecting the distribution and magnitude of current density within the device.

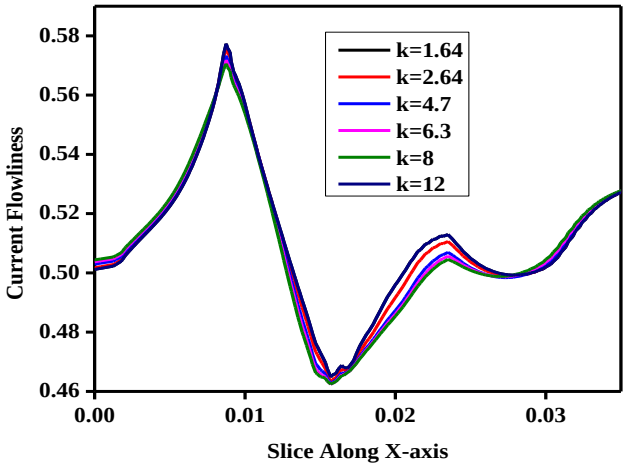


Figure 4.32 Current flowliness of different biomolecules

Figure 4.32 shows the current flowlines for a Ge-S N+ Pocket BG-TFET biosensor, plotted against the slice along the x-axis for different values of the parameter. The various curves, each corresponding to a different K value illustrate how the current flow responds to changes in the x-

axis position within the biosensor. The peaks and troughs in the graph indicate regions of high and low current flow, respectively, reflecting the sensor's sensitivity and performance. The consistent overall pattern across different values suggests a stable behavior of the biosensor's current flow characteristics despite variations in K.

4.6 Surface Potential of Proposed Structure

From 2D-Poisson equations

$$\frac{d^2\psi(x,y)}{dx^2}+\frac{d^2\psi(x,y)}{dy^2}=\frac{-qN_i}{\epsilon_{si}} \tag{4.1}$$

Neglecting the influence of mobile charges, the general solution to Equation (4.1) is given by

$$\psi_i(x,y)=C_{0,i}(x)+C_{1,i}(x)y+C_{2,i}(x)y^2 \tag{4.2}$$

where, subscript "ï" represents each of the fire regions.

To obtain the coefficients $C_{j,i}(x)$:

We consider the following boundary conditions.

I. $$\psi_i(x,0)=\psi_{s,i}(x)\ and\ \psi_i\left(x,t_{si,i}\right)=\psi_{s,i}(x) \tag{4.3a}$$

II. $$\frac{d\psi_{s,i}(x)}{dy}\Big|y=0=\frac{\eta_i\psi_{s,i}(x)-\psi_{G,i}}{t_{si,i}} \tag{4.3b}$$

III. $$\frac{d\psi_{s,i}(x)}{dy}\Big|y=t_{si,i}=\frac{-\eta_i\psi_{s,i}(x)-\psi_{G,i}}{t_{si,i}} \tag{4.3c}$$

Where, $$\eta_i=\frac{C_{ox,i}}{C_{si,i}}\ for\ i=2,3,4,5\&6$$

$$\eta_i=\frac{C_{ox,i}}{C_{Ge,i}} \quad \text{for } i\text{=1} \quad \text{and}$$

$$C_{ox,i}=\frac{\epsilon_{ox,i}}{t_{ox,i}}\ for\ i=2,3\ \&\ 5$$

For narrow, Region 4, $C_{ox,4}=(\frac{2}{\pi})(\frac{\epsilon_{ox,4}}{t_{ox,4}})$ which is due to the fringing effect.

Similarly, for Regions 1 and 6

$$C_{ox,1}=(\frac{2}{\pi})(\frac{\epsilon_{ox,1}}{t_{ox,1}})$$

$$C_{ox,6}=(\frac{2}{\pi})(\frac{\epsilon_{ox,6}}{t_{ox,6}})$$

$$C_{si,i}=(\frac{2}{\pi})(\frac{\epsilon_{ox,i}}{t_{si,i}})$$

$$C_{Ge,1} = (\frac{2}{\pi})(\frac{\epsilon_{ox,1}}{t_{Ge,1}})$$

where

$C_{ox,i}$ Oxide capacitance at each region

$C_{si,i}$ Silicon film capacitance at each region

$t_{Ge,1}$ for region 1

$t_{si,1}$ for region 2 and 3

$t_{si,2}$ for region 4,5 and 6

$t_{ox,1}$ for regions 1, 2 and 3

$t_{ox,2}$ for regions 4, 5 and 6

$\epsilon_{ox,1}$ for regions 1, 2 and 3

$\epsilon_{ox,2}$ for regions 4, 5 and 6, and for all region $\epsilon_{si,i,}\ is\ \epsilon_{si}$ except for region 1(i.e, ϵ_{Ge} for region 1)

The Equation (4.3b) and (4.3c) are obtained from continuity of electric flux at the semiconductor dielectric boundary. Also, Equation (4.3a) is written assuming symmetry in the device across x-axis.

$\psi_{s,i}(x)$ represents the surface potential at the ith region

ψ_G is the gate potential, where $\psi_{G,i}$=$V_{G,i} - V_{fb}$ and,

$V_{fb} = \emptyset_M - \emptyset_{si}$. such that $\emptyset_{si}$=$\chi_{si} - \frac{E_g}{2}$, χ_{si} is electron affinity and E_g is the energy band gap of silicon (in eV). Equation (4.3) is modified to a certain extent for accommodating the salient nature of Regions 1, 2 and 3 as shown in Figure 4.33

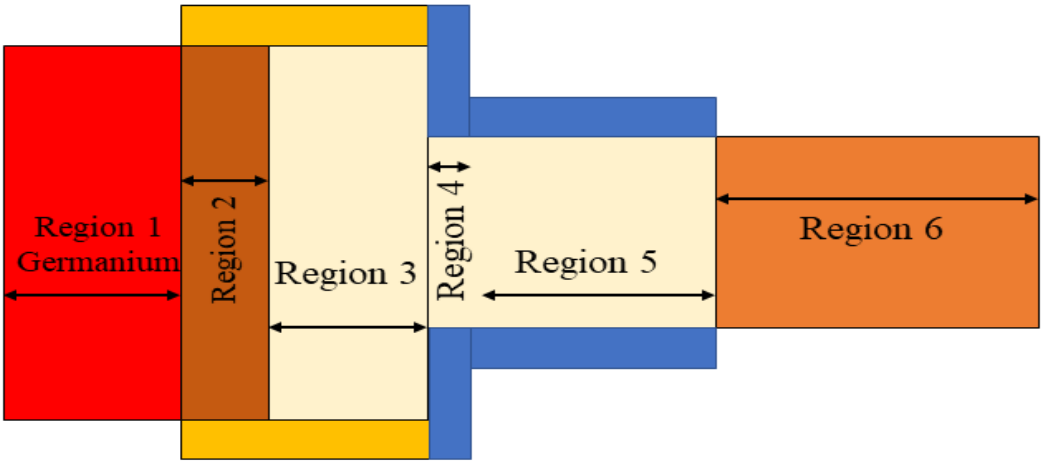


Figure 4.33 Regions of proposed structure

For Region 1

$$\psi_i(x, y = \frac{-t_{Ge,1} - t_{si,2}}{2}) = \psi_{Ge,i}(x) \tag{4.4a}$$

For Region 2

$$\psi_i(x, y = \frac{t_{si,1} + t_{si,2}}{2}) = \psi_{si,i}(x) \tag{4.4b}$$

Then

$$\frac{d\psi_{s,i}(x)}{dy} \Big| y = \frac{-t_{Ge,1} - t_{si,2}}{2} = \frac{\eta_i \psi_{s,i}(x) - \psi_{G,i}}{t_{si,i}} \tag{4.4c}$$

$$\frac{d\psi_{s,i}(x)}{dy} \Big| y = \frac{t_{si,1} + t_{si,2}}{2} = \frac{-\eta_i \psi_{s,i}(x) - \psi_{G,i}}{t_{si,1}} \tag{4.4d}$$

Now put Equation (4.3a) into (4.2)

$$\psi_i(x, 0) = \psi_{s,i}(x)$$

$$\psi_i(x, 0) = C_{o,i}(x) + C_{1,i}(x, 0).0 + C_{2,i}(x, 0).0^2 = \psi_{s,i}(x)$$

$$C_{o,i}(x) = \psi_{s,i}(x) \tag{4.5a}$$

Now put Equation (4.3b) into (4.2)

$$\frac{d\psi_{s,i}(x)}{dy} \Big| y = 0 = \frac{d}{dy} \left(C_{o,i}(x) + C_{1,i}(x, 0).y + C_{2,i}(x, 0).y^2 \right) \Big| y = 0$$

$$\frac{d\psi_{s,i}(x)}{dy} \Big| y = 0 = C_{1,i}(x)$$

From Equation (4.3b), we have

$$\frac{d\psi_{s,i}(x)}{dy}\Big|y = 0 = \frac{\eta_i\psi_{s,i}(x) - \psi_{G,i}}{t_{si,i}} = C_{1,i}(x)$$

$$C_{1,i}(x) = \frac{\eta_i\psi_{s,i}(x) - \psi_{G,i}}{t_{si,i}} \qquad (4.5b)$$

Again put Equation (4.3c) into (4.2)

$$\frac{d\psi_{s,i}(x)}{dy}\Big|y = t_{si,1} = \frac{d}{dy}\left(C_{o,i}(x) + C_{1,i}(x,0).y + C_{2,i}(x,0).y^2\right)\Big|y = t_{si,1}$$

$$= C_{1,i}(x) + 2C_{2,i}(x).y\Big|y = t_{si,1}$$

$$= C_{1,i}(x) + 2C_{2,i}(x)t_{si,1}$$

from Equation (4.3c), we have

$$\frac{d\psi_{s,i}(x)}{dy}\Big|y = t_{si,i} = \frac{-\eta_i\psi_{s,i}(x) - \psi_{G,i}}{t_{si,i}}$$

$C_{1,i}(x) + 2C_{2,i}(x)t_{si,1} = \frac{-\eta_i\psi_{s,i}(x) - \psi_{G,i}}{t_{si,i}}$ but from Equation (4.5b) we have the value for $C_{1,i}(x)$.

$$\frac{\eta_i\psi_{s,i}(x) - \psi_{G,i}}{t_{si,i}} + 2C_{2,i}(x)t_{si,1} = \frac{-\eta_i\psi_{s,i}(x) - \psi_{G,i}}{t_{si,i}}$$

$$2C_{2,i}(x)t_{si,1} = \frac{-2\eta_i\psi_{s,i}(x) - \psi_{G,i}}{t_{si,i}}$$

$$2C_{2,i}(x) = \frac{-\eta_i\psi_{s,i}(x) - \psi_{G,i}}{t_{si,1}^2} \qquad (4.5c)$$

The above Equations (4.5a), (4.5b) and (4.5c) values are the coefficients for the potential at Regions 4, 5 and 6

Now we have to find these values for Regions 1, 2 and 3 by using Equations (4.4a) and (4.4d)

From (4.4a):

$$\psi_i\left(x, y = \frac{-t_{Ge,1} - t_{si,2}}{2}\right) = C_{o,i}(x) + C_{1,i}(x)\left(\frac{-t_{Ge,1} - t_{si,2}}{2}\right) + C_{2,i}(x)\left(\left(\frac{-t_{Ge,1} - t_{si,2}}{2}\right)^2\right) = \psi_{s,i}(x)$$

$$C_{o,i}(x) + C_{1,i}(x)\left(\frac{-t_{Ge,1} - t_{si,2}}{2}\right) + C_{2,i}(x)\left(\left(\frac{-t_{Ge,1} - t_{si,2}}{2}\right)^2\right) = \psi_{s,i}(x) \quad (4.5d)$$

From Equation (4.4b):

$$\psi_i\left(x, y=\frac{t_{si,1}+t_{si,2}}{2}\right)=C_{o,i}(x)+C_{1,i}(x)\left(\frac{t_{si,1}+t_{si,2}}{2}\right)+C_{2,i}(x)\left(\left(\frac{t_{si,1}+t_{si,2}}{2}\right)^2\right)=\psi_{si,i}(x)$$

$$C_{o,i}(x)+C_{1,i}(x)\left(\frac{t_{si,1}+t_{si,2}}{2}\right)+C_{2,i}(x)\left(\left(\frac{t_{si,1}+t_{si,2}}{2}\right)^2\right)=\psi_{si,i}(x) \quad (4.5e)$$

From Equation (4.4c):

$$\frac{d\psi_{s,i}(x)}{dy}\Big|y=\frac{-t_{Ge,1}-t_{si,2}}{2}=\frac{d}{dy}\left(C_{o,i}(x)+C_{1,i}(x).y+C_{2,i}(x).y^2\right)\Big|y=\frac{-t_{Ge,1}-t_{si,2}}{2}$$

$$=C_{1,i}(x)+2C_{2,i}(x).y\Big|y=\frac{-t_{Ge,1}-t_{si,2}}{2}=\frac{\eta_i\psi_{s,i}(x)-\psi_{G,i}}{t_{si,1}}$$

$$C_{1,i}(x)+2C_{2,i}(x)\left(\frac{-t_{Ge,1}-t_{si,2}}{2}\right)=\frac{\eta_i\psi_{s,i}(x)-\psi_{G,i}}{t_{si,1}} \quad (4.5f)$$

$$C_{1,i}(x)+2C_{2,i}(x)\left(\frac{t_{si,1}+t_{si,2}}{2}\right)=\frac{\eta_i\psi_{s,i}(x)-\psi_{G,i}}{t_{si,1}} \quad (4.5g)$$

By combining Equation (4.5d) to (4.5g) we get the values of coefficients for region 1 and 2 as follows:

$$C_{ox,i}(x)=\alpha_i^2\psi_{s,i}(x)-\beta_i\psi_{G,i} \quad (4.6a)$$

for region 1

$$C_{1,i}(x)=\frac{\eta_i(\psi_{s,i}(x)-\psi_{G,i})t_{Ge,2}}{t_{Ge,1}^2} \quad (4.6b)$$

$$C_{2,i}(x)=\frac{-\eta_i(\psi_{s,i}(x)-\psi_{G,i})}{t_{Ge,1}^2} \quad (4.6c)$$

for region 2 and 3

$$C_{1,i}(x)=\frac{\eta_i(\psi_{s,i}(x)-\psi_{G,i})t_{si,2}}{t_{si,1}^2}$$

$$C_{2,i}(x)=\frac{-\eta_i(\psi_{s,i}(x)-\psi_{G,i})}{t_{si,1}^2}$$

where $\alpha^2=1+\beta_i$ (4.7)

and

for region 1

$$\beta_i=\left(\frac{\eta_i}{2}\right)*\left(\frac{t_{si,2}}{t_{Ge,1}}\right)\left(1-\frac{t_{si,2}}{t_{Ge,1}}\right)+\left(\frac{\eta_i}{4}\right)*\left(1-\frac{t_{si,2}}{t_{Ge,1}}\right)^2 \quad (4.8a)$$

for region 2 and 3

$$\beta_i=\left(\frac{\eta_i}{2}\right)*\left(\frac{t_{si,2}}{t_{si,1}}\right)\left(1-\frac{t_{si,2}}{t_{si,1}}\right)+\left(\frac{\eta_i}{4}\right)*\left(1-\frac{t_{si,2}}{t_{si,1}}\right)^2 \quad (4.8b)$$

The values of coefficients from equation (4.6a) to (4.6c) are for region 1, 2 and 3 where i=1,2 ,3 in each formulas.

Now substitute the coefficients $C_{j,i}(x)$ into Equation (4.2), to obtain the electro static potential $\psi(x,y)$.Finally, a differential equation interms of the surface potential is obtained as follows.

$$\frac{d^2\psi_{s,i}(x)}{dx^2}\left(\alpha_i^2+\frac{\eta_i t_{si,2}y^2}{t_{Ge,1}^2}+\frac{\eta_i}{t_{Ge,1}}y^2\right)-\frac{2\eta_i\left(\psi_{s,i}(x)-\psi_{G,i}\right)}{t_{Ge,1}^2}=\frac{-qN_i}{\epsilon_{si}} \tag{4.9}$$

$$\frac{d^2\psi_{s,i}(x)}{dx^2}\left(\alpha_i^2+\frac{\eta_i t_{si,2}y^2}{t_{si,1}^2}+\frac{\eta_i}{t_{si,1}}y^2\right)-\frac{2\eta_i\left(\psi_{s,i}(x)-\psi_{G,i}\right)}{t_{si,1}^2}=\frac{-qN_i}{\epsilon_{si}} \tag{4.9a}$$

In region 1,2 and 3 the surface potential cannot be directly equated with the surface potential of the adjacent regions at the boundary. Instead, we consider a "pseudo" surface potential for the first two regions of y=0 and use that to form boundary conditions required for the solution of Equation (4.9c). Thus the "pseudo" surface potential based differential equation, obtained from Equation (4.9, 4.9a) by putting y=0, can be written as follows:

$$\alpha_i^2\frac{d^2\psi_{s,i}(x)}{dx^2}-\frac{2\eta_i\left(\psi_{s,i}(x)-\psi_{G,i}\right)}{t_{Ge,1}^2}=\frac{-qN_i}{\epsilon_{si}}-\frac{2\eta_i\psi_{G,i}}{t_{Ge,1}^2} \tag{4.9b}$$

$$\alpha_i^2\frac{d^2\psi_{s,i}(x)}{dx^2}-\frac{2\eta_i\left(\psi_{s,i}(x)-\psi_{G,i}\right)}{t_{si,1}^2}=\frac{-qN_i}{\epsilon_{si}}-\frac{2\eta_i\psi_{G,i}}{t_{si,1}^2} \tag{4.9d}$$

Now, for all regions the differential equations can be written as follows:

$$\frac{d^2\psi_{s,i}(x)}{dx^2}-\mathcal{K}_i^2\psi_{s,i}(x)=-\mathcal{K}_i^2\psi_{c,i} \tag{4.9c}$$

where, $\mathcal{K}_i=(\frac{2\eta_i}{t_{si,i}})^{1/2}\ for\ regions\ 4,5\ and\ 6,\quad \mathcal{K}_i=\frac{1}{\alpha_i}(\frac{2\eta_i}{t_{Ge,i}^2})^{1/2}$ for region 1, $\mathcal{K}_i=\frac{1}{\alpha_i}(\frac{2\eta_i}{t_{si,i}^2})^{1/2}$ for regions 2 and 3

$\frac{1}{\mathcal{K}_i}$ is the characteristics length or decay length of the surface potential in each region.

To term $\psi_{c,i}$ is region dependent, with the expression as follows for region 3 to 5

$$\psi_{c,i}=\psi_{G,i}+\frac{qN_i}{\epsilon_{si}\mathcal{K}_i^2} \tag{4.10a}$$

$$\psi_{c,i}=\psi_{G,i}+\frac{qN_i}{\alpha_i^2\mathcal{K}_i^2\ \epsilon_{si}} \tag{4.10b}$$

Finally, the solution for the differential Equation (4.9c) is as follows:

$$\psi_{si,i}(x)=A_i e^{-k_i(\chi-\Sigma x_i-1)}+B_i e^{k_i(\chi-\Sigma x_i-1)}+\psi_{c,i} \tag{4.10c}$$

where, $x_1=L_s$-dep, $x_2=L_1$, $x_3=L_2$, $x_4=L_3$ and $x_5=L_d$-dep.

5 CONCLUSION AND RECOMMENDATIONS

5.1 Conclusion

The thesis presents a comprehensive investigation into the development of high-performance, low-power Tunnel Field-Effect Transistors (TFETs) to address the growing demand for energy-efficient electronic devices. The research explores advanced source engineering techniques, including the exploration of double gate TFETs (DGTFETs), broken gate TFETs (BG-TFETs), and the introduction of a Germanium source in the BG-TFET (Ge-BG-TFET) structure. The culmination of this work is the novel Germanium-Source N+ Pocket broken gate TFET (Ge-S N^+ Pocket BG-TFET) design, which exhibits remarkable performance metrics, including an I_{ON} of 1.82×10^{-4}A/µm, I_{OFF} of 4.33×10^{-18} A/µm, an I_{ON}/I_{OFF} ratio of 4.21×10^{13}, a subthreshold slope (SS) of 29.19 mV/decade, and a threshold voltage (V_{th}) of 0.37534 V. The proposed Ge-S N^+ Pocket BG-TFET structure effectively overcomes the low ION challenge of traditional TFETs while maintaining low power operation, making it a promising candidate for future low-power electronic applications. The thesis also demonstrates the applicability of the TFET structure in biosensing, showcasing its versatility and potential in diverse scenarios. This comprehensive approach underscores the importance of source engineering, particularly material and doping engineering, in developing high-performance, low-power TFETs. The findings of this thesis contribute significantly to the advancement of low-power electronics, providing a robust framework for the design and simulation of next-generation TFETs. The innovative TFET structures and the insights gained from this research pave the way for the development of energy-efficient electronic devices, addressing the growing demand for sustainable and portable technologies in the digital era.

5.2 Recommendations

Future research could explore

- The use of other high-mobility materials beyond Germanium, such as III-V compounds (e.g., InAs, GaSb) or two-dimensional materials (e.g., MoS2, graphene), to further enhance the proposed TFET performance.
- Studying the impact of further scaling down the device dimensions, including gate length and pocket length, to determine the limits of miniaturization while maintaining optimal performance.
- Evaluate the integration of the novel TFET structures into complex circuits and systems, assessing their impact on overall circuit performance, power consumption, and speed.

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