Design and Optimization of Tunnel Field-Effect Transistor using Dielectric Engineering for Analog/RF Amplification

Ashebir Taresa Angesa

A Thesis Submitted to the Department of Electronics and Communication Engineering

School of Electrical Engineering and Computing

Presented in Partial Fulfillment of the Requirement for the Degree of Master's in Electronics and Communication Engineering

(Communication Engineering)

Office of Graduate Studies

Adama Science and Technology University

June, 2022

Adama, Ethiopia

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Co-Advisor: Dr. Dereje Tekilu

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DECLARATION

I hereby declare that this master thesis entitled "**Design and Optimization of Tunnel Field-Effect Transistors using Dielectric Engineering for Analog/RF Amplification**" is my work and has not been submitted to any university for a similar purpose. All sources of materials used for this thesis have been duly acknowledged through citation.

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We, the advisor(s) of this thesis, hereby certify that we have read the revised version of the thesis entitled "**Design and Optimization of Tunnel Field-Effect Transistors using Dielectric Engineering for Analog/RF Amplification,**" prepared under my guidance by Ashebir Taresa submitted in partial fulfillment of the requirements for the degree of masters of Science in Communication Engineering. Therefore, we recommend submitting a revised version of the thesis to the department following the applicable procedures.

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APPROVAL PAGE

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LIST OF ACRONYMS

2-D	Two Dimensional
3-D	Three Dimensional
BGN	Bandgap narrowing
BTBT	Band-to-band tunneling
C-D	Channel-drain junction
CMOS	Complementary Metal Oxide Semiconductors
DIBL	Drain-induced barrier lowering
DMG TFET	Dual Material Gate tunnel field-effect transistor
DP	Dielectric Pocket
EOT	Effective oxide thickness
FD-SOI	Fully doubleted SOI
FinFET	Fin fit FET
GAA	Gate-all-around
Ge	Germanium
IMOS	Ionization MOSFET
IC	Integrated Circuit
ITRS	International technology roadmap for semiconductor
JLTFET	Junction less Tunnelling Field Effect Transistor
GAA TFET	Gate all around TFET
GDO-TTFET	Gate-drain overlap T-shape TFET
GBP	Gain bandwidth product
HfO_2	Hafnium dioxide
HCE	Hot carrier effect
K	Dielectric constant
LPCVD	Low-pressure chemical vapor deposition

LTO	Low temperature oxide
L-TFET	L-shaped TFET
MOSFETs	Metal Oxide Semiconductor Field Effect Transistor
PD-SOI	Partially depleted SOI
PCVD	Plasma enhanced chemical vapor
RF	Radio Frequency
SCE	Short Channel Effect
Si	Silicon
SiGe	Silicon-germanium
SiO_2	Silicon dioxide
Si_3N_4	Silicon Nitrite
SOI	Silicon on Insulator
SRH	Shockley-Read-Hall
SS	Subthreshold Slope
TCAD	Technology Computer-Aided Design
TFETs	Tunnel Field-Effect Transistors
TTFET	T-shaped TFET
VWF	Virtual Wafer Fabrication

LIST OF SYMBOLS

C_{gd}	Gate-drain capacitances
C_{gs}	Gate-source capacitances
I_D	Drain current
E_g	Energy band-gap
f_T	Cut-off frequency
g_m	Transconductance
L_G	Channel length
L_D	Drain length
L_{DP}	Length of Dielectric Pocket
L_S	Source length
tox	Gate oxide thickness
Φ	Work function
V_{GS}	Gate to source voltage
T_{DP}	Thickness of Dielectric Pocket

ABSTRACT

This thesis presents the impact of dielectric pocket (dielectric engineering) on tunnel FET to mitigate the ambipolar current and improves the analog/RF performance of TFETs. It is observed that when a dielectric pocket is inserted into the drain region, it affects the channel-drain junction, and then the increase of tunneling barrier of the interface. In this work, various metrics are invoked in simulation by varying different parameters at the dielectric pocket, such as the dielectric material of the pocket, pocket thickness, and length of the pocket. Furthermore, by replacing three dielectric materials at DP (i.e., HfO_2, SiO_2, and Si_3N_4), a high k dielectric material (HfO_2) delivers a greater reduction in OFF-state current ($7.88x10^{-19}A/\mu m$) and ambipolar current ($1.22x10^{-17}A/\mu m$). Additionally, when comparing conventional TFETs with DP-TFETs (proposed study) for the negative gate voltages (i.e., ambipolar current), the value of I_{AMB} is suppressed from $9.38\times10^{-7}A/\mu m$ to $1.22\times10^{-17}A/\mu m$, thus the ambipolar current is reduced by ten (10) orders of magnitude without decreasing (affecting) ON-state current performance. However, the analog/RF parameter of DP-TFETs with low dielectric material (SiO_2) is much better than that of high k dielectric (HfO_2) and medium K dielectric material (Si_3N_4) and has a peak g_m of 2.7×10^{-6} S/µm, a gain-bandwidth product of 0.3GHz, and a cut-off frequency of 0.23 GHz. All the simulations are done in the Atlas Module of the SILVACO TCAD tool. It is considered the Kane tunneling model in all the simulations. Finally, to show the practical applicability of the DP-TFETs, the inverter analysis of DP-TFET is investigated.

Keywords: Ambipolar conduction; ON-state current; Gain-bandwidth product; Cut-off frequency; Dielectric pocket (DP); TFET; Technology Computer-Aided Design Simulation (TCAD).

CHAPTER ONE

INTRODUCTION

1.1. Motivation

A transistor's essential function is to regulate a current over several orders of magnitude using a regulating voltage (Lai, 2009). Because of this concept, transistors of several varieties are among the most significant components of essentially all electrical equipment. Every CPU in modern computers and smartphones is made up of billions of transistors, but transistors are also required in smaller numbers in analog/RF, sensors, audio, wireless communication amplifiers, and power supply controllers (Maria Jossy & Vigneswaran, 2014). Since its invention in the 1960s, the tunnel field-effect transistor (TFETs) rapid development has been powered mainly by the constant lowering of device size and the occasional introduction of new materials or changes in device design (Riordan et al., 1999). Device structure scaling is reaching fundamental physical limitations as feature sizes have decreased to the thickness of only a few atomic layers. New materials, new architectures, and new physical operating principles have thus become the focus of research efforts since the beginning of the twenty-first century to increase device performance in terms of energy efficiency and speed.

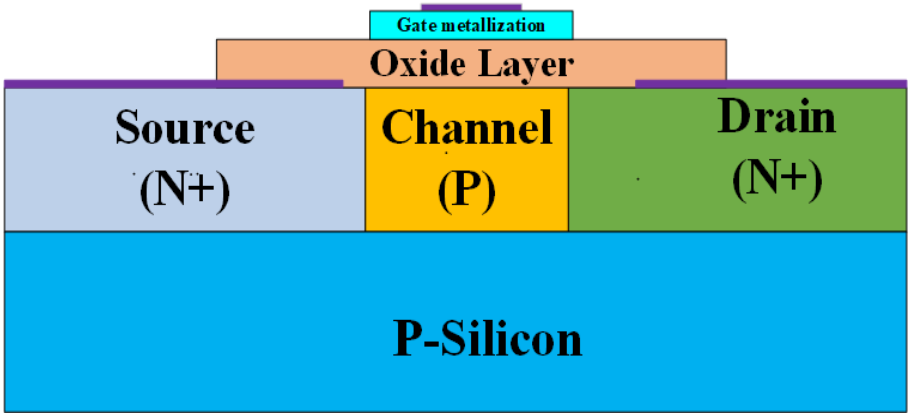
This chapter begins with an overview of TFETs device structure and operation, TFETs applications, TFETs properties, as well as justification of the study, the problem statement, objectives of the study, significance of the study, scope of the study, and our contribution in this study.

1.2. Introduction to Structure and Operating Principle of n-TFETs

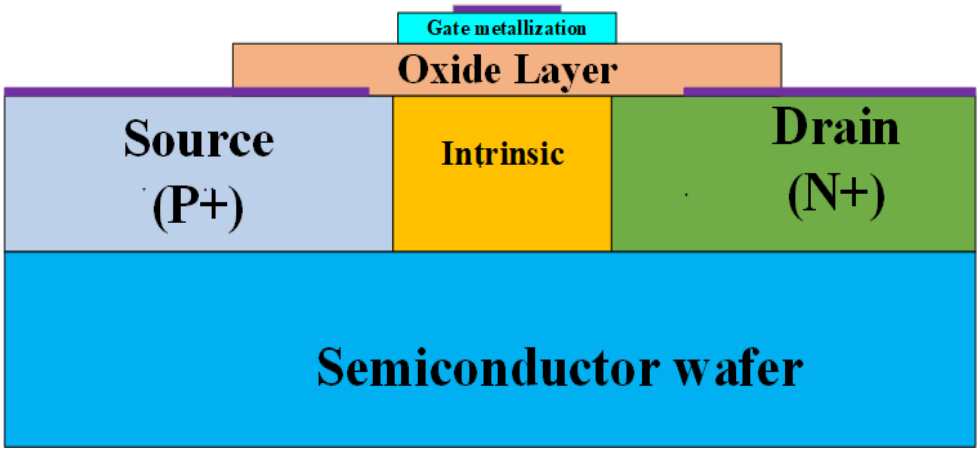
1.2.1. Tunnel Field-Effect Transistors -TFETs

This section will look at the basic structure of a TFET and the operating principle of TFETs. Tunnel field-effect transistors are unipolar transistors that work based on the voltage-controlled current device concept (Satish M. Turkane & Kureshi, 2016). They are devices in which the action of voltage (an electric field) at a third terminal called the electrode gate, which has a thin metal oxide layer between the semiconductor and the metal, and current control between two electrodes drain and source is controlled by the third terminal (gate). The positive voltage at the gate region for n-TFETs causes a negative charge to accumulate

at the oxide-silicon interface, forming a channel for current conduction. The channel connects the path between both the source and the drain regions. Furthermore, the third terminal electrode is usually heavily doped metal work function and is isolated by a thin gate oxide from the silicon channel. To further understand the working principle of n-TFETs, it is helpful to compare them to MOSFETs. The device structure of MOSFETs and TFET are shown in Figure 1.1. This device structure is made of single gate architecture with a gate length dimension of 40 nm, the thickness of gate oxide (SiO_2) is 3 nm, and a substrate (body) thickness of 8 nm is described here for demonstrative purposes only.



(a)



(b)

Figure 1.1: Device stricture of (a) MOSFETs and (b)TFETs

In Figure 1.1, the structure of n-TFETs is compared to that of MOSFET. The basic structure of n-channel field-effect transistors (n-TFETs) is shown in Figure 1.1(b), and the device contains four regions with terminals designated as the source, gate, drain, and substrate (body). Figure 1.1(b) illustrates that TFETs have P-I-N diode and doped regions as the source, channel, and drain, operating under reverse bias conditions (Saxena et al., 2019).

MOSFETs have N-P-N diode and doped regions as the source, channel, and drain. Additionally, in MOSFETs, the carrier injection mechanism is based on thermal injection (Satyanarayana & Prakash, 2021), but TFETs utilize band to band tunnelling (BTBT) as a source carrier injection mechanism. Also, TFETs differ from MOSFETs structure is in TFETs that the drain region and the source region are doped with different types of dopants (i.e., the source region doped in a MOSFET is N-type concentration, whereas it is P-type concentration in the TFET) and the steep slope current-voltage characteristics are achieved using a band-to-band tunneling mechanism through a reverse-biased junction (Koswatta et al., 2009). This is the significant difference between MOSFETs and TFETs.

1.2.2. The Basic properties of TFETs

High input impedance, capable of power gain 3/4 terminal devices (i.e., source, gate, drain, and body or substrate), unipolar device, two device types: depletion mode and enhancement mode, two-channel types: P-channel and N-channel

1.2.3 Applications of TFETs

Microprocessor**,** power devices**,** memories**,** analog/RF circuit.

1.2.4. Qualitative Behaviour (Transfer Characteristics)

The current flow through the device under various biased conditions-describe in its behavior. The most important characteristics of a transistor are its transfer characteristics (Krishna K. Bhuwalka et al., 2006). These characteristic transfer parameters are schemes of the drain current (I_D) in the transistor regarding the gate voltage and the drain bias (I_D-V_G). This behavior of TFETs and the effect of biasing on the drain current of a TFET are observed by the band diagram of TFETs under various biasing conditions are described.

OFF-State

In the OFF-state (V_{GS}=0, V_{DS}>0), charge carriers present in the conduction band of the channel would tend to drift to the drain and thus generate a current (Dutta et al., 2020). However, because the source is p-type, the conduction band contains relatively few electrons, which can inject very few electrons into the channel. This leads to an insignificant OFF-state current (Maria Jossy & Vigneswaran, 2014). Due to the MOSFET principle on thermionic emission, a few of these electrons will be injected into the channel over the potential barrier at the source-channel interface. When a MOSFET is compared to a TFET, the OFF-state leakage current in MOSFET is high, limiting the device's performance.

ON-State

In the ON-state current (V_{GS}>0, V_{DS}>0), current flow in the device and charge carriers (electrons) are injected into the conduction band of the channel (S. Wang et al., 2017). In TFETs, there are insignificant free electrons in the conduction band of the p-type source region, and these charge carriers create from the valance band of the source region. The energy bands in the channel vary with regard to the source as the gate voltage (V_{GS}) is increased. At the positive value of the gate voltage, the valance band in the source region aligns with the conduction band in the channel. In the OFF-state of the device, the electron in the valence band of the source had no available energy state in the channel to the tunnel. The valence band of the source has been determined, the conduction band of the channel, the electron can tunnel into the latter through the potential barrier formed by the band-gap. The gate voltage at which this arrangement of the source valance band and the channel conduction band occurs is the start of the ON-state of the TFET (Sahay & Kumar, 2015).

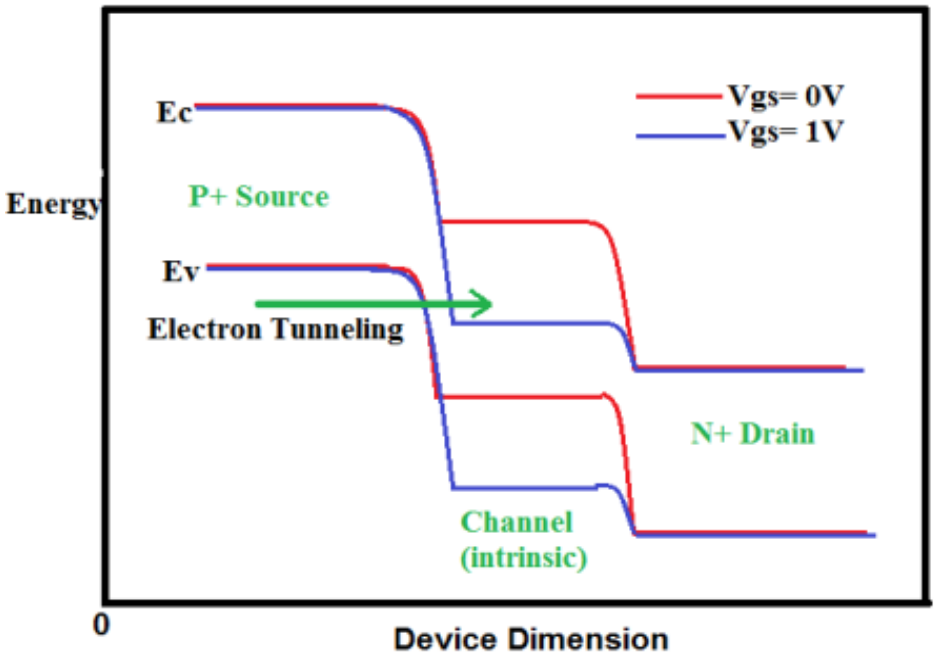


Figure 1.2: Energy band diagram of TFETs where the blue line indicates ON-condition and red lines OFF-condition (Satish M. Turkane & Kureshi, 2016)

In Figure 1.2, the gate voltage carriers tunnel into the channel through the potential barrier in the ON-state of TFETs, using the band to band tunneling operating principle (BTBT).

The channel barrier is high in the OFF-state of a TFET, so there is no current flow. Because of the thermal distribution of carriers, practicality is not zero, but only leakage current flows between the source and drain region.

Ambipolar behavior

A positive gate voltage was applied in the ON-state with the drain voltage $V_{DS}>0$ (Dutta et al., 2019). Here, let's discuss the behavior of a TFET when a negative gate voltage ($V_{GS}<0$) is applied (Satish M. Turkane & Kureshi, 2016). As $V_{GS}=0$, no electron can tunnel from the source valance band to the channel conduction band; as the gate voltage is reduced below 0V ($V_{GS}<0$), the energy band of the channel travels upward through to the source region. When the channel valence band aligns with the drain conduction band, an electron from the channel valence band can tunnel into the drain conduction band, resulting in current flow (Dutta et al., 2021).

The drain current increases significantly as the negative gate bias is increased, further due to (i) reduction of the tunneling length at the channel-drain junction and (ii) an increase in the number of states in the channel valence band from where an electron can tunnel to the conduction band of the drain (Sahay & Kumar, 2015). This is called ambipolar conduction.

Band Diagram

The current conduction mechanism in MOSFETs is thermal carrier injection (over the barrier), while the current conduction mechanism in TFETs is band-to-band tunneling (through the barrier). Electrons tunnel from the source valence band to the drain conduction band in an N-TFET (P-TFET, holes from the source conduction band to the drain valence band) (Li et al., 2018). Changing the gate potential controls the BTBT probability (consequently, the current).

The conduction and valence band energies of MOSFETs and n-TFETs are shown in figure 1.3. The source-side p-n junction barrier limits conduction in MOSFETs in the OFF state ($V_{GS}=0V$, $V_{DS}>1$ V), limiting thermionic carrier emission, but in the ON state current ($V_{GS}>V_{DS}>0V$), the source barrier is insignificant, allowing thermionic carrier emission. The transmission probability of TFETs in the OFF state is low due to the wide source to channel tunnel junction barrier (Low Electric Field), resulting in very low OFF currents. In the ON-state, the tunnel barrier thickness allows carriers to tunnel through into the channel (Koswatta et al., 2009). The BTBT producing mechanism in TFETs improves subthreshold swing by less than 60mV/dec (Park et al., 2018), which means by reducing the device's size, the circuit speeds are also improved by a subthreshold swing. In addition, the most attractive result of scaling is that the subthreshold swing reduces the power dissipation or increases power consumption (energy efficiency).

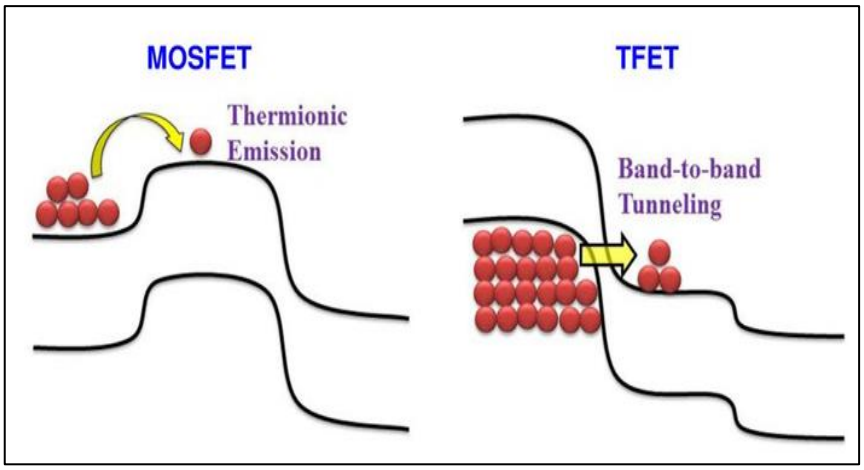


Figure 1.3: Device principle of the MOSFETs and TFETs (Mohankumar et al., 2009)

1.2.5. Analog/RF parameters

The analog/RF amplification analyze by different or various parameters (Q. Wang et al., 2017), such as transconductance (g_m), cut-off frequency (f_T), gate-to-drain capacitance (C_{gd}), gate-to-source capacitance (C_{gs}), and gain-bandwidth product (GBP). Among these, a critical parameter transconductance (g_m) has been investigated for achieving a high cut-off frequency (f_T), and better gain-bandwidth product. The parameter transconductance (g_m) is the transformation of gate-to-source voltage (V_{GS}) to drain current (I_D) and is well-defined by a modification in the drain current when the unit change in gate-to-source voltage occurs (Xu et al., 2009). Transconductance is expressed in equation (1.1).

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \tag{1.1}$$

The other important parameter for amplification achievement in analog/RF analysis is the frequency at which the short-circuit current gain of the device falls to unity (Chen et al., 2018), which is expressed in the equation (1.2).

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{1.2}$$

Whereas, g_m is the transconductance, C_{gs} and C_{gd} are the gate-source and gate-drain parasitic capacitances, respectively (Q. Wang et al., 2017). The other significant characteristic of the amplifiers for a suitable method is the higher bandwidth product. Gain bandwidth product (GBP) is a parameter that expresses how much the amplifier can amplify the high frequency and low frequency of message signals, which influences the frequency selectivity in device applications; it is calculated by equation (1.3).

$$GBP = \frac{g_m}{2\pi\left(C_{gd}\right)} \tag{1.3}$$

Whereas, g_m is the transconductance, C_{gd} is the gate-to-drain capacitance. Furthermore, optimization is required to trade DC characteristics and analog/RF parameters in terms of the structure length of the region profile with a different doping concentration and sectional dimensions of the work function (φ) and dielectric engineering (Raad et al., 2017).

1.3. Justification of the Study

Nowadays growth of modern technologies is rapidly developing. To this growth, device structure scaling plays a basic and essential role. Microelectronics developed into nanoelectronics to keep up with Moore's law prediction. Scaling down is primarily used to achieve higher chip density, lower power consumption, better amplification improvement, improved analog/RF performance parameters. Simultaneously, MOSFET scaling introduced several issues, including short-channel effects, high I_{OFF} leakage current, drain-induced barrier lowering (DIBL), and parasitic capacitance (C_{GD} and C_{GS}) (Liu et al., 2016), which degraded the device's performance.

Furthermore, the subthreshold slope of a MOSFET is greater than 60mV per dec at room temperature is physically limited (Liu Suman Datta, 2015). So, MOSFET replacement is becoming increasingly necessary, and in recent years, hundreds of FET-based devices have been studied. Out of them, tunnel field-effect transistors (TFETs) show its strong candidature to substitute conventional and alternative variants of the MOSFET. TFETs are having good subthreshold slope than MOSFETs. The subthreshold slope shows a fast transition among the device's ON and OFF state currents. Tunneling field-effect transistors (TFET) have received much attention as a capable candidate for analog/RF amplification due to their steeper switching behavior than MOSFET (S M Turkane et al., 2016). However, TFETs have different issues like low ON-current, leakage current, large ambipolar current, and poor analog/RF performance, which necessitate further optimization for low-power and high-frequency applications (Q. Wang et al., 2017).

To decrease the ambipolar current and improve the poor analog/RF performance, the TFET uses dielectric engineering to overcome these tunnel field-effect transistors issues. Low drain doping concentration was previously an effective method for reducing TFET's ambipolar current (Abdi & Kumar, 2014). However, low drain doping concentration increased contact

resistance and poor current driveability. In tunnel FET optimization, a lightly doped drain combined with dielectric engineering has been done to decrease the bottleneck issue of TFET. Furthermore, using dielectric engineering with a lightly-doping drain sideways can suppress ambipolarity and improve the analog/RF figures of merit, whereas utilizing high doping at the source region to improve gate control leads to better I_{ON} current. In TFETs, device performance can be improved by reducing the dimension of the transistor and reducing the short channel effect (SCE) (Liu et al., 2016). Therefore, there is a need to evaluate the performance with dimension scaling and device parameters (Tayal et al., 2021). Moreover, this work study aims to provide a systematic investigation of various parameters of TFET, which is helpful for analog/RF amplification.

1.4. Statement of Problems

The term "scaling" refers to preserving the magnitude of the device's internal electric field although reducing the size or area of tunnel field effect transistors (TFET) by a factor of subthreshold swing (SS) (Krishna K. Bhuwalka et al., 2005). By reducing the device's size, the circuit speeds are also improved by a subthreshold swing. In addition, the most attractive result of scaling is that the subthreshold swing reduces the power dissipation. This tendency of the downscaling device structure, on the other hand, create various issues and fundamental physical limitations. These effects arise due to the velocity saturation, wider tunneling width of the source-to-channel junction, narrow tunnelling width at channel-to-drain junction, the quantum effect, and the high-field effect (Fahad et al.,2011).

For CMOS technology and analog/RF performance, the efficiency of the transistor is mainly determined by the ON-state current (I_{ON}) and OFF-state (I_{OFF}) (Kouhalvandi et al., 2021). However, the scaling technology faces increased I_{OFF} (leakage current issue) due to drain-induced barrier lowering (DIBL) and gate tunneling. On the other hand, the ON-state current does not increase sufficiently (lower I_{ON}) due to insufficient band-band tunneling (BTBT) carrier conduction mechanism being limited by a large material band-gap, dielectric gate thickness, and low K-dielectric material (Kouhalvandi et al.,2021). Low I_{ON} means a small transconductance value, which limit the cut-off frequency and gain-bandwidth product (Q.Wang et al., 2017). Therefore, the optimization technique to increase the ON-state current of TFETs has been studied further in our work, and it can be solved using reducing body thickness and oxide thickness, gate metal work-function, heavy doping at the source region, and high k-dielectric at gate oxide.

TFETs also face other issues due to their ambipolar conduction (I_{AMB}), and higher miller capacitances (gate-to-source and gate-to-drain capacitances) (Chen et al.,2018). Ambipolar conduction are significant problems in tunnel FET (S.Wang et al.,2017), and decrease the performance of the devices (Das et al.,2018). Therefore, to overcome these problems in the TFETs, TFETs optimization has been providing a lightly doped drain side, increased oxide thickness at the channel-drain junction, gate work-function, and dielectric engineering. This means ambipolar current (I_{AMB}) is suppressed by producing a low electric field at the drain-channel junction (i.e., increasing the tunneling barrier width at the drain-channel junction).

Analog/RF merit figures can be defined based on different parameters (Poorvasha et al., 2017), such as frequency of unity gain (f_T), transconductance (g_m), and gain-bandwidth product (GBP). Among these, transconductance is an important parameter and plays an essential role in achieving a higher cut-off frequency and a higher gain-bandwidth product A high value of transconductance and gain-bandwidth product ensures better amplification and is preferred for analog and RF performance. Another critical investigation of TFETs performance for higher frequency or checking the analog/RF performance parameter of a device is cut-off frequency. The cut-off frequency mainly depends on transconductance and parasitic capacitance (Pandey et al., 2021).

Furthermore, the parasitic capacitances (Pandey et al., 2021) must be small to achieve higher frequency characteristics such as cut-off frequency and gain-bandwidth product for fulfilling desired analog and radio-frequency requirements (Ahish et al., 2016). Generally, ambipolar conduction, high leakage current, lower I_{ON} current, transconductance (g_m), cut-off frequency, gain-bandwidth product, and higher parasitic capacitance are problems of TFETs (particularly in analog/RF amplification) and a significant concern of TFETs.

1.5. Objectives of the Study

1.5.1. General Objective

This study aims to design and optimize tunnel field-effect transistors using dielectric engineering for analog/RF amplification.

1.5.2. Specific Objectives

To accomplish this study, it is further divided into the followings sub-objectives:

- To design and simulate the tunnel field-effect transistor (TFET) structure.

- ❖ To optimize transconductance, gate capacitances, cut-off frequency, and gain-bandwidth product (GBP). In other words, to improve analog/RF performance parameters.
- ❖ To achieve the high ON-state current (I_{ON}), highest I_{ON}/I_{OFF} rate, low $I_{OFF,}$ lowest subthreshold slope, and ambipolar conduction,
- ❖ To improve the rate of BTBT generation mechanism at the source-channel junction (decrease the tunneling barrier thickness).
- ❖ To utilize the proposed device in the circuit based and analyze the results.

1.6. Significance of the Study

A tunnel FET (TFET) has been attractive as a substitutable device for a low power application considering it may achieve a subthreshold slope much less than 60 mV/decade at room temperature (Krishna Kumar Bhuwalka et al., 2005), which permits TFET to be operated with the decreased supply voltage retaining a high ON-state current to OFF state current ratio (I_{ON}/I_{OFF}) (A. Garg et al., 2020). Moreover, those devices are appropriate for a low-power operation that might be functioning at high frequencies and different tunnel FET applications consist of low-power precise analogy ICs (included circuits). Generally, this tunnel field-effect transistor (DP-TFETs) study is vital for VLSI or CMOS technology to achieve: compact size (small size), high speed (fast switching), power consumption (energy efficiency), and high bandwidth.

1.7. Scope and Limitation of the Study

1.7.1. Scope of the Study

This thesis investigates the DC transfer characteristics performance and analog/RF parameters, which help for low power operation and high-frequency applications of DP-TFETs under 45nm channel length. All of the devices in this study have been realized and analyzed using the Silvaco Atlas TCAD simulator. For channel length under 45nm, all the device structure parameters are set according to the international technology road map for semiconductor (ITRS) road map. In the case of the TFETs with dielectric pockets, the optimization of the thickness, length of DP, and dielectric of DP are illustrated with detailed simulation results. DC transfer characteristics parameters like the ON-state, OFF-state current, ambipolar conduction, electron concentration, and electric field of all the devices have been investigated and compared with conventional TFET.

For analog/RF performance, parameters such as the transconductance, cut-off frequency, and gain-bandwidth product have been explored.

1.7.2. Limitations of the Study

The study came across the following limitation throughout the research process: the dielectric pocket's impact at the source-channel junction will not be discussed, and also there are a limitation in the fabrication of the device.

1.8. Contributions

This thesis aims to optimize TFETs using dielectric engineering for analog/RF amplification and analyze the comparison with DP and without DP (conventional TFETs) device structure. However, some of the differences between the related work and the proposed study are underlined in the following points.

- Insertion or addition DP at the drain side for better performance of the device.
- Substituted low-dielectric (SiO_2) by high k-dielectric (HfO_2) at gate oxide.
- The lowest value of ambipolar current without variation of ON-state current.
- Performing device simulations
- Analysis of analog/RF parameters.
- Analysis output of DC characteristics like
    - Electric field (at horizontal and vertical direction),
    - Electron concentration and electron BTBT generation,

1.9. Organization of the Thesis

This thesis deals with designing and optimizing tunnel field-effect transistors using dielectric engineering for analog/RF amplification for partial fulfillment of the master program. This section of the thesis indicates the thesis's ways, steps, and progress. It includes the methodology, device structure, circuit-based simulation, scope, the research limitation of the study, results, and discussion of the study. This thesis is organized into five chapters as follows:

The first chapter**, chapter 1,** has provided the introduction part of the study; the problem statement, objectives of the study, significance, scope, contribution, and limitations.

In next chapter, **Chapter 2**, will discuss the review of the existing literature and differences related to tunnel field-effect transistors such as heterojunction source, a high-k gate dielectric

material, double gate architecture, Si/Ge source TFETs, a low-bandgap material in the tunneling region, gate overlapped TFETs (vertical tunneling TFETs), dielectric pocket, extended source/drain TFETs.

Chapter 3 discusses the study's simulation methodology and device structure. It will discuss the design methodology, simulation flow chart, simulation model, inverter circuit design, device structure, and description parameters of DP-TFETs (proposed study) and conventional TFETs.

Chapter 4 describes the result and discussion for a dielectric pocket tunnel field-effect transistor (DP-TFET) with a comparison of conventional TFETs by varying different parameters such as variation of various parameters such as dielectric material variation, thickness or thickness of DP (TDP) variation, length of DP (L_{DP}) and with a comparison of conventional TFETs. Additionally, the analog/RF parameters like cut-off frequency, gain-bandwidth product, gate-to-source/drain capacitances, and transconductance result.

Finally, provides conclusions and some recommendations for future work.

CHAPTER TWO

LITERATURE REVIEW

2.1. Background of the study

The revolution in integrated circuit technology has led to a new era in electronics with great computational capabilities and computing power. Over the past decades, the electronics community's research and development have resulted in the continued miniaturization of the conventional MOSFETs device dimensions, leading to higher circuit density and higher functionality at a reduced cost (Koswatta et al., 2009). Gordon Moore (Intel co-founder) predicted that over the history of computing hardware, semiconductor chips would become two times more powerful every two years, and they would eventually be so small that they could be embedded in memory, computers, and smartphones (Liu Suman Datta, 2015).

The predictions of Moore proved to be accurate for several decades and guided/motivated the semiconductor industry to use them as benchmarks to set the goals for development and research. However, the performance of MOSFETs is limited due to different scaling issues, such as drain-induced barrier lowering, short channel effects, velocity saturation, etc. To scale down a MOSFET, the device's channel length and oxide thickness decrease while substrate doping increases (Dennard scalability). However, the channel length and oxide thickness scaling technology face increasing I_{OFF} (leakage current) due to drain-induced barrier lowering and gate tunneling. Moreover, the I_{ON} current does not increase sufficiently due to lower carrier mobility at source-channel junction. In addition, as technology advances and the number of transistors per unit chip area (size) increases, the leakage power (leakage current) also increases.

In order to solve these issues, the device architectures like fully depleted SOI (FD-SOI, partially depleted PD-SOI) and FinFET are studied in sub-micron technology nodes (Kouhalvandi et al., 2021) (Zhang, 2020). The device structures are designed to improve the system's electrostatics. These device architectures provide better gate control on the channel, as the gate surrounds the channel from multiple sides (Kuamr et al., 2016). Device thickness is scaled-down in these devices without increasing subsurface leakage paths, and, hence, unwanted leakage currents are suppressed. The mobility is also improved because of the undoped body, eliminating surface roughness scattering (Ahmed & Singh Sohal, 2017). So, to adjust the threshold voltage, channel doping is not used as a parameter in these structures.

Random dopant fluctuations, which are a significant source of process variability in bulk MOSFETs, are thus reduced (Chen et al., 2018).

FinFET is another novel device architecture for MOSFET scaling issues (Zhang, 2020). It has a thin-body non-planar MOSFET constructed on silicon-on-insulator (SOI) or bulk substrate, using patterning and etching technologies. In FinFET, the subthreshold swing (SS) improved (i.e., close to 60 mV/decade at room temperature), and short channel effect (SCE) can optimize the fin size. Massive scaling of FinFET is identified as a device that maintains better AC performance and high switching rates when compared with MOSFETs (Chen et al., 2018). FinFET provides an opportunity for researchers in other devices due to the fabrication difficulty. Gate all around FETs (GAAFETs) are also widely explored. They provide great electrostatic control. However, the stacked-FET technology involves fabrication complexities, like forming a high aspect ratio fin structure (Mohankumar et al., 2009). The devices on some new transport phenomena explored to replace conventional MOSFETs. An Impact ionization MOSFET (IMOS) and tunnel field-effect transistor (TFET) (Rajan et al., 2021) are some of the devices that use new phenomena, impact ionization, and band to band tunneling, respectively, for carrier transport. TFETs have been widely researched for low-power VLSI devices because of their exceptional leakage power performance and low OFF current. IMOS suffers from the high voltage requirement required for impact ionization (Kuamr et al., 2016).

The limitations of TFETs are their I_{ON} compared to ITRS requirements and the stringent fabrication steps necessary for extracting performance. Tunneling occurs in the lateral direction from the source to the channel in a conventional lateral TFET. Point to point (P-P) lateral tunneling refers to this type of tunneling. However, the BTBT can be started vertically and from the bulk to the surface if sufficient gate to source overlap is provided. Line tunneling or vertical tunneling (Abdi & Kumar, 2014) are terms used to describe this type of tunneling. Doping optimization (retrograde doping, pocket implant source (Raad et al., 2017), etc.): The BTBT takes place in limited nanometres alongside the source/body junction. This BTBT is a significant necessity of the energy band steepness, which the device's doping profile can control. In TFETs, an n+ pocket implant near the source is typically used to increase the ON current. However, the OFF current increases significantly because the SRH electric field enhances recombination. Generally, to solve the MOSFETs and conventional TFETs issues, recent literature has proposed tunnel field-effect transistors (TFETs). Tunnel field-effect transistors (TFETs) have a low subthreshold slope, are rare,

and are being investigated for various low-power applications. Tunneling from the source's valence band to the channel's conduction band occurs in a gated control PIN diode and the gate voltage controls (Saxena et al., 2019). The gate voltages modulate the tunneling barrier thickness at the source/channel junction. Esaki observed the tunneling mechanism in the Tunnel diode in 1960 (Jurczak et al., 2000). TFETs can operate at a much lower voltage than MOSFETs and, hence, consume less power than MOSFETs (Rajan et al., 2021). When compared MOSFET with TFET, TFETs advantages are low sub-threshold current, which leads to low leakage per device, and its moderate I_{ON}/I_{OFF} ratio can be suitable for analog/RF applications.

2.2 Related Works/shortcoming of TFETs

The main challenges in TFETs are the low ON-state current (I_{ON}), leakage current (I_{OFF}), and ambipolar conduction, which reduce the performance of devices. Because when TFETs have a low ON current and ambipolar behavior, there is more delay in the circuits (Abdi & Kumar, 2014). Due to this, many studies low sub-threshold current leads to low leakage per device, and the TFET's high I_{ON}/I_{OFF} ratio makes it suited for analog/RF applications have been published in recent years to improve the TFET's performance, and although the majority of researchers have focused on TFETs for low-power switching applications. Therefore, many efforts are being made around the world to suppress ambipolar conduction and improve $I_{ON,}$ including the: heterojunction source (Pindoo et al., 2021), a high-k gate dielectric (Rahi et al., 2017), a double-gate architecture (S. Wang et al., 2017), Ge source TFETs (S. Wang et al., 2017), a low-bandgap material in the tunneling region (Satyanarayana & Prakash, 2021), gate overlapped TFETs (Vertical tunneling TFETs) (Chen et al., 2018), pocket doped double gate structure (Raad et al., 2017), extended source TFETs (Dutta et al., 2021), and L-shaped TFETs (Li et al., 2018) have been used to improve ON-state current.

All the methods mentioned above significantly improve the drive capability of the TFETS, but on the other hand, the ambipolar current and leakage current are not enhanced; it is a bottleneck of TFETs due to which the analog/RF performance of the TFETs is degraded. For low-power switching and analog/RF circuits, low subthreshold swing (SS), low ambipolar conduction (leakage current), and a high ON-state current (I_{ON}) to OFF current (I_{OFF}) ratio are all desirable performance characteristics, including a gain-bandwidth product (GBP), transconductance (g_m) and high cut-off frequency parameters (f_T) (Li et al., 2018).

Researchers have documented various efforts in the literature to improve the TFETs parameters. Furthermore, in this section, it is realized that many novel innovations which are incorporated into the TFET device structures.

Approach to suppress ambipolar conduction in Tunnel FET using dielectric pocket studied in (Pandey et al., 2019). A dielectric pocket single gate tunnel field-effect transistor (DP-SG-TFET) structure is developed in this study to minimize ambipolar conduction in tunnel field-effect transistor devices. The dielectric pocket structure of single gate tunnel field-effect transistors improves system performance and prevents ambipolar conduction. The researcher focuses on the DP SG-TFET and L_{OL} structures, which use a 50 nm channel length and a high-K at dielectric pocket (DP) to reduce ambipolar conduction at the channel-drain junction without changing the ON-state current. Researchers have found that using gate-drain overlap (L_{OL}), ambipolar current (I_{AMB}) in TFET devices decreases. However, the added gate-drain overlap increases the distance that is required, which wastes the silicon area and increases the cost of fabrication (Pandey et al., 2019).

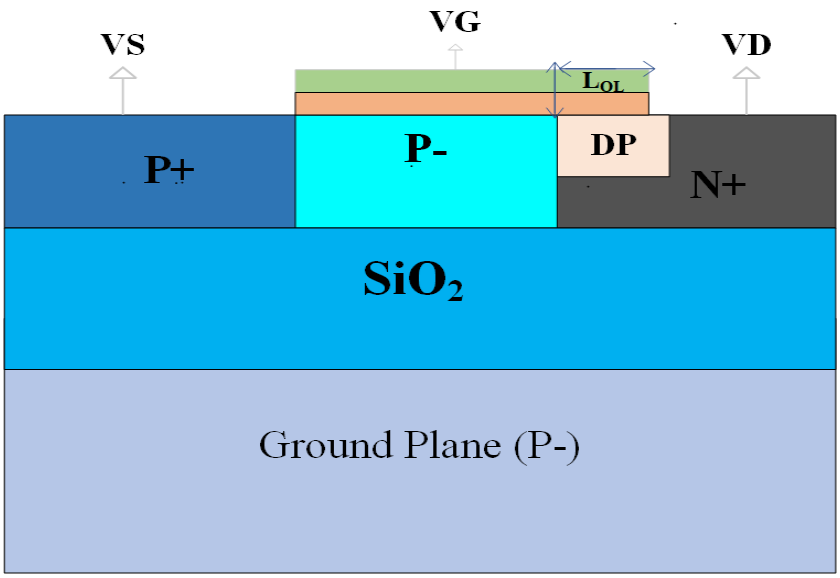


Figure 2.1: Cross-sectional view of SG-TFETs

Performance analysis of drain pocket hetero gate dielectric DG-TFET: Solution for ambipolar conduction and enhanced drive current has been examined in (Goyal et al., 2022). The effect of the drain pocket and heterogeneous gate dielectric (HD) on the performance of double gate tunnel field-effect transistors were investigated in this work (DGTFET). By suppressing BTBT at the channel-DP junction, the researcher noticed that an area and concentration optimized drain pocket near the drain region lowered ambipolar conduction to 7.210^{-15} A/µm. Furthermore, the presence of Al_2O_3 as a heterogeneous dielectric on the

source region (side) causes charge production, resulting in a steeper source-channel junction. Compared to the conventional counterpart, using Al_2O_3 as HD improved I_{ON} to an order of 10^{-5} A/m while avoiding a rise in I_{OFF}, increasing the I_{ON}/I_{OFF} ratio to 10^{11} (Goyal et al., 2022). The ambipolar current and I_{ON} are enhanced by utilizing the above method; however, the drain-gate overlap (DG_{OL}) increases capacitances, limiting the TFET performances at high frequencies. Similarly, a multi-gate structure or reduced channel thickness (lesser channel thickness leads to a larger BTBT rate) does not affect the performance of the hetero dielectric structure.

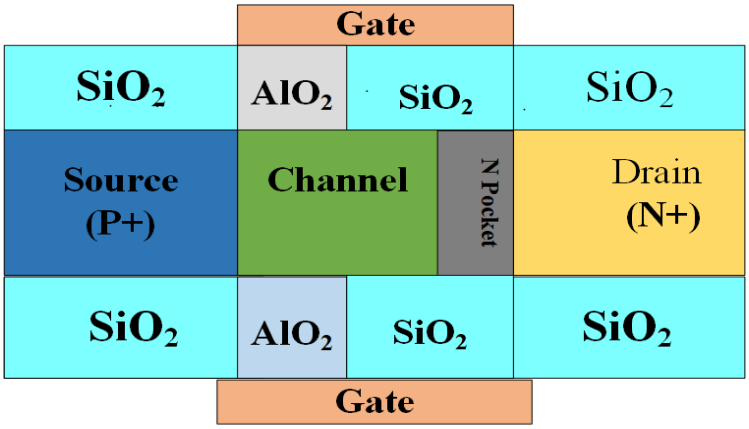


Figure 2.2: Schematic view of DP-HD-DGTFET

A non-uniform silicon TFET design with dual-material source and compressed drain has been studied in (J. Talukdar & Mummaneni, 2020). This study introduced a non-uniform channel TFET structure with a double-material source and compressed drain. This device results show that the suggested structure has a minimum point of SS (subthreshold slope) for gate voltages.

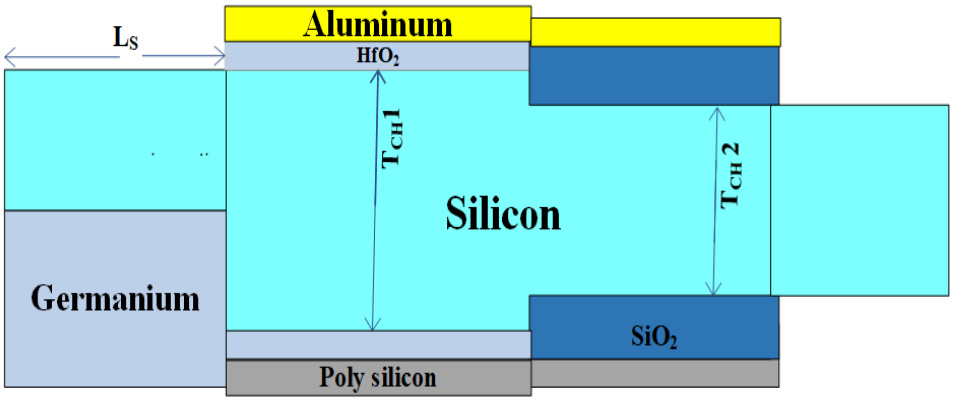


Figure 2.3: Schematic view of non-uniform silicon TFET

Furthermore, the ambipolar current is 10^{-14} A/µm, I_{ON} current is 10^{-5} A/µm, I_{OFF} values 10^{-16} A/µm and an I_{ON}/I_{OFF} ratio around 10^{11}. In this study, the effects of trap charge at the oxide/semiconductor interface have been studied for various trap charge distributions. (J. Talukdar & Mummaneni, 2020). However, gate-to-drain capacitance increases because of the trap charge dispersion at the oxide-semiconductor junction, leading to poor analog/RF performance (i.e., limiting the cut-off frequency).

Suppression of ambipolar current in tunnel FETs using drain-pocket has been studied in (S. Garg & Saurabh, 2018). The effect of a drain pocket (DP) close to the drain region in TFETs on suppressing the ambipolar current is investigated. Even when the TFET is biased at high negative gate voltages and the drain doping is kept as high as the source doping, the addition of DP to a TFET is able to suppress the ambipolar current entirely. Furthermore, because both require similar doping types and concentrations, adding DP to a TFET devices is complementary to the well-known source-pocket technique in a TFET (Garg & Saurabh, 2018). However, previously, lowering TFET ambipolar current with a high drain doping concentration was effective. High drain region doping concentration, on the other hand, reduces the tunneling barrier at the drain-channel interface. It increases the OFF-state of leakage current.

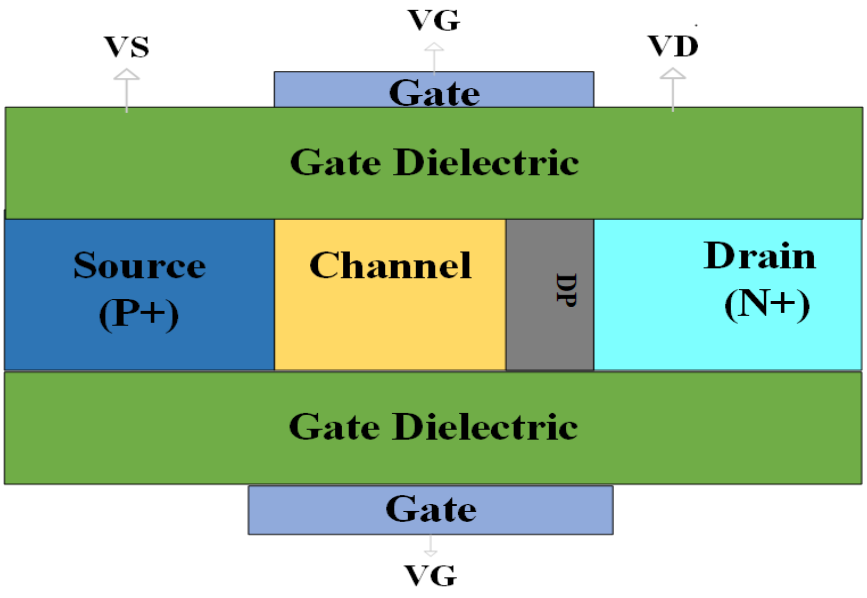


Figure 2.4: Cross-sectional view of DP-DGTFET

Investigation of Ge based double gate dual metal tunnel FET novel architecture using various hetero dielectric materials has been studied (Gracia et al., 2017) to overcome the challenges in conventional silicon (Si) based TFETs, a germanium based dual metal double gate tunnel

field-effect transistor device was investigated in this research. The performance investigation is carried out for various doping concentrations and hetero dielectric materials. It has a leakage current of 9.27×10^{-13} A/m and an I_{ON} of $1.3x10^{-4}$ A/m. This indicates that the device is more suited to low-power applications. (Gracia et al., 2017). Furthermore, Gracia presented a dual metal gate TFET, in which the ambipolar current is lowered, but the drain-gate overlap capacitance is increased, degrading the performance of the TFET devices at high frequencies.

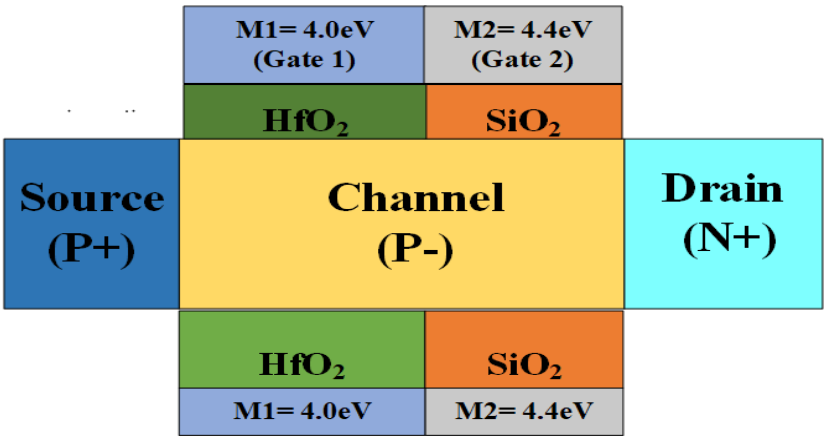


Figure 2.5: 2-D Structure of Dual Metal gate Double gate TFET

Controlling the drain side tunneling thickness to reduce the ambipolar current in tunnel FETs using hetero dielectric BOX has been studied in (Sahay & Kumar, 2015). In this study that utilizing a hetero dielectric BOX (HDB) above a highly doped ground plane can control the tunneling thickness at the channel–drain junction and suppressed the ambipolar current in tunnel FETs by using 2-D simulations (TFETs).

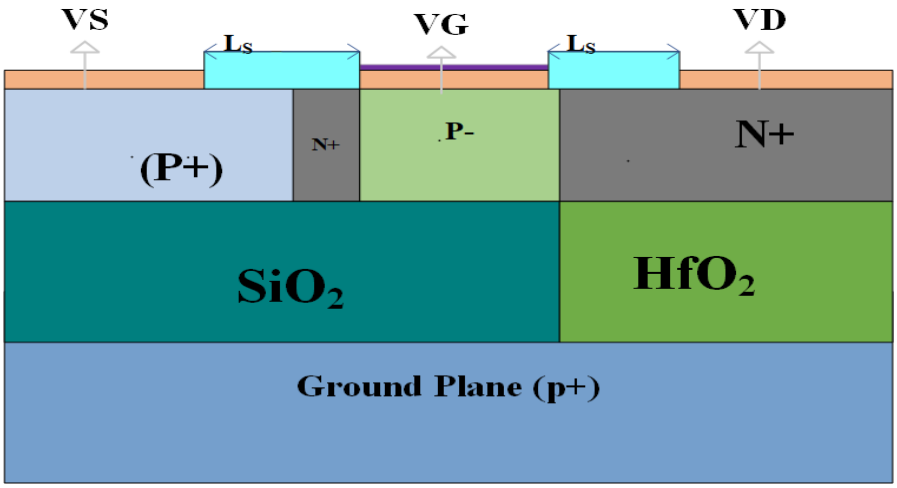


Figure 2.6: Schematic of HDB TFET

The HDB is made up of SiO_2 for source and channel regions and HfO_2 for the drain. Show that the drain region at the channel–drain interface is fully depleted when the HDB thickness is 25 nm and the ground plane is heavily doped. As a result, the tunneling thickness at the channel–drain interface increases, suppressing ambipolar conduction in a TFET (Sahay & Kumar, 2015).

Various "L-shaped architectures based on gate-source overlap structures and vertical channels" have been proposed to increase the current drivability of the devices and minimize the TFET footprint. On the other hand, Conventional L-TFETs structures have been shown to have significant ambipolar behavior (high ambipolar current), which needs further tuning (Li et al., 2018). Recently, "T-shaped TFETs with a gate-drain overlap (GDO) structure" has been studied to enhance the drive current simultaneously and suppress the ambipolar current (Chen et al., 2018). However, it is found that this T-shaped TFET with a gate-drain overlap structure can only suppress ambipolar current when V_{DS} is low. Besides, the GDO structure also increases the gate-drain capacitance, resulting in poor analog/RF performance parameters (Chen et al., 2018).

Table 2.1: A comparison of different approaches implemented for TFETs along with their advantages and limitations

Authors	Titles	Strength	Limitation
Pandey,et al.(2019)	Approach to suppress ambipolar conduction in Tunnel FET using dielectric pocket	•Lower ambipolar current	Analog/RF parameters have not been investigated
Goyal et al.(2022)	Performance analysis of DP-hetero gate dielectric DG-TFET: solution for ambipolar conduction and enhanced drive current	•Moderate I_{AMB} •High I_{ON}/I_{OFF} rate	Limiting the TFET at a high frequency
J.Talukdar & Mummaneni (2020)	A non-uniform silicon TFET design with a	•Moderate I_{ON}/I_{OFF}	Limiting the cut-off frequency

	dual-material source and compressed drain		
Garg&Saurabh (2018)	Suppression of ambipolar current in tunnel FETs using drain-pocket	•High I_{ON}/I_{OFF}	.Analog/RF parameters have not been investigated
Sahay & Kumar, (2015)	Controlling the drain side tunneling thickness to reduce the ambipolar current in tunnel FETs using hetero dielectric BOX	•Moderate I_{ON}/I_{OFF}	Ambipolarity slightly reduced
Gracia et al.(2017)	Investigation of Ge based double gate dual metal tunnel FET novel architecture using various hetero dielectric materials	•High I_{ON}	•Drain-gate overlap capacitance is increased

Generally, based on the above reviewing literature, two significant (major) problems with TFETs have been analyzed, these are:

1. Low ON-state current (low drivability of current and high leakage current)
2. Ambipolar conduction.

Therefore, to mitigate these problems and increase the I_{ON} of the device, a high electric field is essential at the source-channel junction, and the ambipolar current can be decreased by reducing an electric field at a channel-drain junction. Increasing the source doping, utilizing narrow band-gap materials at the source, reducing oxide and body thickness, adjusting the work function, and using dielectric engineering will increase the electric field (improve ON state current) at source/channel junctions. Besides, an electric field (ambipolar conduction) is reduced by providing the following solution: lightly doping at the drain region, increasing oxide thickness, wide band-gap material, work function, and dielectric engineering at channel-drain junctions.

CHAPTER THREE

SIMULATION METHODOLOGY AND DEVICE STRUCTURE

3.1. Overview

This section lists software requirements, simulation parameters, simulation flow chart, device structure, design parameters, circuit-based simulation, and comparisons of the device structure of TFETs.

3.2. Materials Requirement (Software)

- Silvaco Atlas technology computer-aided design (TCAD) simulation software (version of 5.0.10.R)
- S-Pisces/Mixed Mode
- Origin software
- Visio software

Simulation of the thesis study device structure has been performed using Silvaco Atlas TCAD simulator software. It is used for simulating and graphical analysis characterizing. The different device parameters have been analyzed using the Silvaco Atlas TCAD device simulator. Origin software is used for graph (data) analysis, Visio software is used to draw the device structure and flow chart, and another important tool is mixed mode, which is used for circuit-based simulation or inverter simulation.

3.2.1 Simulation Software Description

The Silvaco Atlas TCAD is a one-, two-and three-dimensional device simulation modular and extensible. It is a family of process and device simulation tools that provides users with the ability to perform and graphically analyze the result of electrical characteristics (i.e. I_D_V_G) of devices and simulation-based semiconductors designs. The Atlas framework-based products address the device simulation needs of all analog and digital application areas (Silvaco Inc., 2016).

ATLAS Inputs and Outputs

In the Atlas simulation, there are two input files. The first one is a text file, which contains ATLAS commands. The structure file is the second, which defines the structure that will be simulated. And also, there are three output files produced in the Atlas simulator. The run-time output is the first output file type, which displays the simulation's progress and shows

any problems or warning messages. The log file is the second output type, and it contains or retains all terminal currents and voltages. The third output file type is the solution file, which stores two-dimensional files about the values of solution variables within the device at a certain bias point ATLAS (Silvaco Inc., 2016).

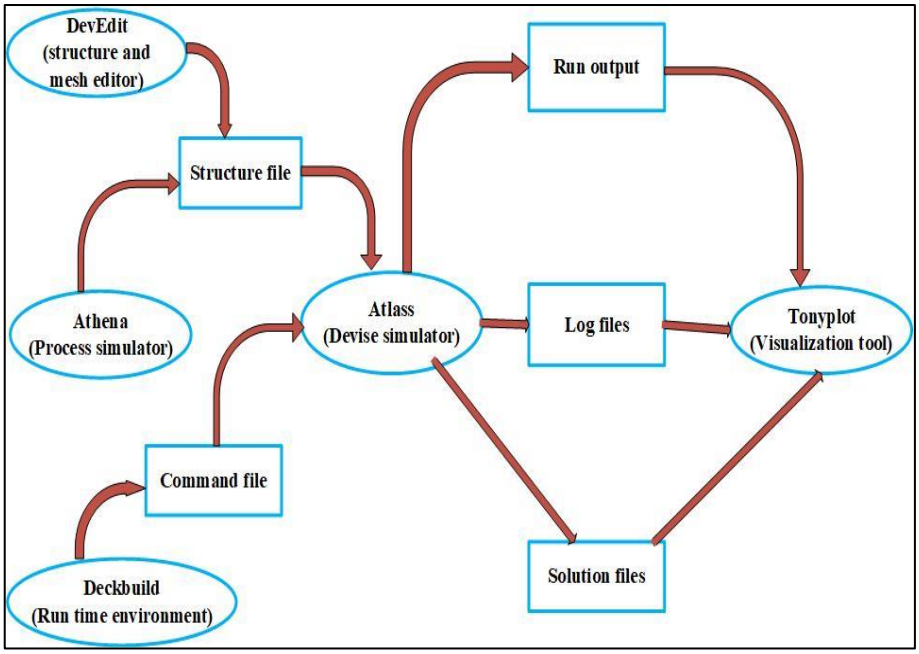


Figure 3.1: Atlas Inputs and outputs files (Silvaco Inc., 2016)

The ATLAS syntax

A list of commands for Atlas to perform or execute is called an Atlas command file. This list is saved as an ASCII text file, which can be created with DECK BUILD or another editor. Using the DeckBuild Commands option to prepare an input file is preferable and more accessible (Silvaco Inc., 2016).

Defining a structure

In Atlas, the structure of the devices can be specified in three methods. The first method is to read an existing structure from a file. ATLAS produces the device structure. The mesh, location, electrode positions, and structural doping are loaded using the MESH statement.

The second option is to use DECK BUILD Automatic Interface tools to transfer the ATHENA or DEVEDIT input structure. The third method uses the Atlas command language to build or create a structure. This study makes or generates all the structures using the ATLAS command language (Silvaco Inc., 2016).

3.3. Design Methodology

Computer-based simulations in technology (TCAD) examine the research of device performance and scaling potentials, as well as the resolution of poor analog/RF parameter performance. Further, the effectiveness of dielectric engineering (Dielectric pocket) tunnel FETs, which contributes to the decrement of I_{OFF}, reduction of ambipolarity, and I_{ON} enhancement essential parameter in analog/RF amplification are analyzed.

3.3.1. Simulation flow chart

Different Atlas programming steps are included in this section to simulate and design the structure of DP-TFETs based on device structure, meshing defining, defining a region, doping of region, models, I-V characteristics, parameter extraction, and so on. Furthermore, the DP-TFETs device structure demonstrates using the below flow chart diagram.

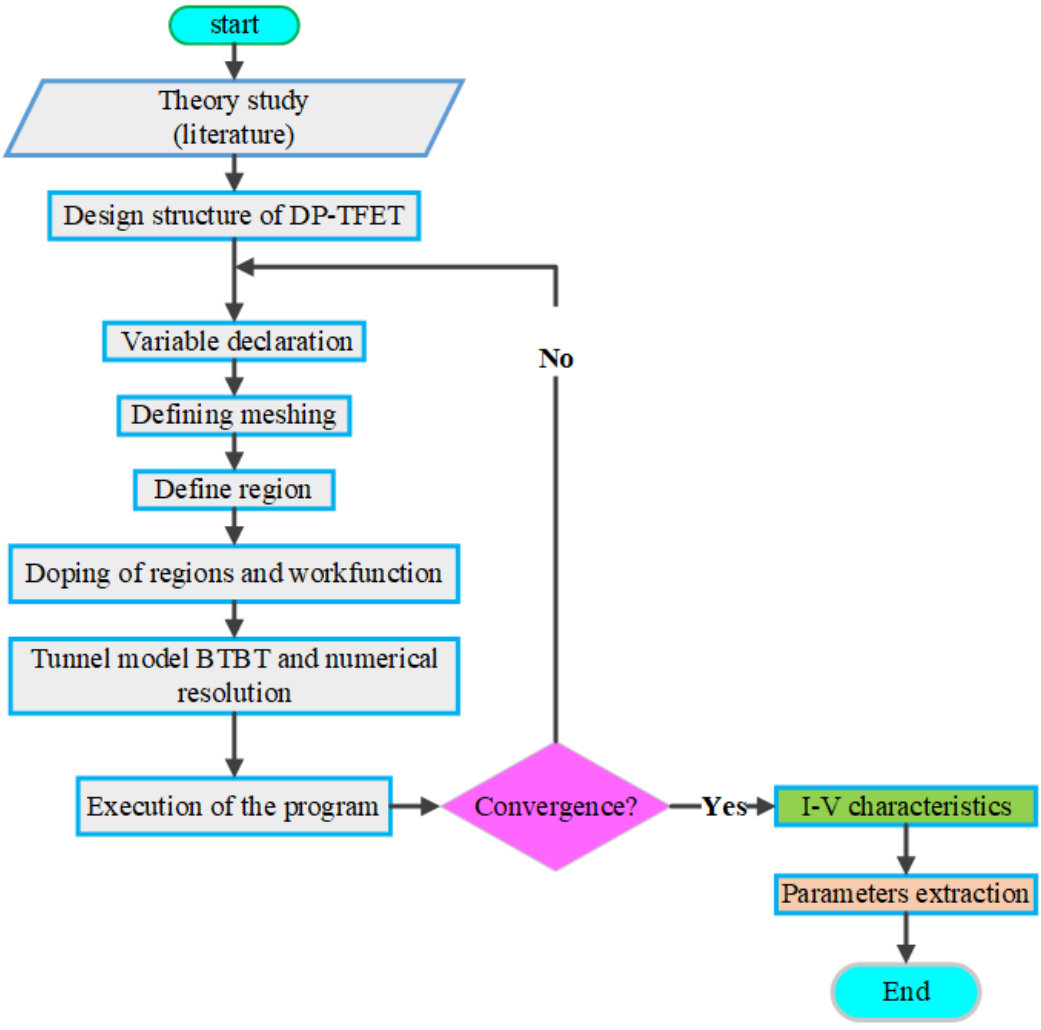


Figure 3.2: Atlas resolution algorithm of DP-TFETs

3.3.2. Simulation Procedures

The device structure of TFETs has been designed in a sequence of defining mesh, region, electrode, doping, and contact.

Meshing

The mesh statement defines the device structure in the 2-dimension cartesian grid. The x-axis side mesh (X.mesh) occurs on the left to the right hand, and the y-axis mesh (Y.mesh) is from bottom to top (Silvaco Inc., 2016). All coordinates or values are entered in microns meter (μm), and The spacing is used to refine the sharpness and precision at a given position (Vijayvargiya & Vishvakarma, 2014).

Table 3.1: Atlas Command groups with primary statements in each group

Group	Statements
Structure Specification	Mesh, Region, Electrode, Doping
Material Models Specification	Material, Model, Contact, Interface
Numerical Method Selection	Method
Solution Specification	Log, Solve, Load, Save
Result Analysis	Extract Tony plot

Regions

The region statement separates the initial mesh statement into blocks and defines the initial material parameters, which are then referenced by region number. A region must be assigned to each meshed area of a structure, and the regions must be ordered from lowest to a highest region (Silvaco Inc., 2016).

Electrode

Once the regions are set, the electrodes must be assigned to the desired region to be electrically analyzed. Any region or section of a region can be allocated electrodes. Gate, source and drain are some of the electrode names used by ATLAS. These parameters were defined using the following statements:

Electrode <location parameters> Name=<electrode name>

The X.min, X.max, Y.min, and Y.max metrics are used to specify the placement parameters in microns. Several electrode statements may have identical electrode names.

It is interesting to note that those with the same electrode name are considered electrically contact (Silvaco Inc., 2016).

Doping

The last required input of the device structure specification is the doping statement. Other characteristics can be added (to make impurity) to the doping statement to define how the semiconductor was doped and whether the region is N or P-type (Liu et al., 2016). To define doping type parameters, the following statements were used:

Doping <distribution type> <dopant concentration type> <location parameters

Uniform or Gaussian doping profiles can be found in analytical doping profiles. However, the uniform doping concentration in our thesis study was employed (Silvaco Inc., 2016).

Material

The material statement relates physical parameters with the materials assigned to the mesh. ATLAS defines the important material parameters for most standard semiconductors. This thesis work utilized the extensive model libraries in ATLAS since the developed tunnel junctions were based on silicon semiconductor material, which is well-researched and documented (Vijayvargiya & Vishvakarma, 2014).

Simulation Model

The local BTBT model approximates the tunneling barrier and assumes that the lateral electric field is constant throughout the tunneling area. However, a non-local BTBT model considers the electric field change in the tunneling region. Therefore, a non-local dynamic BTBT model to simulate BTBT current in TFET accurately and also, it is used that the Kane BTBT model to find the generation carrier due to band to band tunneling. Kane's model has been employed as:

$$G(E) = A\frac{|E|^2}{\sqrt{E_g}}\exp(-B\frac{E_g^{3/2}}{|E|}) \tag{3.1}$$

Where Eg is the energy gap and |E| is the magnitude of an electric field, which is explained as $|E| = E_x + E_y$. Auger and Shockley-Read-Hall recombination model has been added for

high impurity atom concentration in the channel region. The energy band-gap is a significant parameter that reduces heavily source region doping at a source-channel junction and increases band-gab with lightly drain doping at the channel-drain junction and directly impacts the tunneling current. Because of this reason, band bap narrowing (BGN) has been added for highly doped sources and lightly doped drains. The Fermi-Dirac model has been used to govern and decreases the charge concentration (charge density). The concentration-dependent mobility model, Lombardi model, and electric-field-dependent mobility model have been used as mobility models, and quantum tunneling direction models have also been added for the appropriate study of the performance of the TFETs device (Dutta et al., 2020) (Silvaco Inc., 2016).

After the simulation, a different number of parameters are observed by drawing a cut line along an arbitrary direction specified by two-point in the XY plane. The variation of different parameters, such as energy band diagram (conduction band and valance band), electric field (vertical and horizontal electric field direction), electron concentration (electron density), and electron BTBT generation rate, along the direction of the cut-line are examined. Finally, the two-dimensional Silvaco Atlas TCAD simulation justifies parameters by different characteristics (Silvaco Inc., 2016).

Table 3.2: Description of different models used

Model	Syntax	Comments
Shockley-Read-Hall	SRH	Responsible for generation-recombination, Used for a fixed minority lifetime.
Band Gap Narrowing	BGN	Important in the heavily doped region (Specify band-gap narrowing model).
Lombardi (CVT) model	CVT	To account for the high field mobility effect
Band to band tunneling (Kane)	BBT.KANE	Allows modeling of forward and reverse tunneling

Concentration mobility	CONMOB	They are used for low-field mobility to the impurity concentration.
Auger transition	AUGER	Important at a high current density.
Field dependent mobility	FLDMOB	Used in field mobility.

The statement used in the code is listed below:

Models SRH CVT BGN Fermi Print BBT.Kane print

Output

By default, a structure file contains several values, such as doping, I-V curve, electron concentration, electric field, electron BTBT, etc., by using the output statement (Silvaco Inc., 2016).

Output val.band con.band u.bbt charge e.lines band.param e.field j.electron j.hole j.conduc j.total ex.field ey.field e.mobility

Solution Specification

In ATLAS simulations, the log/solve/save instructions are used to create data files. These statements work together to generate data to analyze for other functions. In this study, these statements of the drain current with respect to gate voltage are used to analyze device structure results (Silvaco Inc., 2016).

Log

The LOG statement allows all terminal characteristics generated by a solve statement to be saved to a file.

Solve

The SOLVE statement specifies which bias points are to be applied to produce an output.

Save

All node point data is saved into an output file using the SAVE statement. For the tunnel junction of the study, the typical use of the LOG/SOLVE/SAVE statements is depicted below.:

Solve vgate=-2 vstep=0.1 vfinal=2

Save outf=test.str

Tonyplot test.log

Tonyplot test.str

3.4. Device Structure and Simulation Approach Descriptions

3.4.1. TFETs Structures

The design device structure is a silicon-source-based SOI-TFET with a dielectric pocket (DP) at the top of the drain region. The study of device structure (DP-TFET) has been compared to a conventional TFET (without DP) and, as shown in Figure 3.3, the optimum thickness and length of DP (dielectric pocket) at the drain region were found to be 6nm and 5nm, respectively, and DP is made up of dielectric constant to achieve low leakage current, which improved device performance. Additionally, the device structure design parameters, such as gate oxide, are made up of high-k dielectric (HfO_2), and dielectric thickness is 5nm. The Insulator region of SOI made of SiO_2 is a place to provide isolation between drain and source. The gate length is 45 nm and is made up of metal work functions that are kept constant at 4.9eV. The length of the source and drain regions is fixed at 100nm each, respectively. A doping concentration of 1×10^{20}, $1\times10^{16,}$ and 5×10^{18} cm^{-3} is selected for source, channel, and drain regions, respectively. A lightly p-type doped layer at a substrate is added in the BOX (buried oxide) at a certain depth from the back silicon dioxide (SiO_2) interface. Adding a BOX in the device structure depletes the drain region at the channel-drain junction and reduces the leakage current. The BOX also controls the short channel effect (SCE), which helps with device scalability (Sahay & Kumar, 2015).

Table 3.3 lists the device parameters that have been used in the design of the TFET simulation structure. The parameter numbers used here are taken from the ITRS roadmap.

Table 3.3: List of parameters in TFETs device simulations

Parameters	Values
Channel length and thickness	45 and 15 nm
Gate work function,	4.9eV
Source length and thickness	100 and 15 nm

Drain lengths and thickness,	100 and 15 nm
Source doping	1e20 cm^{-3}
Channel doping	1e16 cm^{-3}
Drain doping	5e18cm^{-3}
Gate oxide (HfO_2) thickness	5 nm
Silicon-On-Insulator (SOI) thickness (tsi)	25 nm
Silicon-On-Insulator (SOI) length	100 nm
Substrate doping (NA)	1e16 cm^{-3}
Drain pocket (material HfO_2) length	2nm to10nm
Drain pocket (material HfO_2) thickness	2nm to 6 nm

In the designed TFET structure source region is heavily P-type doped. A drain region is lightly doped with n+ type, while the channel is lightly doped with P-type. The higher doping levels in the source region and lightly drain side doping added with that of a DP-TFETS are needed to optimize the device's performance, which is required for ON-state current and reduces ambipolar current (I_{AMB}), respectively. The gate terminal controls the electrostatic potential and the charge concentration, thus increasing the junction between the semiconductor and the extrinsic region (R et al., 2022).

The profile simulated structures mentioned in Figure 3.3(b) are:

- Region-one is the HfO_2 layer of 5 nm on the top of the drain, source, and gate
- Region two is the source region of length 100nm and a thickness of 10 nm
- Region three is the HfO_2 pocket drain region with a length and thickness respectively 5 nm and 6 nm.
- Region four-channel length of 45nm and a thickness of 15 nm.
- Region-five SOI region with the length and thickness respectively 245 and 25 nm.
- Region-six is a drain region of length 100 nm and a thickness of 15 nm
- Region-seven is silicon substrate under an insulator of length and thickness of 245 nm and 65 nm, respectively.

So, by partitioning the above structure into definite regions, we have been able to design the device structure correctly. The dielectric pocket and box areas are composed of HfO_2 and SiO_2, respectively.

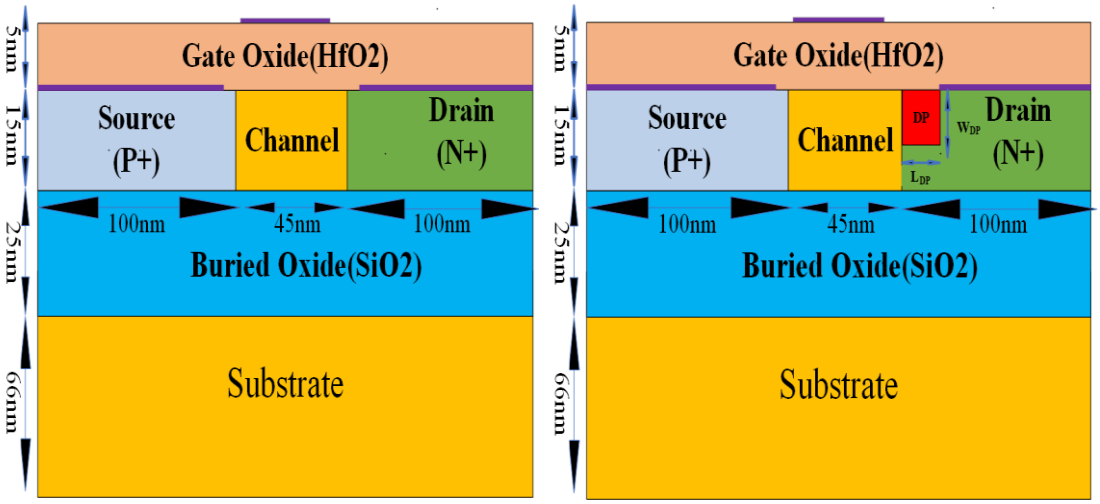
The Doping Profile of the simulated Structure is given below:

- The doping density in region2-------uniform, P-type 1×10^{20}
- The doping density in region 4------uniform, P-type, 1×10^{16}
- The doping density in region 6------uniform, N-type, 5×10^{18}
- The doping density in region 7------uniform, P-type, 1×10^{16}

Dielectric materials used and their properties

Table 3.4 List of dielectric materials used and their properties

Dielectric materials	**Properties**	
	Energy band-gap (eV)	Permittivity (i.e. K)
SiO_2	9	3.9
Si_3N_4	5	7.5
HfO_2	5.7	25



(a) **(b)**

Figure 3.3: Basic structure of (a) Conventional n-type TFETs (without DP) and (b) proposed structure of TFETs (DP-TFETs)

The two-dimensional device structure of the conventional TFETs and the proposed DP-TFETs structures are shown in Figures 3.3(a) and (b). Figure 3.3(a) has the same device dimension and structure same as DP-TFETs except for the addition of DP at the drain region. In DP-TFETs, the drain region of the device's structure has been scaled down to its optimal length of dielectric pocket (L_{DP}) and pocket thickness of dielectric pocket (TDP). Furthermore, a dielectric pocket (DP) or a high-k dielectric (HfO_2) at the length and thickness drain side has been mounted above the scaled drain regions. Similarly, adding a dielectric pocket (DP) in the portion of the drain is shown to increase the tunneling thickness at the channel-drain junction, resulting in the ambipolar current being reduced. This is the only structural difference between the thesis study (DP-TFETs) and conventional TFETs.

3.5. TFET Process Steps

Figure 3.4 illustrates that the DP-TFET structure can be made on a lightly doped p-type SOI wafer. For the DP-TFETs device, the following procedures were necessary.

- Thermal Oxidation: The SOI layer is first scaled down to 25 nm, and then the formed oxide is removed using this method. The active area is patterned using optical lithography and dry etching.
- Atomic Layer Deposition: this process is utilized to place aluminum as the gate (Al), low-temperature oxide (LTO) gate-hard mask, and hafnium oxide as the capping layer.
- Ion Implantation and Thermal Annealing: Ion implantation technique has been used for masking, whereas thermal annealing has been used for lightly n-type impurity doping in the drain region.
- Isotropic Dry Etching: This process has been used to recess silicon in the source area undercutting the gate electrode.
- Low-Pressure Chemical Vapour Deposition: The boron-doped silicon is deposited using this Low-Pressure Chemical Vapour Deposition (LPCVD) reactor. An extra patterned and etched LTO layer has been deposited to enable direct probing of the gate, source, and drain regions.

The fabrication process of the device structure is similar to that of the conventional TFET, except for an extra step for fabricating DP on the drain side, and the gate oxide is HfO_2. Jurczak et al. presented a method for fabricating a DP in the drain region. To determine the thickness of DP, use anisotropic plasma etching to create a 6nm depression in the drain

region. Then, using the plasma-enhanced chemical vapor deposition (LPCVD) process (technique), DP (dielectric pocket) can be deposited in a depression created inside the drain region. After deposition of DP, the excess part of the depression region formed during the etching process is now refilled using the selective epitaxial growth technique (Jayanarayanan et al., 2006).

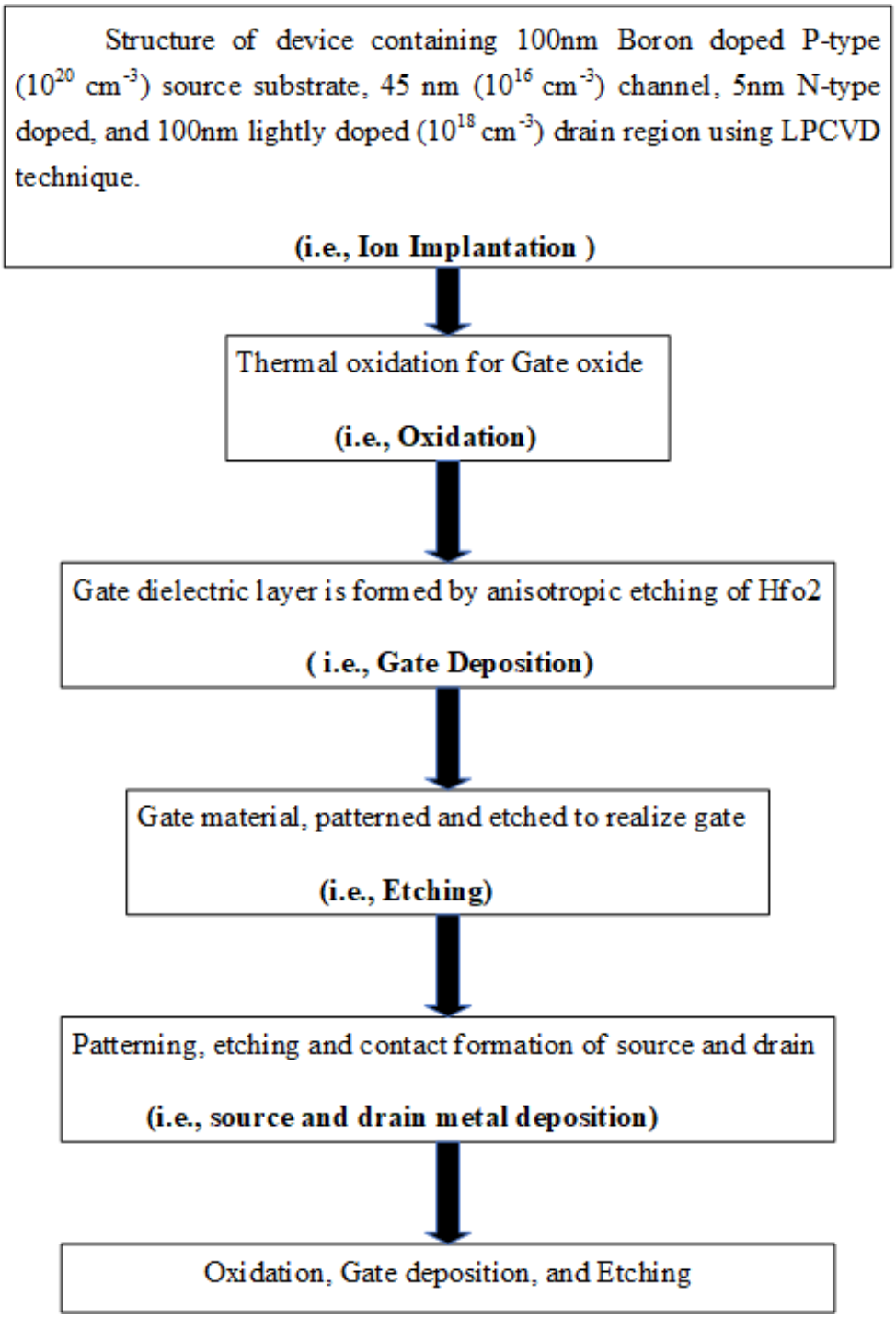


Figure 3.4: Steps in the fabrication of the DP-TFETs device

3.6. Circuit Simulation

In a mixed-mode simulation, physical-based device models can be substituted for a compact model device. The Atlas TFETs (AP) are to be simulated by the Silvaco Atlas TCAD simulator to do the circuit simulation of the device structures as an inverter. As shown in Figure 3.5, the drain is connected to a node 1(NET1) while the source is connected to a ground node (GND), the gate to connected to node 3(NET3), and the circuit's input voltage (V_{IN}) is supplied to node-3(NET3), and the transistor's output (AP) is generated from node-1(NET1), which produces output. The output of an inverter generates the logical value that is the inverse of the logic value applied to the input. Figure 3.5 shows that such a circuit acts as an inverter (Priya et al., 2019).

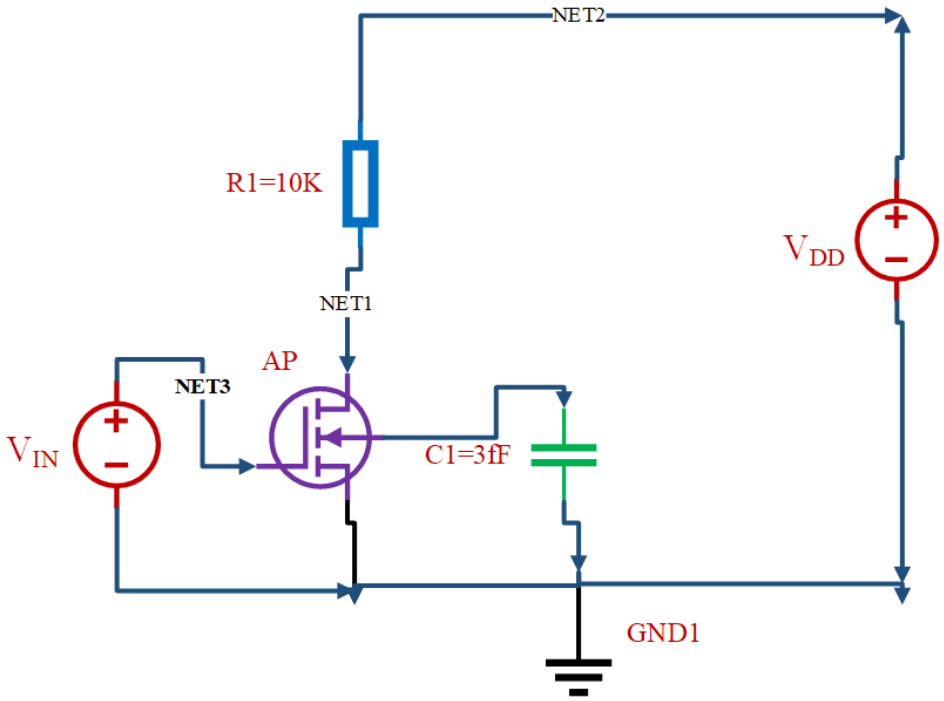


Figure 3.5: DP-TFETs inverter circuit

CHAPTER FOUR

RESULTS AND DISCUSSIONS

The structural design result is evaluated using the Silvaco Atlas TCAD simulator. This chapter has a discussion of the results based on the TCAD simulations. It has studied and analyzed the simulated transfer characteristics (I_{DS}-V_{GS}), electron BTBT generation rate, electric field (horizontal and vertical direction), and electron concentration. Besides the device's electrical characteristics parameters and impact of various dielectric pocket parameters such as pocket dielectric material, pocket thickness (T_{DP}), and pocket length (L_{DP}) are mentioned in this section. Additionally, the analog/RF parameters, comparisons between conventional TFETs (without DP), and proposed TFET (DP-TFET), and inverter-based simulation will be evaluated.

4.1 Performance Metrics

Several effective measurement systems of TFET, and their performance is important for the digital, analog/RF application viewpoint. These are described as follows:

ON-state current, OFF-state current, and ambipolar current

The drain current at V_{GS}=-1.5V and V_{DS}=1V is the ambipolar condition (state) of the TFET considered in this thesis study. OFF-state current is the drain current values at V_{GS}= 0V and V_{DS}=1V and ON-state current V_{GS}= 1V and V_{DS}=1V. To utilize the TFETs for low power, high speed, high bandwidth, and high-frequency performance, tunnel FETs need to achieve the high I_{ON}, lower $I_{OFF,}$ and ambipolar current (I_{AMB}).

Transconductance is an essential parameter for achieving a high-frequency characteristic (cut-off frequency and gain-bandwidth product). This parameter indicates the amplification capability of the TFET devices and is expressed as the change of the gate-source voltage (V_{GS}) to drain current (I_D) occurs.

Gain bandwidth product (GBP) is a parameter that shows the amplifier's ability to magnify both high and low-frequency message signals, which influences the frequency selectivity in device applications.

Cut-off frequency (f_T) is a frequency characteristic analysis method for electronic devices and analog/RF performance. It can be calculated using the g_m / C_{gg} ratio. Whereas g_m is transconductance and C_{gg} is total gate capacitances.

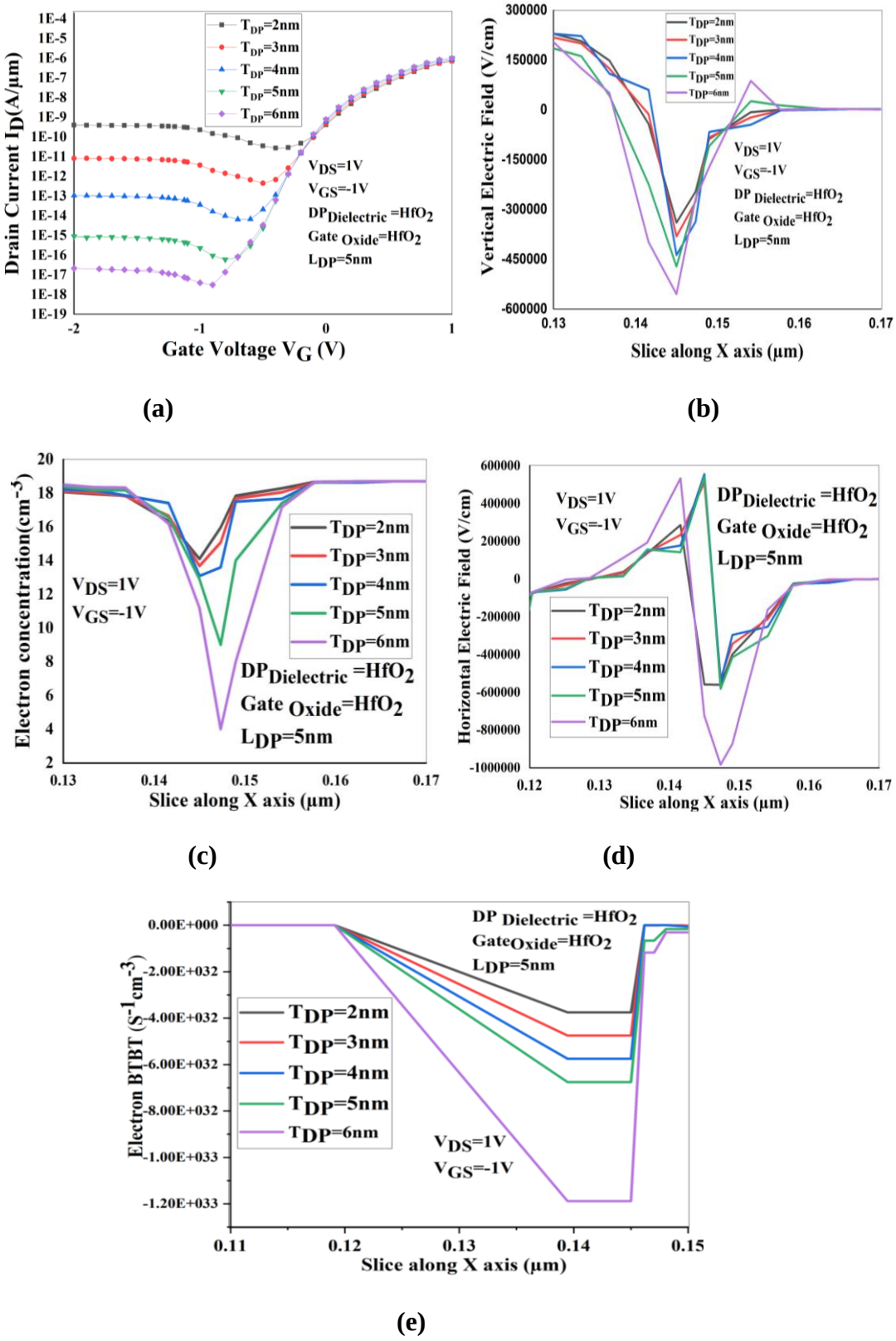
4.2. DP-TFETs Parameters Variation Study

This section contains an exhaustive parameters variation in a DP (dielectric pocket) of length (L_{DP}), a thickness of the DP (T_{DP}), and dielectric materials of DP on the TFETs device is investigated to select optimum parameter values.

(I). Impact of DP thickness (TDP) variation on device performance

This section covers various device parameters of the DP-TFET that are investigated with varying DP thickness. Figure 4.1(a) compares the transfer characteristics of the device for various dielectric pocket (DP) thickness values. The rate at which charge carriers travel through the junction determines ambipolar conduction at the drain-channel interface. When a dielectric pocket is present above a scaled drain terminal at the drain-channel junction, the underlying drain region is significantly depleted. During simulations, the DP length is kept fixed at 5 nm, and HfO_2 is added in the dielectric pocket area are fixed, because a dielectric with a high K (dielectric constant) value has a more significant effect on the electrostatic behavior in the drain region. As observed in the figure, an ambipolar current is reduced from 10^{-9} to 10^{-17}A/μm when T_{DP} has increased from 2nm to 6nm, respectively, and ambipolarity is nearly removed up to 6nm thickness of DP (T_{DP}).

Figure 4.1(b) illustrates the electric field along the vertical direction of the drain-channel junction with the dielectric pocket thickness varying. The figure shows that the electrical field can be reduced at the drain-channel junction as the thickness of DP increases due to the larger depletion of high K in the T_{DP}, which decreases I_{OFF} and ambipolar current. Figure 4.1(c) shows the result of increasing the dielectric pocket thickness (T_{DP}) on the horizontal electric field at a channel-drain (C-D) junction. The horizontal electric field at a channel to drain interface significantly decreases when the thickness of DP increases. Since the fringing field comes from the dielectric pocket, the output tunneling junction is widely spread over the depleted drain region below DP; due to these causes, the electric field (flow of charge carriers tunneling) is reduced at a C-D junction. The electron concentration of the DP-TFET along the C-D junction is illustrated in Figure 4.1(d). Due to a dielectric pocket with a thickness of 6nm having a broader or wider electron concentration, the tunneling width at the output tunneling interface increases, which decreases the charge carrier tunneling rate through the drain-to-channel junction. The effect of T_{DP} on the BTBT electron in TFET is shown in Figure 4.1(e), in which the electron BTBT (band to band tunnel) generation rate of charge carriers is decreased when the T_{DP} is increased



Figures 4.1: DC characteristics of the DP-TFETs (a) transfer characteristics, (b) vertical electric field, (c) horizontal concentration, (d) electron concentration, (e) electron-BTBT generation rate, on variation of T_{DP}

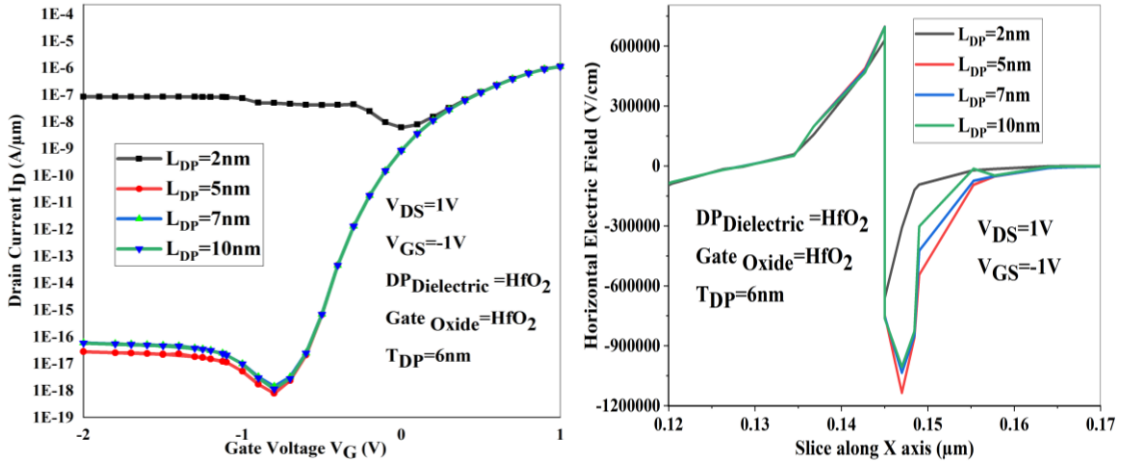
When TDP is increased, the electron BTBT is lowered; due to the reduced BTBT generation rate of electron charge carriers, the leakage current and ambipolar current in DP-TFET are reduced.

(II). Impact of DP length (L_{DP}) variation on device performance

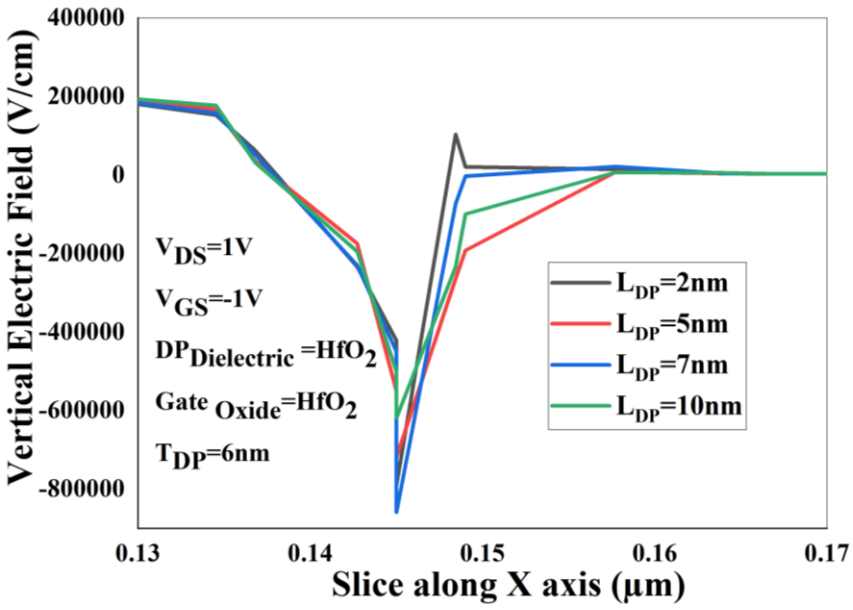
Figure 4.2(a**)** shows the effect of varying the dielectric pocket (L_{DP}) lengths at the drain region on the I_D-V_G curve of DP-TFETs. Throughout simulations, the thickness of the DP at the drain region is kept at its optimum of 6nm, and the dielectric material is constant with a high K (HfO_2) value. The I_{AMB} is about 10^{-17}A/μm when the length of the DP is 5nm (optimum). Furthermore, for dielectric pocket lengths greater than 5nm, I_{AMB} reduction stopped rapidly as DP length increased. Therefore, I_{AMB} is more suppressed when the length of DP is 5nm.

In Figure 4.2(b), the electric field in the horizontal direction is plotted for the L_{DP} varying from 2nm to 10nm at the ambipolar state. When DP is 5nm, an ambipolar current and leakage current are reduced. In other words, which further causes a significant increase in the tunneling barrier thickness of charge carriers at a channel to drain junction.

Figure 4.2(c**)** shows that the electric field in a vertical direction is designed to change the electric field when the DP-TFETs device is biased at the ambipolar state. With L_{DP}=5nm (optimum), the vertical electrical field induces rapid charge carrier recombination in the drain region below DP, and this causes the depletion area to appear at the channel drain interface of the DP-TFETs, causes a more expansion in the output tunneling barrier thickness at a C-D junction when L_{DP}=5nm.



(a) **(b)**



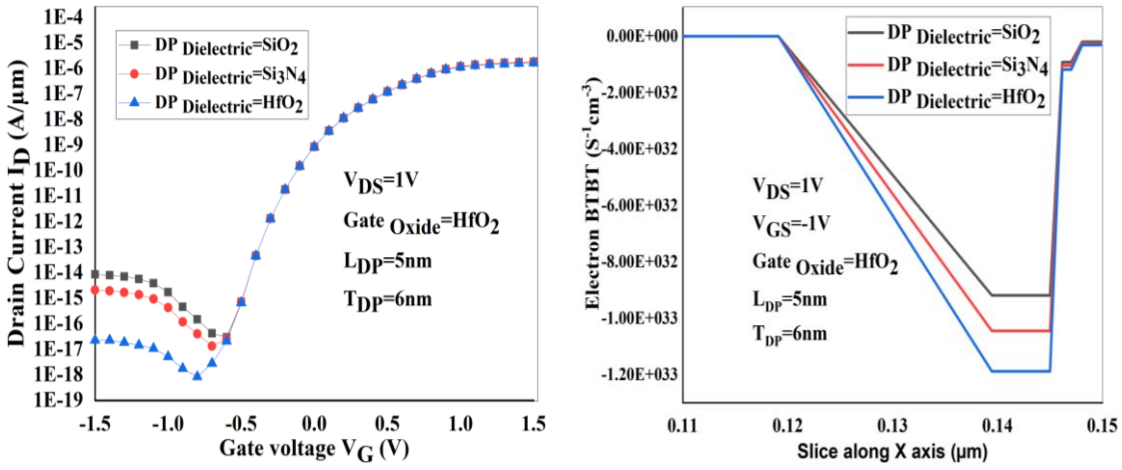
(c)

Figures 4.2: DC characteristics of the DP-TFETs (a) transfer characteristics, (b) horizontal electric field, (c) vertical electrical field, on a variation of L_{DP}

(III). Effects of Dielectric Materials

In this section, the impact of dielectric materials variation at the DP has been analyzed appropriately to achieve the low ambipolar current and low OFF-state leakage current. The physical DP dimension thickness is 6nm and length of 5nm, have been considered (optimum) with various dielectric materials, such as SiO_2, Si_3N_4, and HfO_2, which have different properties. The device's I_D-V_G is exposed in Figure 4.3(a) by varying the dielectric material at the DP. The graph result shows that high dielectric material HfO_2 shows higher performance (preferred) over two materials, Si_3N_4 and SiO_2. So high K-values have a more significant impact on reducing ambipolarity conduction and leakage current. Moreover, the fundamental goal of this study is to find a device structure that reduces I_{AMB} significantly without decreasing (affecting) I_{ON}. Because the existence of a dielectric pocket on the drain region has no effect on charge carriers' tunneling from the source-to-channel junction.

Figure 4.3(b), in which electron-BTBT generation rate of charge transfer by varying dielectric material (SiO_2=3.9, Si_3N_4=7.5, and HfO_2=25) device is biased at ambipolar state. The electron BTBT is reduced when DP is incorporated with TFETs; due to the reduction of BTBT generation rate at the C-D junction, an OFF-state leakage current and I_{AMB} are reduced in DP-TFET, and the order of this decrease is when a high-K (HfO_2) material is utilized in the DP, the result is found to be high.



(a) **(b)**

Figures 4.3: DC characteristics of the DP-TFETs (a) transfer characteristics or I_D-V_G curve (b) electron-BTBT generation rate for different dielectric materials at DP.

4.3. Device Optimization

This section analyses the impact of dielectric pocket with (proposed study) and without DP (conventional TFETs). To suppress the ambipolar current, reduce OFF-state current, and improve electrical characteristics of TFETs the TFET structure is modified, and a DP is introduced at the drain region.

(i). Performance comparison of conventional TFET and Proposed TFET (DP-TFET)

Figure 4.4(a) compares the I_D-V_G curve of the conventional TFETs (without dielectric-pocket) and with dielectric pocket or DP-TFETs. Primarily, it is noted that the transfer characteristics for conventional TFETs and DP-TFETs are similar in ON-state current (in positive gate voltages). This means the insertion of DP at the drain region does not affect (change) the I_{ON} performance. However, as shown in Table 4.1**,** different electrical parameter characteristics such as I_{OFF}, $I_{ON}/I_{OFF,}$ and SS have improved. While for the ambipolar state, it is noticed that I_{AMB} is suppressed from 9.38×10^{-7}A/μm in the conventional TFETs to 1.22×10^{-17}A/μm in the DP-TFET, thus decreasing the ambipolar conduction (I_{AMB}) by ten (10) order of magnitude.

Furthermore, it is demonstrated in Figure 3.3(b**)** that the studied structure with DP offers a lesser value of SS, ambipolar current, $I_{OFF,}$ and a higher value of I_{ON}/I_{OFF} rate when compared with conventional TFET thus improving the device performance special for low power operation and high-speed applications as well as digital and analog and radio frequency (RF) amplification.

So, with this small trade-off between transfer characteristics, the structure presented as better structure TFETs include those having a DP on the drain region.

Table 4.1: Comparison of performance parameters between the conventional TFET and proposed TFET (DP-TFET)

Performance Parameters	**Conventional TFET**	**Proposed TFET (DP-TFET)**
I_{ON} (A/μm)	2.09×10^{-6}	2.09×10^{-6}
I_{OFF} (A/μm)	4.13×10^{-8}	7.88×10^{-19}
I_{AMB} (A/μm)	9.38×10^{-7}	1.22×10^{-17}
SS (mV/dec)	~78	~58

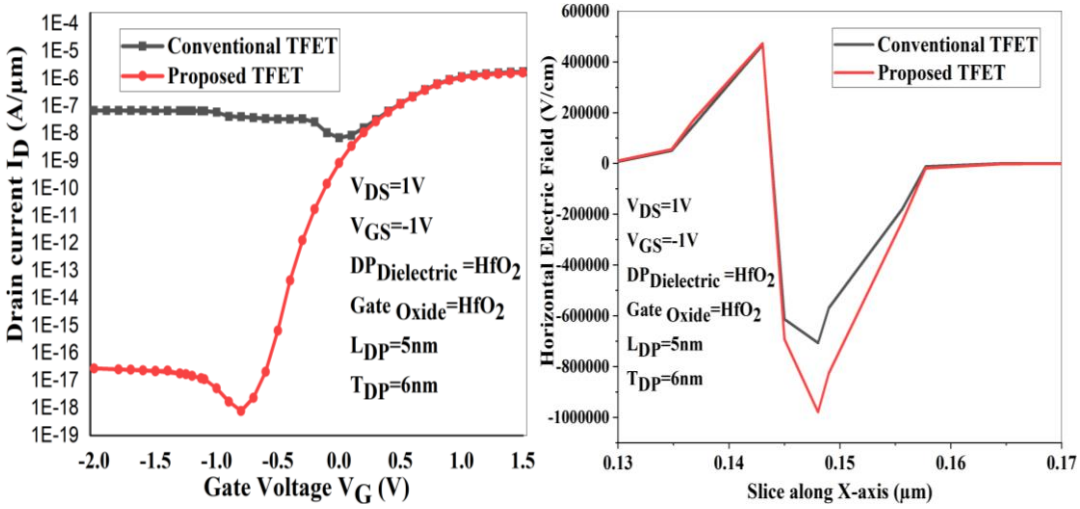
Figures 4.4(b) shows the comparison electric field of conventional TFETs and DP-TFETs in the horizontal direction at the C-D interface in the TFETs device. As observed from the figure, due to the addition of a dielectric pocket (DP), the electric field is decreased in the channel-drain interface, which means when an electric field is decreased at a C-D junction, the ambipolar current is significantly reduced in DP-TFET because the output tunnel barrier thickness is increased.

Yet again, as observed from Figure 4.4(c), electron concentration in the drain side of the conventional and proposed study is plotted at ambipolar current. As observed from the figure when comparing conventional TFETs with DP-TFETs, the electron charge carrier's concentration is reduced in DP-TFET because the insertion or addition of a dielectric pocket (DP) in the drain region decreases the electrostatic behavior of DP-TFETs devices.

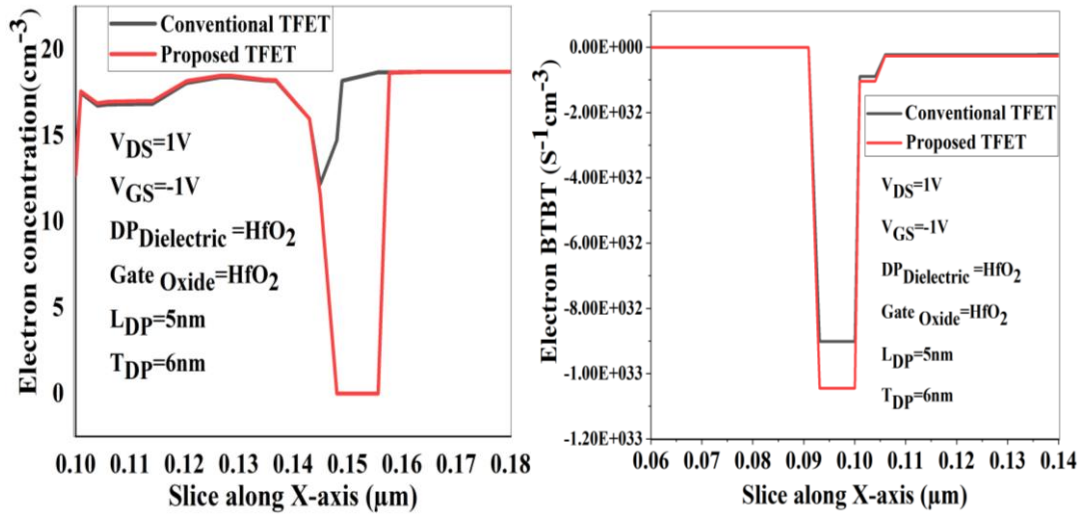
Figure 4.4 (d) shows the effects of DP in the ambipolar state, in which the electron BTBT generation rate is compared with conventional TFETs and DP-TFETs devices. The electron BTBT is reduced when DP is incorporated with TFETs. Due to this reduction in the BTBT generation rate of electron charge carriers, the ambipolar current is suppressed in DP-TFET,

and the order of this decrease is found to be high when HfO_2 dielectric material is used at DP.

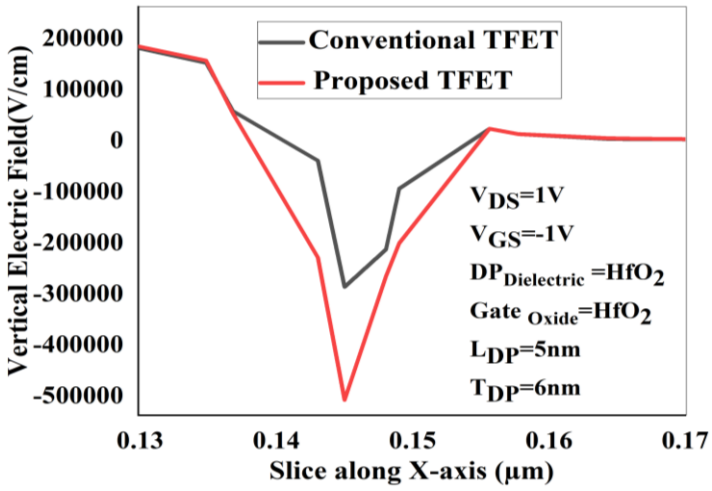
Figure 4.4(e) shows the electric field in the vertical direction at the channel-drain junctions without DP (conventional) and the proposed study based on the ambipolar state. The decreased value of the vertical electric field at the channel-drain junction using a dielectric pocket is better than that of conventional (without DP). This ultimately causes a wider reduction in output tunneling thickness in the channel-drain junction of DP-TFET, which leads to suppressed or reduced ambipolarity and OFF-state leakage current. Based on the observations made from analysis, an optimum value for all three design parameters of DP dielectric, L_{DP} and T_{DP} are found which cause the proposed device offering minimum OFF-state leakage current and ambipolar current as compared with the conventional TFET.



(a) **(b)**



(c) **(d)**



(e)

Figures 4.4: DC characteristics of (a) transfer characteristics (b) horizontal electric field, (c) electron concentration, (d) electron-BTBT generation rate, (e) vertical electrical field, between conventional TFETs and DP-TFETs.

Additionally, a subthreshold slope (SS) comparison between conventional and DP-TFETs is shown in Figure 4.4(f). A subthreshold parameter slope is defined as the change in gate voltage required to produce a one-decade increase in output current. The figure shows that the subthreshold slope for thesis study (DP-TFETs) is better than conventional TFETs.

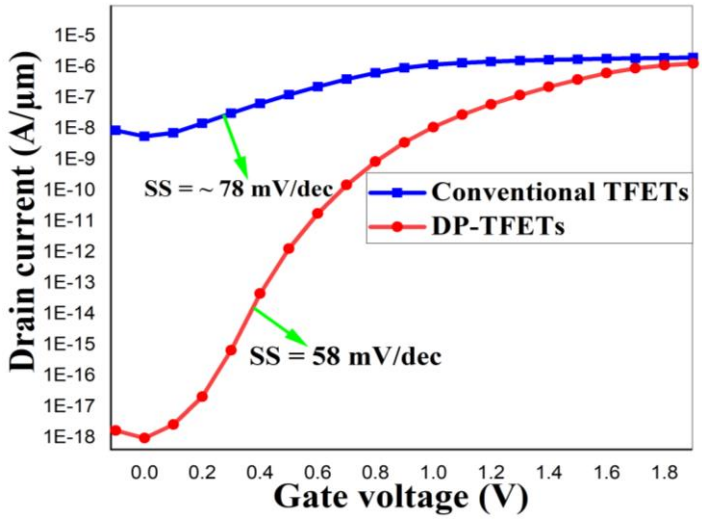


Figure 4.4(f): Comparison of transfer characteristics of conventional and DP-TFETs.

This indicates that the addition of DP at the drain region significantly impacts the reduction of subthreshold slope and the improvement of device performance. It is expressed as equation (4.1).

$$SS = \frac{\partial V_{GS}}{\partial \log I_{DS}} \tag{4.1}$$

4.5. Analog/RF Performance Analysis

This section explains the effect of DP by varying different dielectric materials for low power operations and the high-frequency applications. The analog/RF performance is evaluated based on the parameters like transconductance, cut-off frequency, gain-bandwidth product, and capacitance gate to source and drain can be analyzed for DP-TFETs.

(a) Transconductance Analysis:

The slope of the transfer characteristics of I_d-V_{gs} defines transconductance (g_m), which measures the device's amplification capabilities. (N et al., 2020). It is determined by the following equation (4.2).

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \tag{4.2}$$

As shown in Figure 4.5, the g_m of TFET with varying three dielectric materials at DP as a function of V_{GS} (gate-source voltage) for the channel of length 45nm and V_{DS}=1V. The higher transconductance value of low-K dielectric material (SiO_2) is better than the other dielectric materials (HfO_2 and Si_3N_4).

Notes: A device with a higher gm means has better control over the drain current.

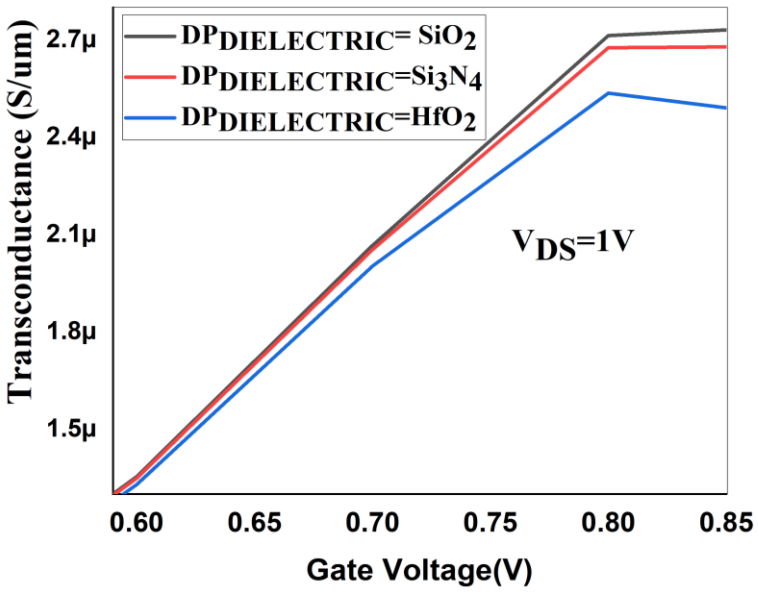


Figure 4.5: Comparative plots of transconductance between dielectric materials variation at DP

(b) Capacitance characteristics

The amplification capability and frequency characteristics of an analog/RF performance (and integrated circuit) are closely related to the total gate capacitance (C_{GG}). Capacitances exist in TFET due to the charges that have been deposited in the channel (Singh et al., 2016). The Miller-capacitance effect is exacerbated because TFETs have a much larger total gate capacitance than MOSFETs. The tunnel barrier width causes unbalanced charge distribution between source and drain regions, resulting in greater miller capacitances (Cgd and Cgs), leading to large overshot voltage/undershot and poor analog/RF performance (Ionescu et al., 2011). This section shows that both C_{GG} mainly consists of gate-to-source (C_{GS}) and gate-to-drain capacitance (C_{GD}). Gate capacitance is calculated using the change in gate charge (Qg) as a function of a small change in the terminal voltage (V) at each bias (Cgg). It can be obtained with the following equation (4.3).

$$C_{gg} = \frac{\partial Q_g}{\partial V_g} \tag{4.3}$$

The two capacitances between gate-drain and gate-source junction in DP-TFETs with varying three dielectric materials (i.e., HfO_2, Si_3N_4, and SiO_2) at the DP side as a function of gate voltage (V_{GS}) are compared in Figures 4.6 and 4.7, respectively. When the gate voltage is less in magnitude, there is no inversion layer created in the channel of TFETs, and the gate-to-source capacitance and gate-drain capacitance are crated parasitic capacitances. The inversion layer is created at the drain terminal as V_{GS} is increased, and it then travels towards the source terminal as V_{GS} is increased (Singh et al., 2016).

(i)Gate-to-Drain capacitance

Figure 4.6 show that DP has more effect on C_{gd} in DP-TFET with low-K dielectric material at DP. Due to this low-K dielectric, the intrinsic fringing field at the drain region is reduced, thus reducing the overall value of gate-drain capacitance (C_{gd}). As shown in Figure 4.6, low-k dielectric (SiO_2) offers the smallest value of C_{gd} compared to the other two dielectric materials, HfO_2 and Si_3N_4, with gate voltage function at 0.79V, which can be calculated by the equation (4.4).

$$C_{gd} = \frac{\partial Q_g}{\partial V_d} \tag{4.4}$$

Where Cgd is gate-to-drain capacitance, Qg is gate charge, and Vd is a voltage at the drain.

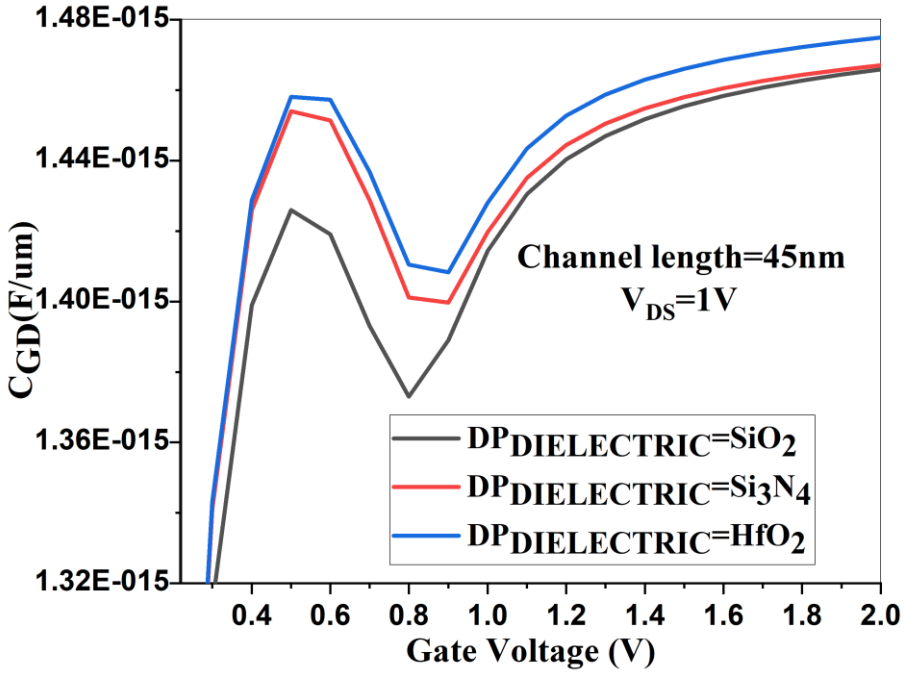


Figure 4.6: Comparative plots of gate-to-drain capacitance dielectric materials for HfO_2, Si_3N_4, and SiO_2

(ii) Gate-to-Source capacitance

Adding a dielectric pocket to the drain region of a TFET alters the values of gate-source capacitance. To analyze or observe the effect of dielectric materials, three different dielectric materials, HfO_2, Si_3N_4, and SiO_2, are added to DP.

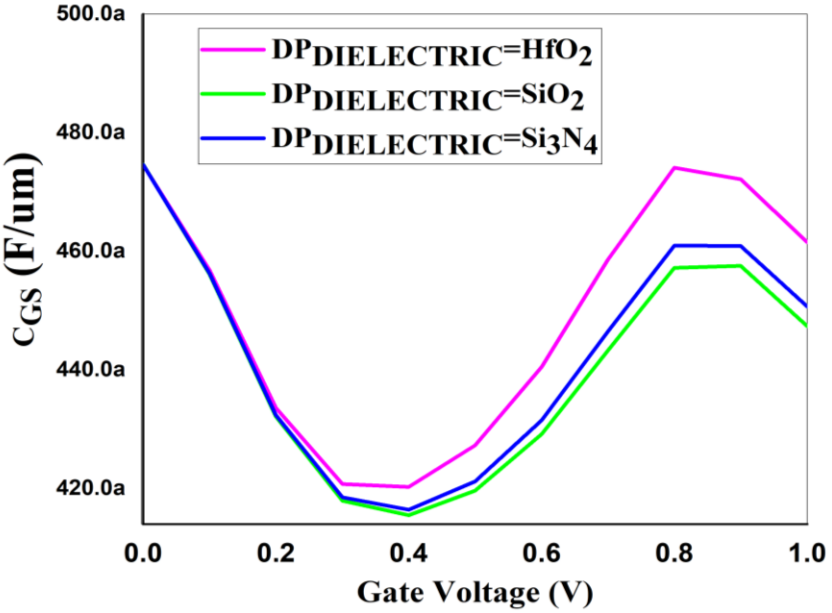


Figure 4.7: Comparative of gate-to-source capacitance for HfO_2, Si_3N_4, and SiO_2.

As observed in Figure 4.7, Cgs are reduced more in TFET by adding low K-dielectric material (SiO_2) at the dielectric pocket due to the fringing field coming out of DP and its interaction with the source-channel junction. The value of C_{gs} can be calculated by mathematical expression (4.5).

$$C_{gs} = \frac{\partial Q_g}{\partial V_s} \tag{4.5}$$

Where Cgs is gate-to-source capacitance, Qg is gate charge, and Vs is a voltage at the source.

(c) Frequency characteristics

Frequency characteristics or analog/RF parameters can be analyzed using the cut-off frequency and gain-bandwidth product.

(i) Cut-off Frequency Analysis

The cut-off frequency (f_T) is the most desired design parameter for high-speed and low-power applications, and it is a critical parameter in analyzing the analog/RF performance of a device. It determines the maximum frequency that can be amplified by the device (N et al., 2020). The cut-off frequency is obtained by the relation between the two parameters, g_m and C_{gg}, with the following relation, equation (4.5).

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{4.6}$$

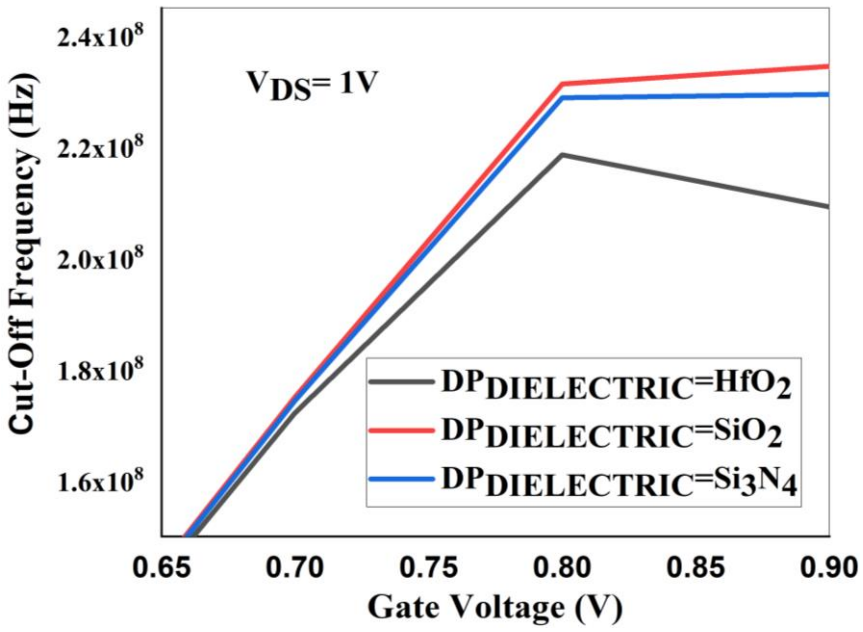


Figure 4.8: Comparative plots of cut-off frequency (f_T) for various dielectric materials

The cut-off frequency of three dielectric materials at DP as a function of Vgs is shown in Figure 4.8. Due to the gate capacitances (C_{gg}) in SiO_2 material (as shown in Figure 4.6) being relatively low compared to the other two dielectric materials, the high value of f_T can be observed when low-K (SiO_2) is added in DP. As shown in the figure, the value of f_T is simultaneously improving and achieves a peak value at Vgs 0.79V.

(ii) *Gain-bandwidth product Variation*

The gain-bandwidth product (GBP) is another vital analog/RF performance parameter. The GBP is a metric that describes how much an amplifier can amplify both high and low-frequency message signals and determines frequency selectivity in device applications (N et al., 2020), which can be calculated based on the ratio of two parameters (transconductance and gate-drain capacitance). It is expressed as equation (4.7).

$$GBP = \frac{g_m}{2\pi\left(C_{gd}\right)} \tag{4.7}$$

In Figure 4.9, it can be shown that SiO_2 (low K-dielectric) at DP has a higher GBP value than the other two dielectric materials (Si_3N_4 and HfO_2).

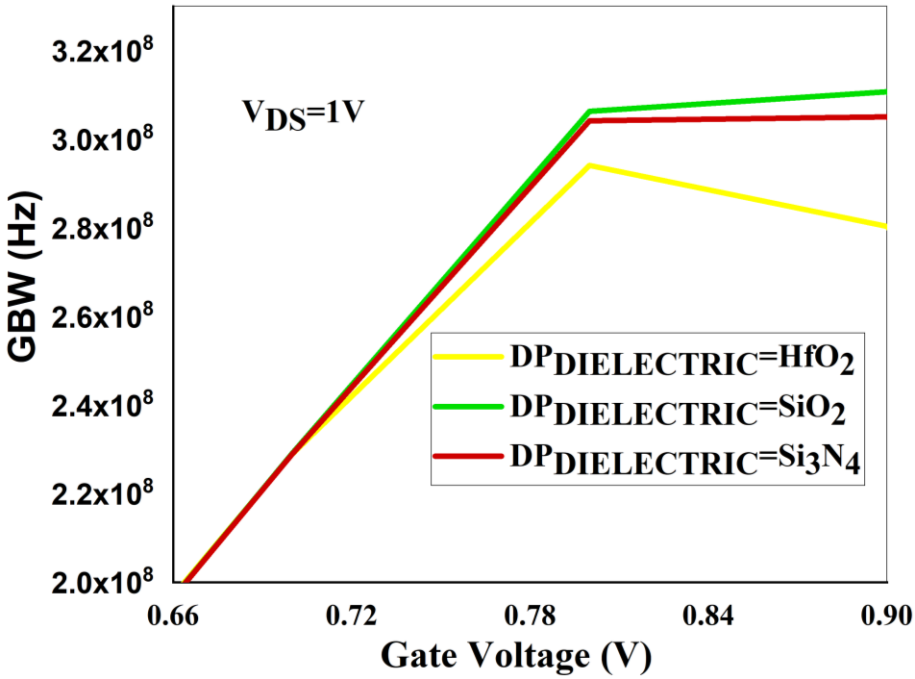


Figure 4.9: Comparative of gain-bandwidth product between the dielectric materials

Based on the results, it can be found that adding DP to a TFET with a low dielectric material (SiO_2) value improves analog/RF performance when compared to high dielectric material

(HfO_2) and medium dielectric material (Si_3N_4) at DP-TFET. For better result comparison, three dielectric materials' analog/RF performance parameters are listed in Table 4.2. This table shows the analog/RF performance, such as gate-to-source capacitance, gate-to-drain capacitance, transconductance, cut-off frequency, and gain-bandwidth product comparison of three dielectric materials.

Table 4.2: Extracted performance of the analog/RF parameters

Dielectric material	C_{GS} (aF)	C_{GD} (aF)	g_m (µS)	f_T (GHz)	GBP (GHz)
HfO_2	4.7	1.44	2.5	0.21	0.29
Si_3N_4	4.6	1.39	2.6	0.22	0.30
SiO_2	4.5	1.37	2.7	0.23	0.306

4.5. Performance Comparisons of Proposed Study and Other Works

This section has referred to different device structures of TFETs to understand our contribution work with some related works.

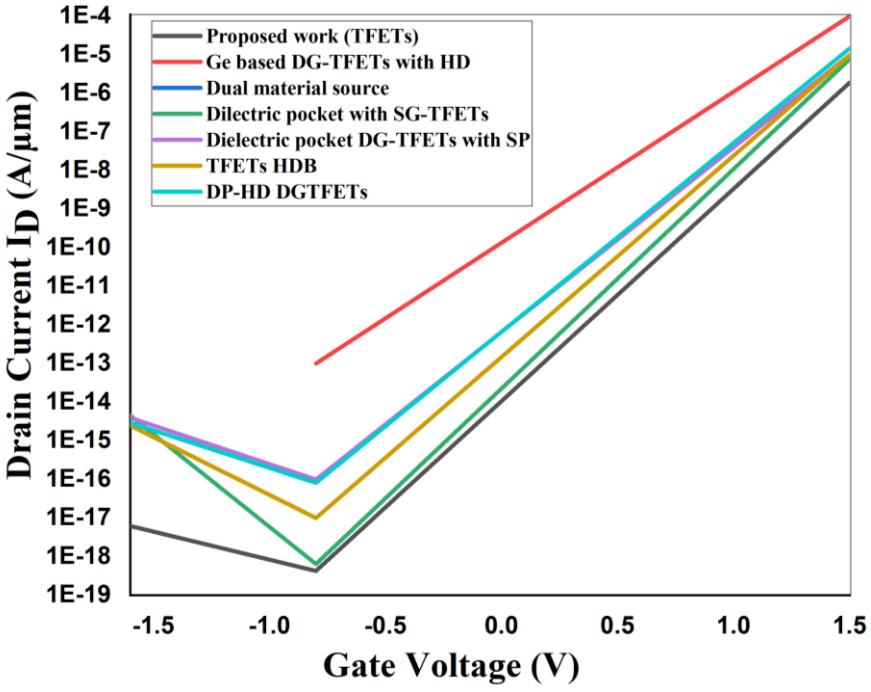


Figure 4.10: Comparisons of DP-TFETs transfer characteristics with other works

Table 4.3: Comparisons of TFETs Performance/Electrical characteristics of various devices with other works

Device structure	**I_{ON} (A/µm)**	**I_{OFF} (A/µm)**	**I_{AMB} (A/µm)**
Ge based DG-TFET with HD (Gracia et al., 2017)	$\sim10^{-4}$	$\sim10^{-13}$	-
Dual material source and compressed drain (J. Talukdar & Mummaneni, 2020)	$\sim10^{-5}$	$\sim10^{-16}$	$\sim10^{-14}$
Dielectric pocket with SG-TFETs (Pandey et al., 2019)	7.66×10^{-6}	6.43×10^{-19}	4.15×10^{-14}
Dielectric pocket DG-TFETs with SP (S. Garg & Saurabh, 2018)	$\sim10^{-5}$	$\sim10^{-16}$	$\sim10^{-14}$
TFETs HDB (Sahay & Kumar, 2015)	$\sim10^{-5}$	$\sim10^{-17}$	$\sim10^{-14}$
DP-HD-DGTFETs (Goyal et al., 2022)	1.48×10^{-5}	8.2×10^{-17}	7.2×10^{-15}
This work (DP-TFETs)	**2.09×10^{-6}**	**7.88×10^{-19}**	**1.22×10^{-17}**

Generally, as shown in Figure 4.10, transfer characteristics (DC characteristics), TFETs device structure with dielectric pocket (DP) or proposed work shows satisfactory results in a reduction of ambipolar current (1.22×10^{-17}A/µm) and OFF-state leakage current (7.88×10^{-19}A/µm), when compared with other devices structure this result is better than related work. Therefore, the proposed TFETs (DP-TFET) can be expected to be a capable structure of the TFET to achieve low-power operation and high bandwidth applications.

4.6. Inverter Circuit Implementation

The invertor analysis of DPTFET is investigated, and the circuit of the inverter is shown in Figure 3.5. To show the practical applicability of the DP-TFET, the resistive inverter with a 10K resistor as a load and DP-TFET as the driver FET is simulated and analyzed. The mixed-mode tool of SIVLACO TCAD is used to perform the simulation. The load is realized in the form of a capacitor 3Femto farad (ff) is taken as the load. The Spice netlist is written below which is used in the mixed-mode TCAD simulation.

V2 3 0 0

R1 1 2 10k

AP 3=GATE 1=DRAIN 0=SOURCE 0=SUBSTRATE INFILE=DP_TFETs.str WIDTH=15

C1 1 0 3fF

V1 2 0 1

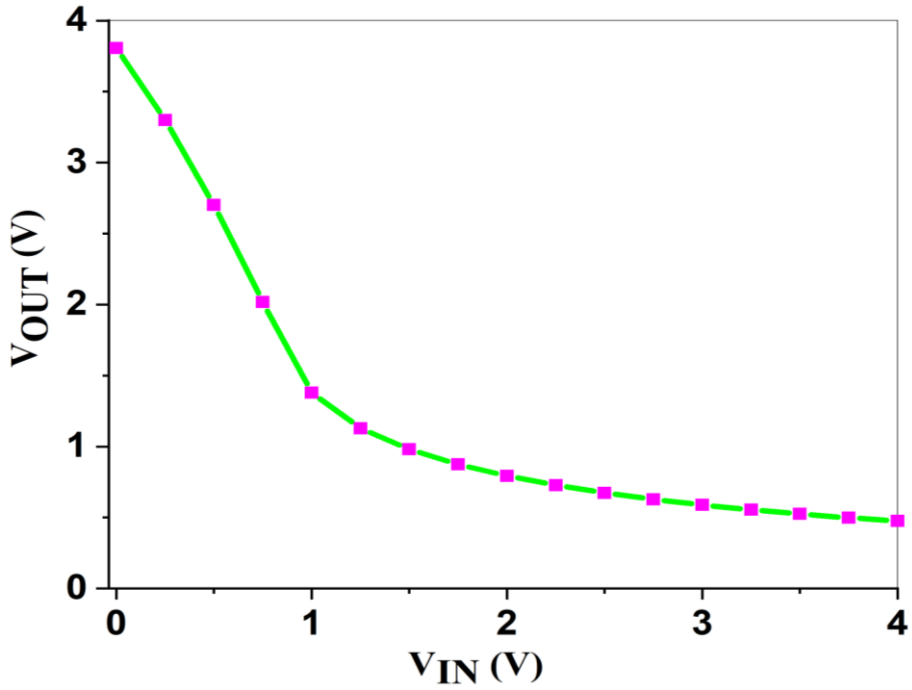


Figure 4.10 Input/Output plot for DP-TFETs Inverter

The DC performance in the form of voltage transfer characteristics (VTC) of circuit simulation is depicted in Figure 4.10. The input (gate) voltage was swept from zero to four volts to start the biased circuit. As is shown in the figure, when the applied voltage input becomes LOW, the output received is HIGH, and also, when the input is HIGH, the output received is LOW.

5. CONCLUSION AND RECOMMENDATIONS

5.1. Conclusion

In this thesis study, we have investigated the dielectric engineered SOI tunnel FET. This study aims to determine the solution for improved ON current (I_{ON}), decreased ambipolar current (I_{AMP}), and reduced leakage current in the TFET structure for better analog/RF performance. When the dielectric pocket (DP) is placed at the channel drain interface junction, ambipolar current is reduced. In this work, we have studied the effect of parameter variation such as TDP, L_{DP}, and dielectric DP on the device's performance tunnel FETs (TFET). It is observed that the dielectric pocket (DP) is an important parameter that effects the TFET device's ambipolar behaviour, further the ambipolar current is also reduced when the low K (SiO_2) material is replaced by the high K material (HfO_2).

The optimized dimension for the dielectric pocket is 5nm length, and 6nm thickness of beneath at the channel-drain junction. TFET device reached low ambipolar conduction, OFF-state current when compared to conventional TFET structure and with some related work. Furthermore, it has also been added (insertion) that DP at the drain side does not degrade the ON-state performance of TFET, thus improving the current drive capacity of the device. The reduced ambipolar current (I_{AMB}) is $1.22x10^{-17}$A/μm in this improved structure with a drain side dielectric pocket, while I_{OFF} (leakage current) is around $7.88x10^{-19}$A/μm, which is lower with approximately ten (10) magnitude than conventional TFETs. Furthermore, those DP-TFETs devices are suitable for low-power operation, which can be working at high frequencies, and different applications of tunnel FETs consist of low-power circuits. This work is done by using the 2D-Silvaco Atlas TCAD simulator.

Furthermore, as compared to the other two dielectric materials (SiO_2 and Si_3N_4), a high k dielectric material (HfO_2) delivers a more significant reduction in OFF-state current (leakage current) and ambipolar current. However, the analog/RF characteristic of DP-TFETs with low k-dielectric material (SiO_2) is significantly better than that of high K dielectric (HfO_2) and medium K dielectric material (Si_3N_4), and has a g_m of 2.7×10^6 S/μm, a gain-bandwidth product of 0.3GHz, and cut-off frequency of 0.23GHz. Additionally, to show the practical applicability of the DP-TFETs device, DC performance in the form of voltage transfer characteristics (VTC) of inverter circuit simulation is studied.

5.2. Recommendation for the Future Work

In the thesis study, we have discussed dielectric engineered TFET for low power analog/RF performance. Further research work in the areas covered in this thesis can be carried out as follows:

- We have added DP in the drain side without I_{ON} variation in our work. Improving the I_{ON} with DP at the source region would be another interesting area to make TFETs for the fast switching (high drivability of current).
- Incorporating the effect of strain in the device to improve mobility which further increases the ON current.
- Design the heterojunction TFETs with III-V alloys is another area to be explored
- Further the analytical modelling of the device can be performed.

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