

Analysis and Design of Multilevel Inverter Using SPWM for Closed Loop Induction Motor Drive

Case Study: Chemical Industry Corporation Muger Cement Factory

Erste Telila Sebetu



**A Thesis Submitted to the Program chair of Electrical Power and Control
Engineering**

School of Electrical Engineering and Computing

**Presented in Partial Fulfillment of the Requirement for the Degree of Master's in
Electrical Power and Control Engineering (power electronics)**

Office of Graduate Studies

Adama Science and Technology University

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Declaration

I hereby declare that this MSc Thesis is my original work and has not been presented for a degree in any other university, and all sources of material used for this thesis have been duly acknowledged.

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We, the undersigned, members of the Board of Examiners of the final open defense by **Erste Telila Sebetu** have read and evaluated his/her thesis entitled “**Analysis and Design of Multilevel Inverter Using SPWM for Closed Loop Induction Motor Drive**”, Examined the candidate. This is, therefore, to certify that the thesis has been accepted in partial fulfillment of the requirement of Master’s Degree of **Electrical power and Control Engineering (power Electronics)**.

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LIST OF ACRONYMS AND ABBREVIATIONS

AC	Alternative Current
APOD	Alternate Phase Opposition Disposition
ASDs	Adjustable Speed Drives
CMLI	Cascaded Multilevel Inverter
DC	Direct Current
DCMI	Diode Clamped Multilevel Inverter
EMC	Electromagnetic Compatibility
IM	Induction Motor
IPD	In Phase Disposition
MC-SFOPWM	Multicarrier Switching Frequency Optimal Pulse Width Modulation
MC-SHPWM	Multicarrier Sub-Harmonic Pulse Width Modulation
PI	Proportional Integrator
PID	Proportional Integrator Differentiator
POD	Phase Opposition Disposition
PWM	Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modulation
THD	Total Harmonic Distortion
VFDs	Variable Frequency Drives

SYMBOLS

f_c	carrier frequency
f_m	frequency of modulating waves
K_d	Derivative gain, a tuning parameter
K_i	Integral gain, a tuning parameter
K_p	Proportional gain, a tuning parameter
L_m	Mutual inductance
L_r	Rotor inductance
L_s	Stator inductance
m_a	amplitude modulation index
m_f	frequency modulation index
n_s	Synchronous speed
R_r	Rotor resistance
R_s	Stator resistance
v_c	peak carrier voltage
v_m	peak amplitude of voltage
Φ_c	phase shift angle between any two adjacent carrier waves
F	Friction factor
J	Inertia
M	Modulation index
m	multilevel inverter with m voltage levels
n	Level
N_p	Number of pulse
P	Nominal Power
PV	Process Variable
rpm	Revolution Per Minute
SP	Set Point
t	Time or instantaneous

ABSTRACT

The power loss, the electromagnetic stress dv/dt and Total Harmonics Distortion becomes the issue of industrial electrical drives today. Induction motors are most widely used machine in both industrial and domestic sector. However, they require variable-frequency power-electronic drive for their optimal speed control. Out of the various methods, the cascaded multilevel inverter based speed control has proven to be the most versatile. The SPWM techniques are used at this thesis work that providing better sinusoidal wave form of both voltage and current. In this thesis work, using MATLAB R2013a/SIMULINK software, a five and seven cascaded multilevel inverter topologies are analyzed, designed and simulated to eliminate the fifth and seventh harmonics that are dominant in closed loop induction motor drive. The THD values of five level and seven level CMLI inverter is compared. The THD value measured from chemical industry corporation mugher cement factory are 49% and 7. 10% for current and voltage respectively is compared with designed cascaded multilevel inverter are 4.06% and 5.06% for current and voltage respectively. Hence the cascaded multilevel inverter is proven and result with lower THD value. Moreover, the PI controller is designed and cascaded with multilevel inverter to obtain smooth speed control of IM as per settled reference speed. The smooth speed control IM is compared for the two CMLI for the same settling time and settled reference speed.

Keyword: Cascaded Multilevel (CML), Sinusoidal Pulse Width Modulation, PI controller, MATLAB/SIMULINK, speed control.

CHAPTER ONE

INTRODUCTION

1.1 Background of the study

Multilevel Pulse Width Modulation inverters have been gained importance in high performance power applications without requiring high ratings on individual devices, as static var-compensators, drives and active power filters. A multilevel inverter divides the dc rail directly or indirectly, so that the output of the leg can be more than two discrete levels. As both amplitude modulation and pulse width modulation are used in this, the quality of the output waveform gets improved with low Total Harmonics Distortion. The advantages of multilevel inverter are good power quality, low switching losses, reduced output dv/dt and high voltage capability. Increasing the number of voltage levels in the inverter increases the power rating. The three main topologies of multilevel inverters are the Diode clamped inverter, Flying capacitor inverter, and the Cascaded H-bridge inverter [1][2]. The PWM schemes of multilevel inverters are classified in to two types the multicarrier sub-harmonic PWM (MC-SHPWM) and the Multicarrier switching frequency optimal pulse width modulation (MC-SFOPWM) [4] [5]. The MC-SHPWM diode clamped multilevel inverter strategy reduced total harmonic distortion and the MC-SFOPWM technique for multilevel inverter strategy enhances the fundamental output voltage [6], [8]. For this thesis work MATLAB® R2013a /SIMULINK software is used for the design and implementation of cascaded multilevel inverters, and the way by which the performance of the machine can be improved by increasing the level of the inverter. This thesis work enhances the method to produce a wave which is similar to that of a sine from a DC source. This is mainly applicable where there is only DC supply like the Batteries, fuel, photovoltaic cell etc. As the main device which converts the DC power to AC power is inverter, this thesis deals with evolution of inverters. The type of inverter circuit used in this project is cascaded H-bridge inverter model as it is more advantageous compared with that of the others. The triggering pulses are produced by the sinusoidal pulse width modulation technique. The obtained output is given to the three-phase squirrel cage induction motor and its speed is taken and compared with that of the reference speed and the desired speed is attained using PI controller

1.2 Statement of the problem

The presence higher frequencies are engaged in traditional pulse width modulation methods because of the unwanted harmonics occur at higher frequencies, which can be

filtered easily and several kHz is well above the acoustic noise level. But, in the case of chemical industry corporation mugher cement factory the designed addition filter for the traditional pulse width modulation methods cause electromagnetic interference (EMI). The rapid change in voltage (dv/dt) is the cause of electromagnetic interference. A high dv/dt produces common-mode voltages across the windings of motor and leads to damage. As a result cascaded multilevel inverter based speed control will overcome the above problem for industrial motor drives.

1.3 Significance of the study

The need to signify cascaded multilevel inverter for closed loop induction motor drives, for the reason that this topologies can generate output voltage with extremely low distortion, lower dv/dt , draw the input current with very low distortion, provide smaller common mode voltage thus reducing the stress in the motor bearing, they can operate with a lower switching frequency. Hence this method prevents the switching loss, reduces Total Harmonic Distortion and unwanted power loss which result in extra billing cost for industry.

1.4 Objective of the study

1.4.1 General objectives

The main objective of this thesis Work is to analysis the existing speed control method of Chemical Industry Corporation Mugher Cement Factory and design cascaded multilevel inverter for closed loop induction motor drive by using PWM techniques.

1.4.2 Specific objectives

- To examine the existing speed control method of Chemical Industry Corporation Mugher Cement Factory.
- To design cascaded multilevel inverters using SPWM techniques.
- To design closed-loop PI controller that control speed of induction motor drive.
- To designed and test the combined overall system to verify the speed control of closed loop induction motor drive.
- To compare and analyzed THD level of both five and seven cascaded multilevel inverters voltage and current with the IEEE standard value [IEEE 519-1992].

1.5 Scope

This thesis work includes the design, simulation of the development of SPWM techniques for cascaded multilevel inverter speed control of closed loop three phase squirrel cage

induction motor by using MATLAB software. The design and simulation of cascaded multilevel inverter for speed control of induction motor in this thesis proposal is limited to five multilevel and seven multilevel inverter for the elimination of 5th and 7th harmonics.

1.6 Limitation

During this thesis work the researcher limited to the existing speed control method data at selected study area i.e. Chemical Industry Corporation Mughar Cement Factory. The company doesn't have data measured like THD values of their control method; this problem leads to inefficient use of Electric Power Utility.

1.7 Organization of the thesis

Chapter one deals with the complete introduction of the thesis work, statements of the problem, significance of the study, the aim of the thesis work and the way the thesis is organized. It also gives a basic idea of the content present in the thesis.

Chapter two deals with the literature review and also given for the further references. In this chapter various speed control of three phase induction motor is reviewed. The working of the basic inverter and its circuit operation along with the output waveforms, pulse width modulation techniques is explained. Then the need for the multilevel inverters is concentrated. The different types of multilevel inverters topology along with their advantages and disadvantages are explained.

Chapter three deals with methodology and system design. A detailed study on the sinusoidal pulse width modulation is explained and the way the pulses are produced for different levels are schematically shown. MATLAB®2013a /SIMULINK implementation of the generation of pulses and cascaded Multilevel for both five and seven level is also explained.

Chapter four deals with results and discussion of the thesis work. The THD value of five cascaded multilevel and seven cascaded multilevel inverter is compared and the THD value proven that as the number of level increases the THD value is reduced. The comparison of open loop and closed loop for both speed and load torques is discussed in this chapter. Chapter five deals with conclusions made and recommendation for this thesis work.

CHAPTER TWO

LITERATURE REVIEW

Adjustable Speed Drives (ASDs) and less THD are the essential and endless demand of the industries and researchers. They are widely used in the industries to control the speed of conveyor systems, blower speeds, machine tool speeds and other applications that require adjustable speeds. Now days, AC motors are preferred to DC motors, in particular, an induction motor due to its low cost, low maintenance, lower weight, higher efficiency, improved ruggedness and reliability. All these features make the use of induction motors in many areas of industrial applications [9].

2.1 Various speed control method of Induction Motor

There are various methods for the speed control of an Induction Motor. They are:

- Variable Rotor Resistance Control
- Variable Supply Voltage Control
- V/f Control
- Variable Supply Frequency control
- Speed control by pole changing
- Multilevel inverter based SPWM speed control etc.

Before the development of semiconductor power electronics, it was difficult to vary the frequency, and cage induction motors were mainly used in fixed speed applications. Applications such as electric overhead cranes used DC drives or wound rotor induction motors with slip rings for rotor circuit connection to variable external resistance allowing considerable range of speed control. However, resistor losses associated with low speed operation of wound rotor induction is a major cost disadvantage, especially for constant loads. Due to power loss in the resistance, this method is used where speed changes are required for short period only. This method also used for wound rotor induction method but not for cage motor [34].

Variable frequency drives can control the speed, but if we use this control method a lot of it will have harmonics in electric lines which damage sensitive electronic equipment, to prevent this it need more filter which need another cost [5].

By varying supply frequency (on small amount), we can vary the speed. But a decrease in supply frequency decreases the speed and increases the flux, core losses which lead heating and low efficiency. Increase in frequency increases the speed and reduces the torque.

Separate costlier auxiliary equipment is required to provide a variable frequency. So this method is not used in practical [34].

In the case of v/f control, speed of the motor is controlled by varying the ratio of v/f accordingly. But the speed is not varying proportional to application so it consumes the rated power and it becomes economical disadvantages [5].

The change of number of poles is done by having two or more entirely independent stator windings in the same slots. Each winding gives a different number of poles, so we will get different speeds. Due to cost and complex switching arrangements, it is not practical to provide more than two arrangements of poles (i.e. two normal speeds) [34].

Of the above mentioned methods, the advancement in Power Electronics and semiconductor technology has triggered the development of high power and high speed semiconductor devices in order to achieve a smooth, continuous and step less variation in motor speed. Applications of solid state converters/inverters for adjustable speed of induction motor drive are wide spread in electromechanical systems for a large spectrum of industrial systems [1], [2].

Because of the above reviewed literatures drawback of different various speed control nowadays industrial application is move toward adjustable speed drives, hence this thesis work focus on cascaded multilevel inverter for the Adjustable speed control of closed loop three phase squirrel cage induction motor drives. Three-phase squirrel cage rotor induction motors are widely used in industrial drives because they are rugged, reliable and economical.. The rotor of the slip ring motor has a cylindrical core with parallel slots, and each slot consists each bar. The slot of the squirrel cage motor is not parallel to each other. The slip ring motor is also called phase wound rotor. The construction of the slip-ring motor is complicated because it consist slip ring and brushes whereas the construction of the squirrel cage motor is simple. The phase wound motor consists external resistance circuit, whereas in squirrel cage motor it is not possible to add any external resistance circuit because their rotor bars are permanently slotted. For starting the slip ring motor the rotor resistance starter is used, whereas the slip ring motor does not require any starter. The starting torque of the slip-ring motor is high, whereas in squirrel cage motor it is low. The maintenance cost of the slip ring motor is high as compared to squirrel cage motor because the slip ring motor consists brushes and rings. The copper loss is more in slip ring motor as compared to squirrel cage motor. The slip ring motor has brushes for transferring the power whereas the squirrel cage motor is brushless. The copper loss in the phase wound

motor is high as compared to squirrel cage motor. The efficiency of the slip ring motor is low whereas the squirrel cage motor has high efficiency. The speed of the phase wound motor is controlled by using the resistance circuit. It is impossible to control the speed of the squirrel cage motor. The slip ring motor has low power factor as compared to squirrel cage motor. The cost of the phase wound rotor is high because it consists brushes. The squirrel cage motor is cheap. The starting current of the phase wound rotor is low because it is controlled by resistance circuit whereas it is high in squirrel cage motor. The phase wound motor is mostly used in places where high starting torque is required like a hoist, cranes, etc. The squirrel cage motor is used in a drilling machine, lathe machine, etc [33]. In general, because of the above reviewed literature merits this thesis work focus on the speed control of three-phase squirrel cage induction motor in closed loop drives system control.

Synchronous speed

An AC motor's synchronous speed, n_s , is the rotation rate of the stator's magnetic field, which is expressed in revolutions per minute as

$$n_s = \frac{120 \times f}{P} \quad (2.1)$$

Where f is the motor supply's frequency in Hertz and P is the number of magnetic poles.

Slip

Slip, s , is defined as the difference between synchronous speed and operating speed, at the same frequency, expressed in rpm or in percent or ratio of synchronous speed. Thus

$$S = \frac{n_s - n_r}{n_s} \quad (2.2)$$

Where n_s is stator electrical speed, n_r is rotor mechanical speed. Slip, which varies from zero at synchronous speed and 1 when the rotor is at rest, determines the motor's torque. Since the short-circuited rotor windings have small resistance, a small slip induces a large current in the rotor and produces large torque. At full rated load, slip varies from more than 5% for small or special purpose motors to less than 1% for large motors.

$$n_r = n_s(1 - S) \quad (2.3)$$

Hence slip plays an essential role in induction motor speed control. As we know, the slip speed is the difference between the synchronous and the rotor speed of induction motor (2.4).

$$S = \frac{\omega_s - \omega_r}{\omega_s} \quad (2.4)$$

Therefore emf (e_2) induces in the rotor because of relative motion, or we can say the slip speed of the motor. So,

$$e_2 \propto n_s - n_r \quad (2.5)$$

The rotor current (i_2) is directly proportional to the induced emf.

$$i_2 \propto e_2 \quad (2.6)$$

The torque (T) is directly proportional to the rotor current.

$$T \propto i_2 \quad (2.7)$$

Therefore,

$$T = K (n_s - n_r) \text{ or } K n_s \left(\frac{n_s - n_r}{n_s} \right) \text{ or } T = K_1 S \quad (2.8)$$

Hence, torque is directly proportional to the slip.

$$T \propto S \quad (2.9)$$

The equation (2.9) shows that the torque induces on the rotor are directly proportional to the slip of the induction motor. The high value of slip induces the emf in the rotor. This EMF develops the heavy torque on the rotor conductors. The value of the slip is adjusted by considering the load on the motor. For full-load, the high value of torque is required. This can be achieved by increasing the amount of the slip and reducing the speed of the rotor. The slip of the motor is kept low when the induction motor is running at no-load. The small slip produces the small torque on the motor [35].

2.2 Introduction to Inverters

A device that converts dc power into ac power at desired output voltage and frequency is called an inverter. The main applications of inverters are uninterruptable power supply, speed adjustment in ac drives, HVDC transmission lines.

Recent advances in the power handling capabilities of static switch devices such as IGBTs with higher voltage rating has made the use of voltage inverter feasible for high power applications. Multilevel pulse width modulation inverter topologies have drawn tremendous interest in the power industry since it can provide the high power application. The unique structure of multilevel inverters allows them to operate at high voltages without switching devices connected in series. The inverter is also capable to operate at megawatt power level, with low distortion and low dv/dt stress [23].

Several industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system for a high power application [11-12].

The concept of multilevel converters has been introduced since 1975 [13]. The term multilevel began with the three-level converter. Subsequently, several multilevel converter topologies have been developed. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected [15-22].

2.3 Need for multilevel inverters

The need of multilevel converter is to give a high output power from medium voltage source. Sources like batteries, super capacitors, solar panel are medium voltage sources, and hence the squirrel cage IM run on AC power, there should be a conversion from DC to AC by a power converter. Inverters are employed to do this conversion. The simplest topology that can be used for this conversion is the two-level inverter that uses four switches. Each switch needs an anti-parallel diode, so there should be also four anti parallel diodes. There are also other topologies for inverters. A multilevel inverter is a power electronic system that synthesizes a sinusoidal voltage output from several DC sources. These DC sources can be fuel cells, solar cells, ultra capacitors, etc. The main idea of multilevel inverters is to have a better sinusoidal voltage and current in the output by using switches. Many switches are put in series and the switching angles are important in the multilevel inverters because all the switches should be switched in such a way that the output voltage and current have low harmonic distortion [16].

Basically, the THD will be decreased by increasing the number of levels. It is obvious that an output voltage with low THD is desirable, but increasing the number of levels involves more complexities like more hardware and a more complicated control strategy. Choosing an inverter model with various levels is an optimum selection between price, weight, complexity and a very good output voltage with lower THD [6].

2.4 Introduction to multilevel inverters (MLI)

The voltage source inverters produce an output voltage or a current with levels either 0 or $\pm V_{dc}$. They are known as the three-level inverter. To obtain a quality output voltage or a current waveform with a minimum amount of ripple content, they require high-frequency along with various pulse width modulation strategies. In high-power and high-voltage applications, these two-level inverters, however, have some limitations in operating at high frequency mainly due to switching losses and constraints of device ratings.

In such cases we prefer for Multilevel Inverters. MLI's are well suited for high power, high voltage applications; the structure of MLI's is used to synthesize a near sinusoidal voltage from several levels of dc voltages. As the number of levels increases, the synthesized output waveform has more steps, which produce a staircase wave that approaches a desired waveform and the harmonic distortion of the output waveform decreases, approaching zero as the number of levels increases [18, 19].

2.5 Types of multilevel inverters

Multilevel inverters are of three types, namely:

- Diode clamped multilevel inverter
- Flying capacitor multilevel inverter
- Cascaded H-bridge multilevel inverter

2.5.1 Diode clamped multilevel inverter

A diode clamped multilevel inverter was one of the first inverters ever used. This inverter topology is as shown in figure 2.4 below. The diode-clamped inverter provides multiple voltage levels through connection of the phases to a series bank of capacitors. According to the original invention, the concept can be extended to any number of levels by increasing the number of capacitors. Early descriptions of this topology were limited to three-levels where two capacitors are connected across the dc bus resulting in one additional level.

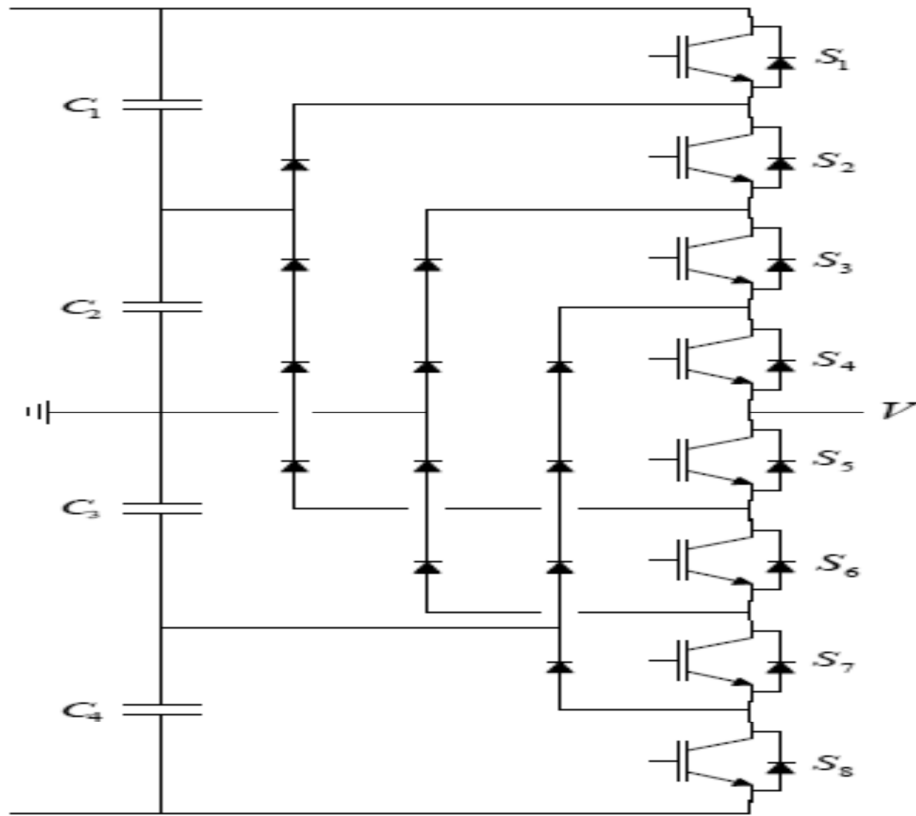


Figure 2.1 Structure of diode clamped multilevel inverter [38]

The additional level was the neutral point of the dc bus, so the terminology neutral point clamped (NPC) inverter was introduced. However, with an even number of voltage levels, the neutral point is not accessible, and the term multiple point clamped (MPC) is sometimes applied. Due to capacitor voltage balancing issues, the diode-clamped inverter implementation has been mostly limited to the three-level. Because of industrial developments over the past several years, this inverter topology has faded out of extensive use. The advantages of the diode clamped multi-level inverter are as large number of levels results in a small harmonic distortion. All phases share same DC bus, the control method is relatively simple and interconnection of two diode clamped multilevel inverters back-to-back with a DC capacitor link is suitable for applications like unity power factor control, frequency changer, phase shifter, etc. however excessive clamping diodes $(n-1)$ $(n-2)$ are required per phase. Reactive power flow is difficult because of capacitors imbalance. Maximum output voltage in the output is half of the DC source (this problem can be solved by cascading two diode clamped multilevel inverters) [28].

2.5.2 Flying capacitor multilevel inverter

Another fundamental multilevel topology, the flying capacitor, involves series connection of capacitor clamped switching cells. This topology has several unique and attractive features when compared to the diode-clamped inverter. One feature is that added clamping diodes are not needed. Furthermore, the flying capacitor inverter has switching redundancy within the phase which can be used to balance the flying capacitors so that only one dc source is needed. A conventional 5-level flying capacitor model is as shown in next page in Figure 2.3.

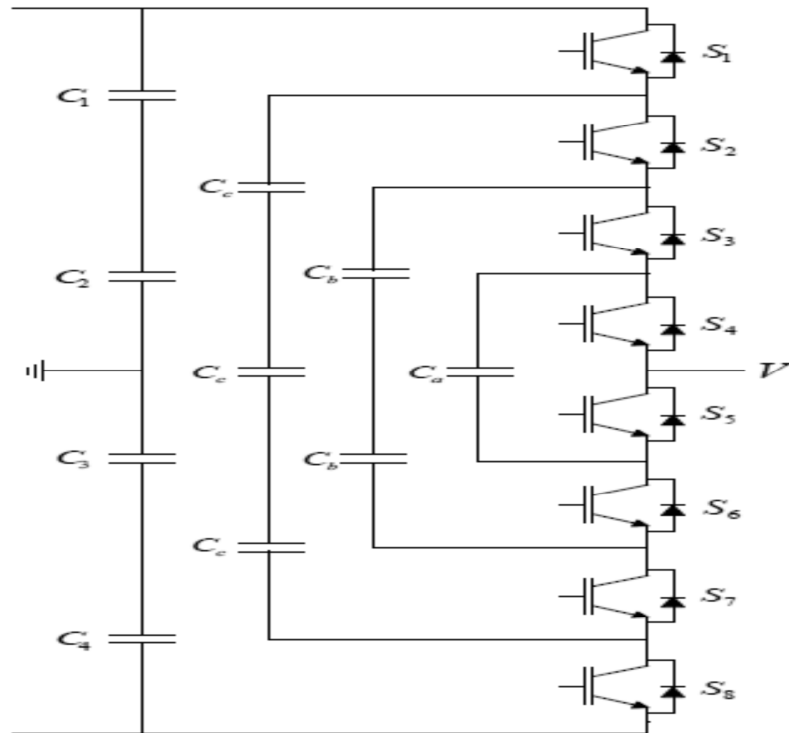


Figure 2.2 Structure of flying capacitor multilevel inverter [38]

This model is capable of solving capacitor voltage unbalance problem and excessive diode count requirement in DCMI. An n level inverter needs $2(n-1)$ switching devices, $(n-1)(n-2)/2$ balancing capacitors per phase & $(n-1)$ main DC bus capacitors. The advantages of the flying capacitor multi-level inverter, it provide switch combination redundancy for balancing different voltage levels. Similar to diode - clamp inverter with more levels, the harmonic content is low enough to avoid the need of filters and both real and reactive power flow can be controlled. But his topology has results in an excessive number of storage capacitors are required when the number of levels is high, high level inverters are more difficult to package with the bulky power capacitors and are more expensive too. The

inverter control can be very complicated, and the switching frequency and switching losses are high during practical applications for high power transmission [36].

2.5.3 Cascaded H-bridge multilevel inverter

The concept of this inverter is based on connecting H-bridge inverters in series to get a sinusoidal voltage output. The output voltage is the sum of the voltage that is generated by each cell. The number of output voltage levels are $2n+1$, where n is the number of cells. The switching angles can be chosen in such a way that the total harmonic distortion is minimized. An n level cascaded H-bridge multilevel inverter needs $2(n-1)$ switching devices where n is the number of the output voltage level [27].

A schematic diagram of a cascade m, d H-bridge inverter is as shown in Figure 2.3 below:

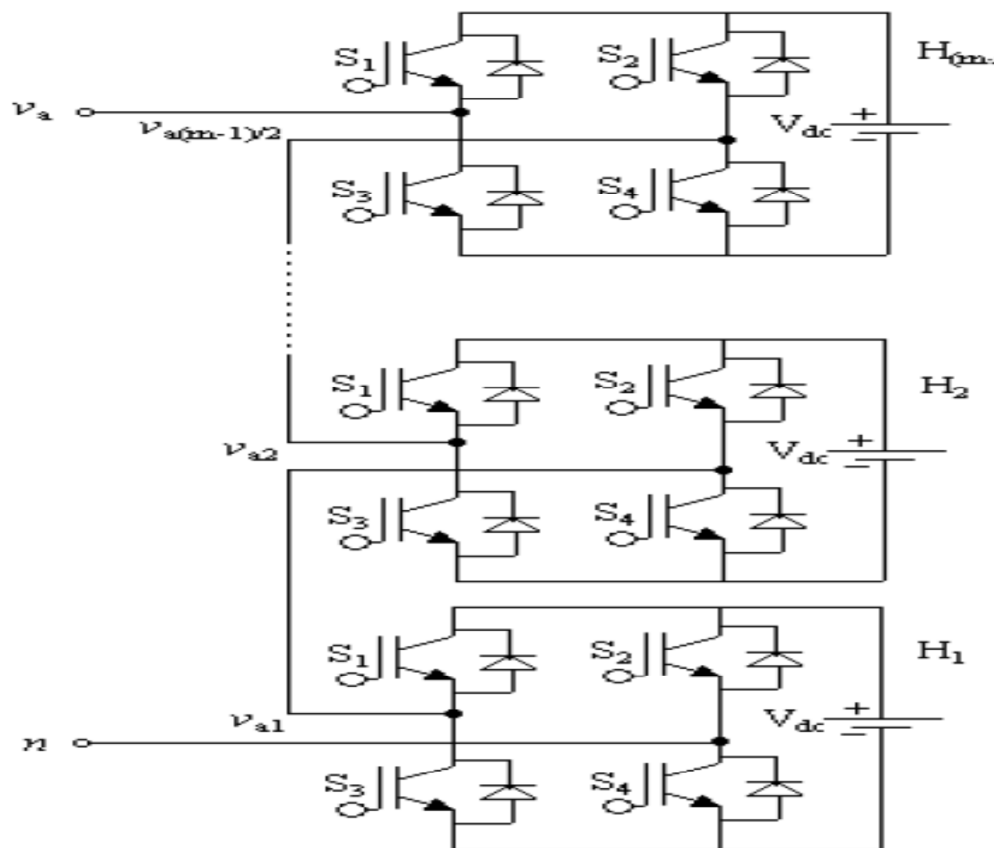


Figure 2.3 Cascaded H-bridge multi-level inverter

The advantage of the cascaded H-bridge multi-level inverters has the simple architecture and the lowest component count, the converter is very modular and easy to understand not only to its Structure, but also its control. For real power conversions from AC to DC and then DC to AC, the cascaded inverters need separate DC sources. The structure of separate DC sources is well suited for various renewable energy sources such as fuel cell,

photovoltaic and biomass. However, there is only limited access to DC bus capacitors, which limits its area of application to either those with only reactive power flow, or those where the power source or load can be both modular and isolated. It needs separate dc sources for real power conversions, thereby limiting its applications.

2.6 Comparison of the three multilevel inverter topologies

A comparative study of the above said inverter topologies can be represented by the following tabular column Table 2.1.

Table 2. 1 Comparison of the three multilevel inverter topologies

Inverter Configuration	Diode-Clamp	Flying-Capacitor	Cascaded-Inverter
Main switching devices	$2(n-1)$	$2(n-1)$	$2(n-1)$
Main diodes	$2(n-1)$	$2(n-1)$	$2(n-1)$
Clamping diodes	$(n-1)(n-2)$	0	0
DC bus capacitors	$(n-1)$	$(n-1)$	$(n-1)/2$
Balancing capacitors	0	$(n-1)(n-2)/2$	0

2.7 Introduction to Pulse Width Modulation

In many industrial applications, control of output voltage is often necessary to withstand with the variations of dc input voltage, to regulate voltage of inverters, to satisfy the constant volts and frequency control requirement. There are various techniques to vary the inverter gain .The most efficient method of controlling the gain is to incorporate PWM control within the inverters .The commonly used techniques for single phase inverters are:

- Single-pulse -width modulation
- Multiple-pulse-width modulation
- Sinusoidal pulse-width modulation

And for three phase inverters are:

- Sinusoidal pulse width modulation

2.8 The Carrier Based Modulation Schemes of Multilevel Inverters

The carrier based modulation schemes for multilevel inverters can be generally classified into two categories:

- Phase-Shifted Carrier Based Modulation and
- Level-Shifted Carrier Based Modulation

Both modulation schemes can be applied to the cascaded multilevel inverters.

2.8.1 Phase-Shifted Carrier Based Modulation

A multilevel inverter with m voltage levels requires $(m-1)$ triangular carriers. In phase shifted multicarrier modulation, all the triangular carriers have the same frequency and the same peak-to-peak amplitude, but there is phase shift between any two adjacent carrier waves, it's given by:

$$\Phi_c = \frac{360^\circ}{(m-1)} \quad (2.3)$$

Where:

m = multilevel inverter with m voltage levels

Φ_c = phase shift angle between any two adjacent carrier waves

2.8.2 Level-Shifted Carrier Based Modulation

Similar to the phase shifted modulation, an m -level cascaded multilevel inverter level shifted multicarrier modulation schemes requires $(m-1)$ triangular carriers, all having the same frequency and amplitude. The $(m-1)$ triangular carrier is vertically disposed such that the bands they occupy are contiguous. The frequency modulation index is given by equation (2.4), which remains the same as that for the phase shifted modulation scheme whereas the amplitude modulation index is defined as in equation (2.3).

$$m_f = \frac{f_c}{f_m} \quad (2.4)$$

$$m_a = \frac{v_m}{v_c} \quad (2.5)$$

$$\text{for } 0 \leq m_a \leq 1$$

Where:

m_f = frequency modulation index

f_c = carrier frequency

f_m = frequency of modulating waves.

m_a = amplitude modulation index

v_m = peak amplitude of voltage

v_c = peak carrier voltage

THD of phase-shifted modulation is much higher than level-shifted modulation [30]. Therefore, the modulation schemes of this thesis are considered level shifted modulation. An m cascaded multilevel inverter using level-shifted multicarrier modulation scheme requires $(m-1)$ triangular carriers, all having the same frequency and amplitude. The $(m-1)$

triangular carriers are vertically disposed such that the bands they occupy are contiguous. There are three alternative PWM strategies with different phase relationships for the level-shifted multicarrier modulation:

- In-phase disposition (IPD), where all carrier waveforms are in phase.
- Phase opposition disposition (POD), where all carrier waveforms above zero reference are in phase and are 180° out of phase with those below zero.
- Alternate phase disposition (APOD), where every carrier waveform is in out of phase with its neighbor carrier by 180° . Hence the THD value of IPD is less comparing to the rest above two PWM techniques for the level shifted multicarrier modulation in phase disposition PWM techniques is considered for this thesis work [30].

Comparison between phase shifted and level shifted PWM Schemes

To compare the performance of the phase and level shifted modulation schemes, it is assumed that the average switching frequency of the solid state device is the same for both schemes.

Table 2. 2 comparison between the phase and level shifted PWM schemes [29]

Comparison	Phase Shifted Modulation	Level Shifted Modulation (IPD)
Device switching frequency	Same for all devices	Different
Device conducting Period	Same for all devices	Different
Rotating of switching pattern	Not required	Required
Line-to-line voltage THD	Good	Better

Single Pulse Modulation

In single pulse width modulation control ,there is only one pulse per half cycle and the width of the pulse is varied to control the inverter output voltage .The gating signals are generated by comparing a reference signal of amplitude V_r , with a carrier wave of amplitude V_c . The frequency of the reference signal determines the fundamental frequency of output voltage. As the semiconductor devices receive only one pulse during half cycle, one semiconductor devices is switched on. The output voltage of the inverter can be controlled by controlling width of pulse. This will control the output voltage of the inverter and the frequency of the output voltage depends upon frequency of reference signal [7].

Multiple Pulse Width Modulation

There is more than one pulse per half cycle in the multiple width modulation. These gate pulses are used to control output voltage of the inverter as well as reduce harmonics. The magnitude and width of the pulses are equal in this method. The reference signal and higher frequencies carrier signal are compared in this method in order to generate more than one gating pulses. The number of gate pulses depends upon carrier frequencies of whereas the output voltage depends frequencies of reference signal. Figure 2.5 illustrate the multiple pulse width modulation techniques as follow.

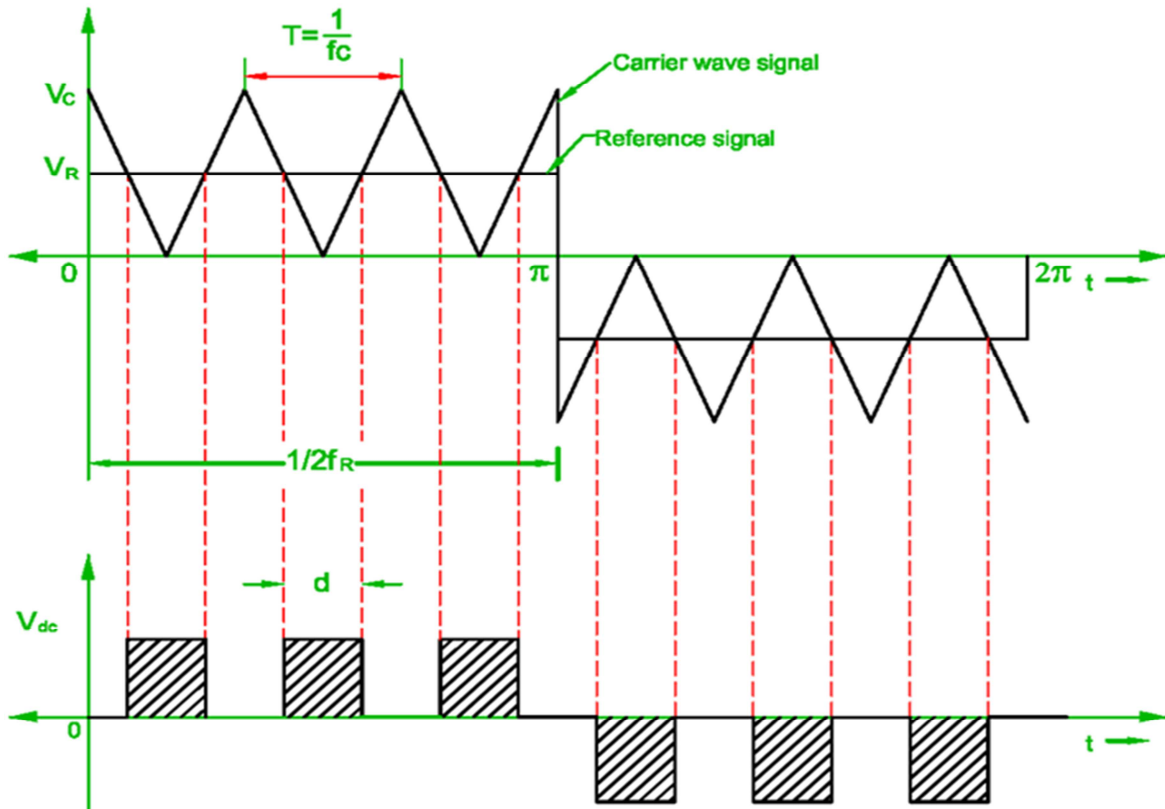


Figure 2.4 Multiple Pulse Width Modulation

From figure 2.4

Carrier frequency = f_c in Hz

Reference frequency = f_R in Hz

$$\frac{1}{f_c} = \frac{\pi}{3} \quad (2.6)$$

$$T_c = \frac{\pi}{3}$$

Or

Similarly

$$\frac{1}{2f_R} = \frac{1}{\pi} \quad (2.7)$$

Or

$$T_R = \frac{1}{\pi}$$

$$T_R = \pi/2$$

There number of the pulses per half cycle

N_p =Length of the half cycle reference signal /Length of one cycle Triangular waveform

$$\begin{aligned} N_p &= \frac{1}{2f_R} / \frac{1}{f_c} \\ &= \frac{f_c}{2f_R} \end{aligned} \quad (2.8)$$

$$\begin{aligned} \text{Number of generated pulses } N_p &= \frac{3}{\pi} * \pi \quad [\text{from equation (2.6) and (2.7)}] \\ &= 3 \end{aligned}$$

As the number of pulses increases in each half cycle, lower order harmonics reduces but higher order harmonics increases. The higher order harmonics are reduced by using filter. It is to be noted that the switching losses of the semiconductor increase as there are more number of pulses per half cycle. This modulation technique is also called symmetrical modulation control.

Sinusoidal pulse-width modulation

This is similar to that of the above mentioned method of the pulse generation by comparison of the triangular wave with that of the sine wave. But the main difference is the generation of the triangular waves. The amplitude of the triangular is changed depending on the required switching sequence keeping the sine wave amplitude constant.

The reference signal is taken as sinusoidal waveform whereas the carrier signal is taken as triangular waveform in this method. The width of the pulse in the SPWM is not equal due to reference signal is taken as sinusoidal waveform. The amplitude of sinusoidal waveform is not constant. The width of gate pulse is determined by intersect point of the sinusoidal waveform and triangular waveform. The frequency of the inverter output voltage depends upon frequency of reference signals f_R and amplitude of the reference signals V_R controls

the modulation index (M). The number of pulses per half cycle when the amplitude of triangular wave becomes maximum and sinusoidal waveform become zero.

$$N_p = \frac{f_c}{2f_R} \quad 2.9$$

Where

$$f_c = \text{carrier wave frequency} = \frac{3}{\pi}$$

$$f_R = \text{Reference wave frequency} = \frac{1}{2\pi}$$

Therefore

$$\begin{aligned} N_p &= \frac{3}{\pi} * \frac{2\pi}{2} \\ &= 3 \end{aligned} \quad 2.10$$

The number of pulses per half cycle when the amplitude of triangular waveform and sinusoidal become zero at same time.

$$\begin{aligned} N_p &= \frac{f_c}{2f_R - 1} \\ &= 2 \end{aligned} \quad 2.11$$

$$\text{The modulation index} = \frac{V_R}{V_C}$$

The analysis of harmonic is done in the sinusoidal PWM control is below. When the value of modulation index is less than one, the maximum harmonic number in the output voltage is:

$$\frac{f_c}{f_R} \pm 1$$

Or

$$2N_p \pm 1$$

Where N_p = Number of pulses per half cycle

As the number of pulses per half cycle increases, the higher order harmonics also increases. Let $N_p = 3$, it will generate will generate 5th harmonic and 7th harmonic but higher order harmonics are easily filtered out. As the number of pulses increases per half cycle, the switching losses also increase and it affects the efficiency of the inverter. When the modulation index is greater than one, lower order harmonics reduces in the output of the inverter.

Multilevel inverter based SPWM speed control is the most advantages for industrial and domestic applications because of its Adjustable Speed Drives (ASDs), reduction of Electromagnetic interference and less THD comparing to the rest. Thus in areas where precision is required, Multilevel inverter based SPWM speed control used. The various advantages multilevel inverter based SPWM speed control is as follows:

- It gives good running and transient performance.
- Reduce harmonic
- No need to filter circuits
- It has low starting current requirement.
- It has a wider stable operating region.
- Voltage and frequencies reach rated values at base speed.

Voltage or current converters generate discrete output waveforms which led the use of machines with special isolation and in some applications large inductances connected in series with the respective load. The distorted voltages and currents waveforms produce harmonic distortion additional power losses, and high frequency noise that can affect not only the power load but also the associated controllers [3], [6].

All these unwanted operating characteristics associated with PWM converters could be overcome with multilevel converters in addition to the fact that higher voltage levels can be achieved. The poor quality of output current and voltage of an induction motor fed by a classical two-level inverter is due to the presence of harmonics. The presence of significant amount of harmonics makes the motor to suffer from severe torque pulsations, especially at low speed, which manifest themselves in cogging of the shaft [3], [7]. It will also causes undesired motor heating and Electromagnetic interference. The reduction in harmonics calls for large sized filters, resulting in increased size and the cost of the system. Nowadays multilevel inverters are the promising alternative and cost effective solution for high voltage and high power applications including power quality and motor drive problems. Multilevel structure allows raising the power handling capability of the system in a powerful and systematic way. The advancements in the field of power electronics and microelectronics made it possible to reduce the magnitude of harmonics with multilevel inverters, in which the number of levels of the inverters are increased rather than increasing the size of the filters. The performance of multilevel inverters enhances as the number of levels of the inverter increases [1, 2, 4].

CHAPTER THREE

METHODOLOGY AND SYSTEM DESIGN

The methodology of this thesis work involves a number of different tasks that are performed to lead towards completion. This is followed by the literature review where all the theoretical information regarding the component multilevel inverter and Mathematical calculation such the speed of the motor, torques and so on. Design of the project will be implemented by using MATLAB R2013a/SIMULINK software for simulate the result.

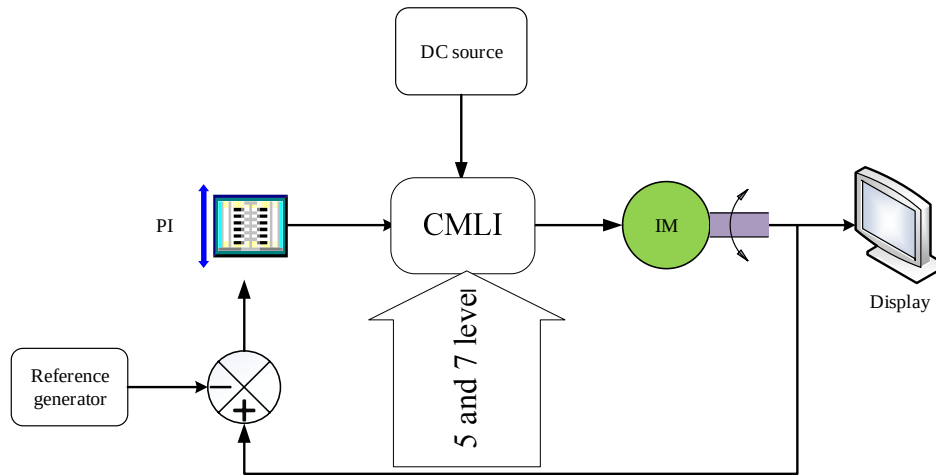


Figure 3.1 Block diagram for induction motor with closed loop speed control

According to the above block diagram the DC source given to the three phase H-bridge, which followed by Signal generator PWM techniques. The overall completed CML inverter is fed the induction motor drive, such a way that the speed of induction motor is controlled by using PI controller control by comparing actual speed of the motor with respect the set value or reference generator. The compilation methodology of the research is discussed as follow by using MATLAB R2013a software as tools.

3.1 MATLAB Implementation of Sinusoidal Pulse width Modulation (SPWM)

The MATLAB® high-performance language for technical computing integrates computation, visualization, and programming in an easy-to-use environment where problems and solutions are expressed in familiar mathematical notation. Simulink software models, simulates, and analyzes dynamic systems. It enables you to pose a question about a system, model the system, and see what happens. With Simulink, you can easily build models from scratch, or modify existing models to meet your needs. Simulink supports linear and nonlinear systems, modeled in continuous time, sampled time, or a hybrid of the two. The Sinusoidal pulse width modulation is generated by using Simulink block in such

a way that by comparing the fundamental frequency with that carrier it generates the gate signals. This circuit consists of the sine generator block, triangular generator block, logical comparator and they are connected as shown in the Figure 3.1.

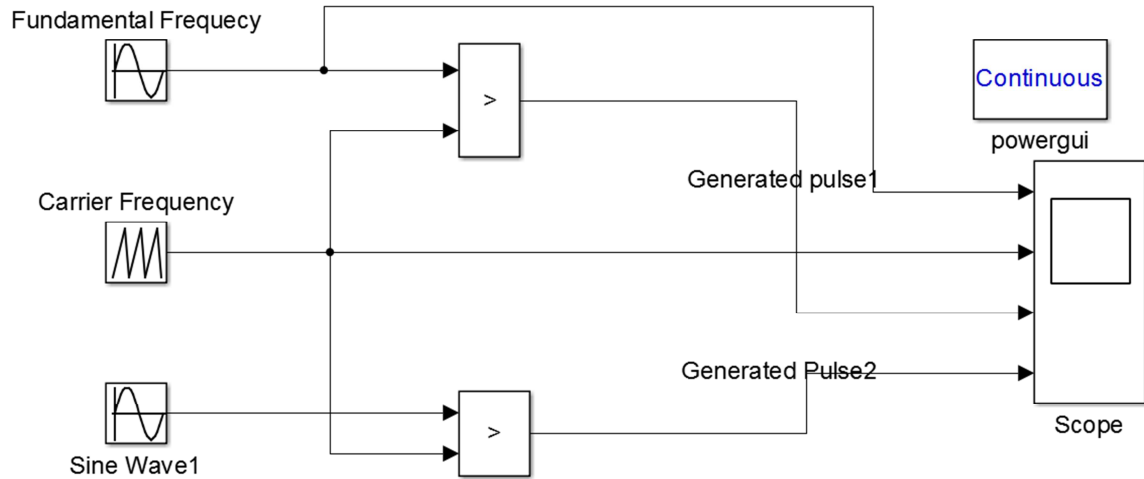


Figure 3.2 Simulation circuit of the sinusoidal pulse width modulation technique

In the above simulation circuit one of the sine wave is a phase shift of 0° where the other sine block is with a phase shift of 180° . The triangular block is common one which gives the carrier frequency for the generation of pulse1 and pulse 2 shown in the Figure 3.1. The output waveform of this circuit is shown in Figure 4.1.

3.2 Metal Oxide Field Effect Transistor (MOSFET)

The metal–oxide–semiconductor field-effect transistor (MOSFET, MOS-FET, or MOS FET) is a transistor used for amplifying or switching electronic signals. Although the MOSFET is a four-terminal device with source (S), gate (G), drain (D), and body (B) terminals, the body (or substrate) of the MOSFET often is connected to the source terminal, making it a three-terminal device like other field-effect transistors. Because these two terminals are normally connected to each other (short-circuited) internally, only three terminals appear in electrical diagrams. The MOSFET is by far the most common transistor in both digital and analog circuits, though the bipolar junction transistor was at one time much more common [25].

Metal- oxide- semiconductor field effect transistors require the continuous application of a gate-source voltage of appropriate magnitude in order to be in the on state. No gate current flows except during the transitions from on to off or vice versa when the gate capacitance is being charged or discharged. The switching times are very short, being in the range of a

few tens of nanoseconds to a few hundred nanoseconds depending on the device type. The on-state resistance $r_{DS(on)}$ of the MOSFET between the drain and source increases rapidly with the device blocking voltage rating. On a per-unit area basis, the on-state resistance as a function of blocking voltage rating BV_{DSS} , can be expressed as

$$r_{DS(on)} = kBV_{DSS}^{2.5-2.7} \quad 3.1$$

Where k is a constant that depends on the device geometry. Because of this, only devices with small voltage ratings are available that has low on-state resistance and hence small conduction losses.

$$P_S = \frac{1}{2} V_d I_o f_s (t_{c(on)} + t_{c(off)}) \quad 3.2$$

Where, P_S is switching power loss, V_d input voltage, I_o , entire current, f_s device switching frequency and t_c is conduction time. This is an important result because it shows that the switching power loss in a semiconductor switch varies linearly with the switching frequency and the switching times. Therefore, if devices with short switching times are available, it is possible to operate at high switching frequencies in order to reduce filtering requirements and at the same time keep the switching power loss in the device from being excessive. However, because of their fast switching speed, the switching losses can be small in accordance with Eq. 3.2. From a total power loss standpoint, 300-400V MOSFETs compete with bipolar transistors only if the switching frequency is in excess of 30-100 kHz. However, no definite statement can be made about the crossover frequency because it depends on the operating voltages, with low voltages favoring the MOSFET. Metal- oxide semiconductor field effect transistors are available in voltage ratings in excess of 1000 V but with small current ratings and with up to 100 A at small voltage ratings [7], [36].

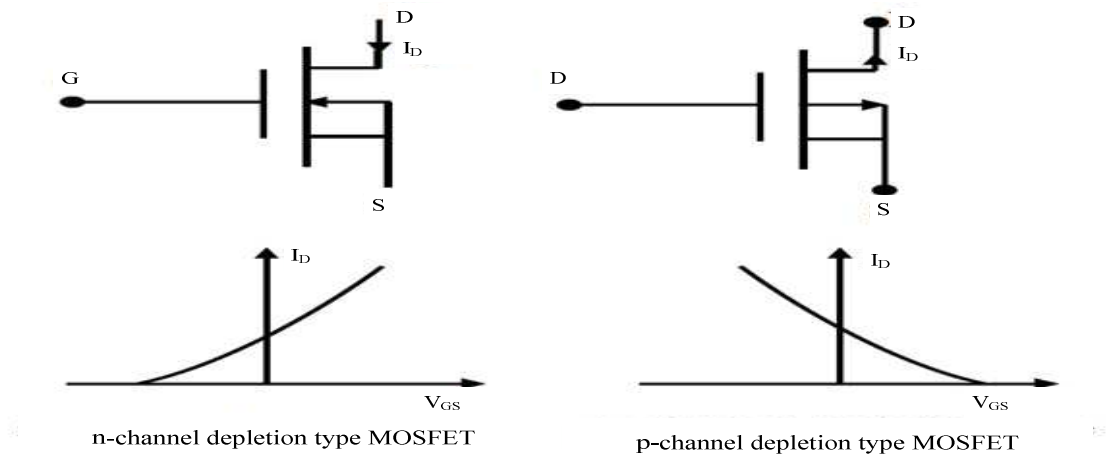


Figure 3.3 N-channel and P-channel depletion type MOSFET

From Figure 3.3 it can be concluded that depletion type MOSFETs are normally ON type switches i.e. with the gate terminal open a nonzero drain current can flow in these devices. This is not convenient in many power electronic applications.

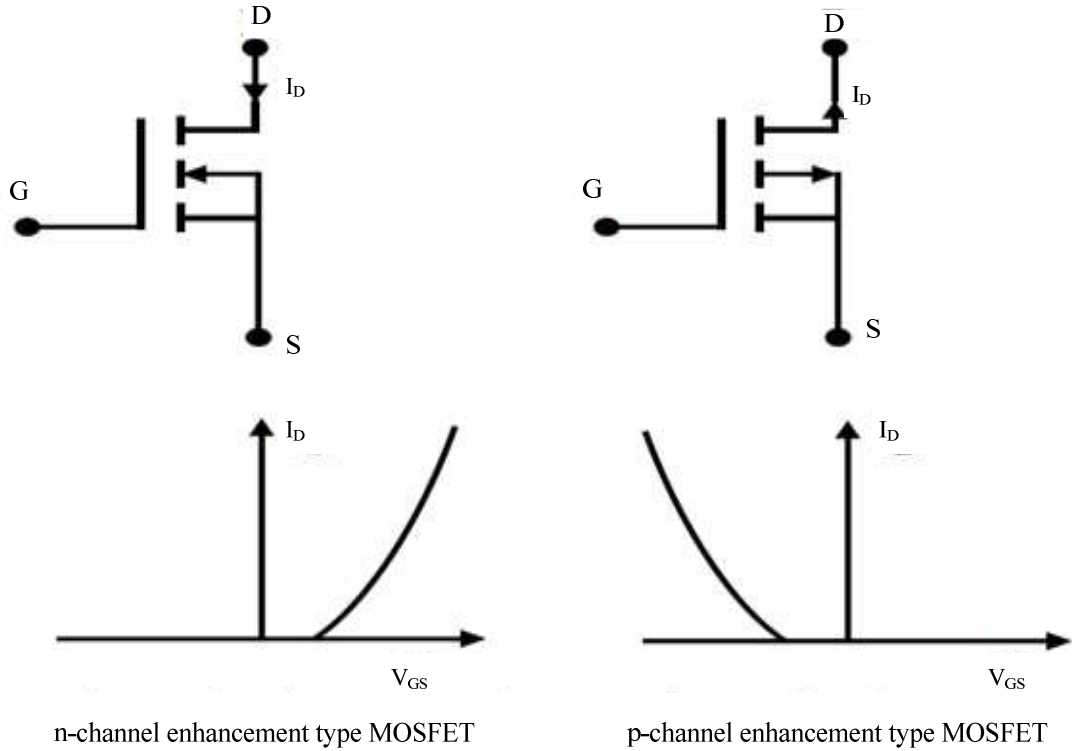


Figure 3.4 N-channel and P-channel enhancement type MOSFET

The enhancement type MOSFETs (particularly of the n-channel variety) is more popular for power electronics applications. This is the type of MOSFET is used for the design of cascaded multilevel inverter in this thesis work. Both "n-channel" and "p-channel" devices are being made, but the former are available in higher ratings because the electrons have a higher mobility than holes inside the silicon crystal.

The main advantage of a MOSFET is that it requires almost no input current to control the load current, when compared with bipolar transistors. In an enhancement mode MOSFET, voltage applied to the gate terminal increases the conductivity of the device. In depletion mode transistors, voltage applied at the gate reduces the conductivity [24], [37].

MOSFETs also have comparatively higher on state resistance per unit area of the device cross section which increases with the blocking voltage rating of the device. Consequently, the use of MOSFET has been restricted to low voltage (less than about 500 volts) applications where the ON state resistance reaches acceptable values. Inherently fast switching speed of these devices can be effectively utilized to increase the switching frequency beyond several hundred kHz.

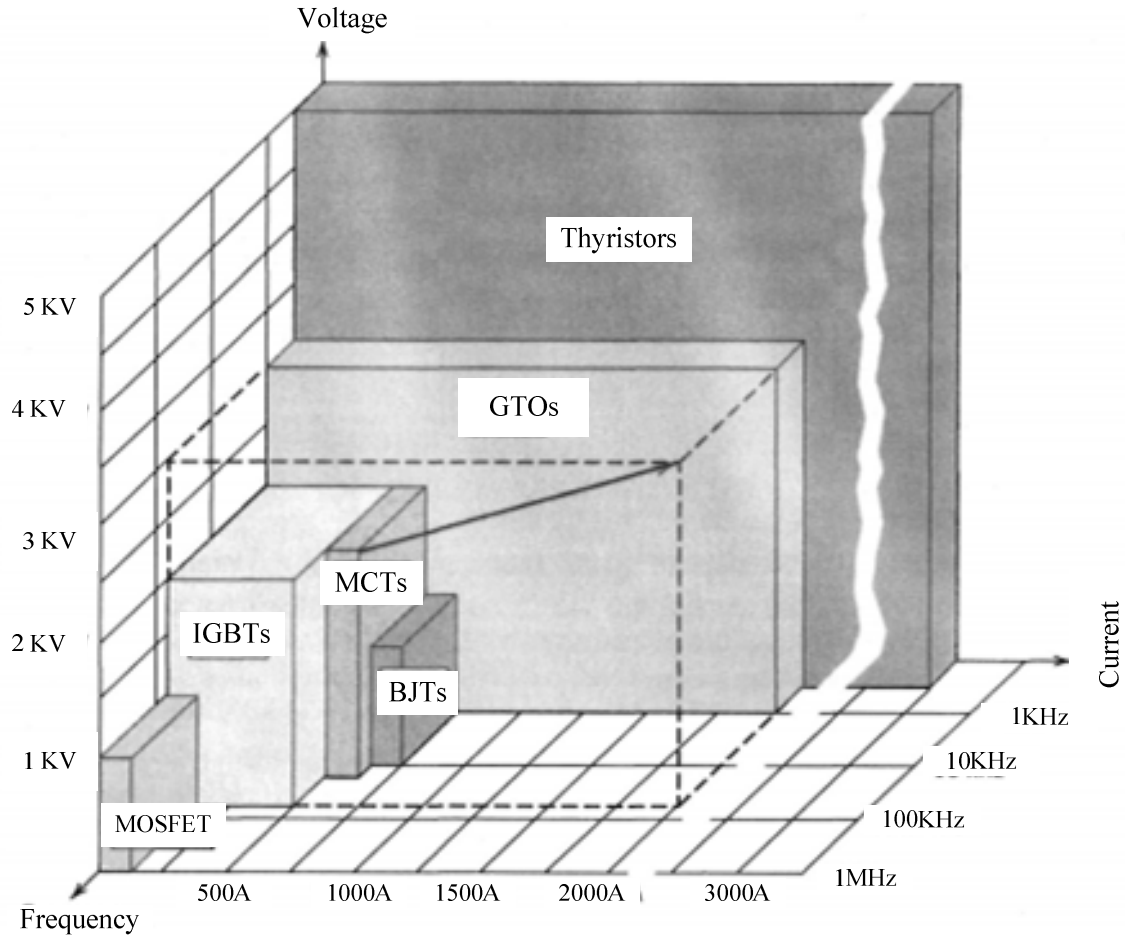


Figure 3.5 Summary of power semiconductor device capabilities.

3.3 MATLAB implementation of Three Phase Five CMLI Level Inverter

This circuit consists of 24 MOSFET's with 8 for each phase. These 8 MOSFET's are connected as H-bridge with two legs having two switches each. These two bridges are connected in series for a single phase as shown in the Figure 3.4

The waveform of one leg of cascaded H-bridge multilevel inverter of V_{AN} can be expressed in terms of Fourier series as

$$V_{AN} = \frac{4V_{DC}}{\pi} \sum_{n=1,3,5,7,\dots}^{\infty} \frac{1}{n} \{ \cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) \} \sin(n\omega t) \quad 3.1$$

$$\text{For } 0 \leq \theta_3 < \theta_2 < \theta_1 \leq \pi/2$$

Where n is the harmonic order, and θ_1, θ_2 and θ_3 are the independent switching angles. The coefficient $\frac{4V_{DC}}{\pi}$ represent the peak values of the maximum fundamental voltage $V_{H,Max}$ of an H-bridge cell, which occurs when switching angle θ_1 of v_{H1} for example , reduce to zero. The switching sequence is stated in table 3.1.

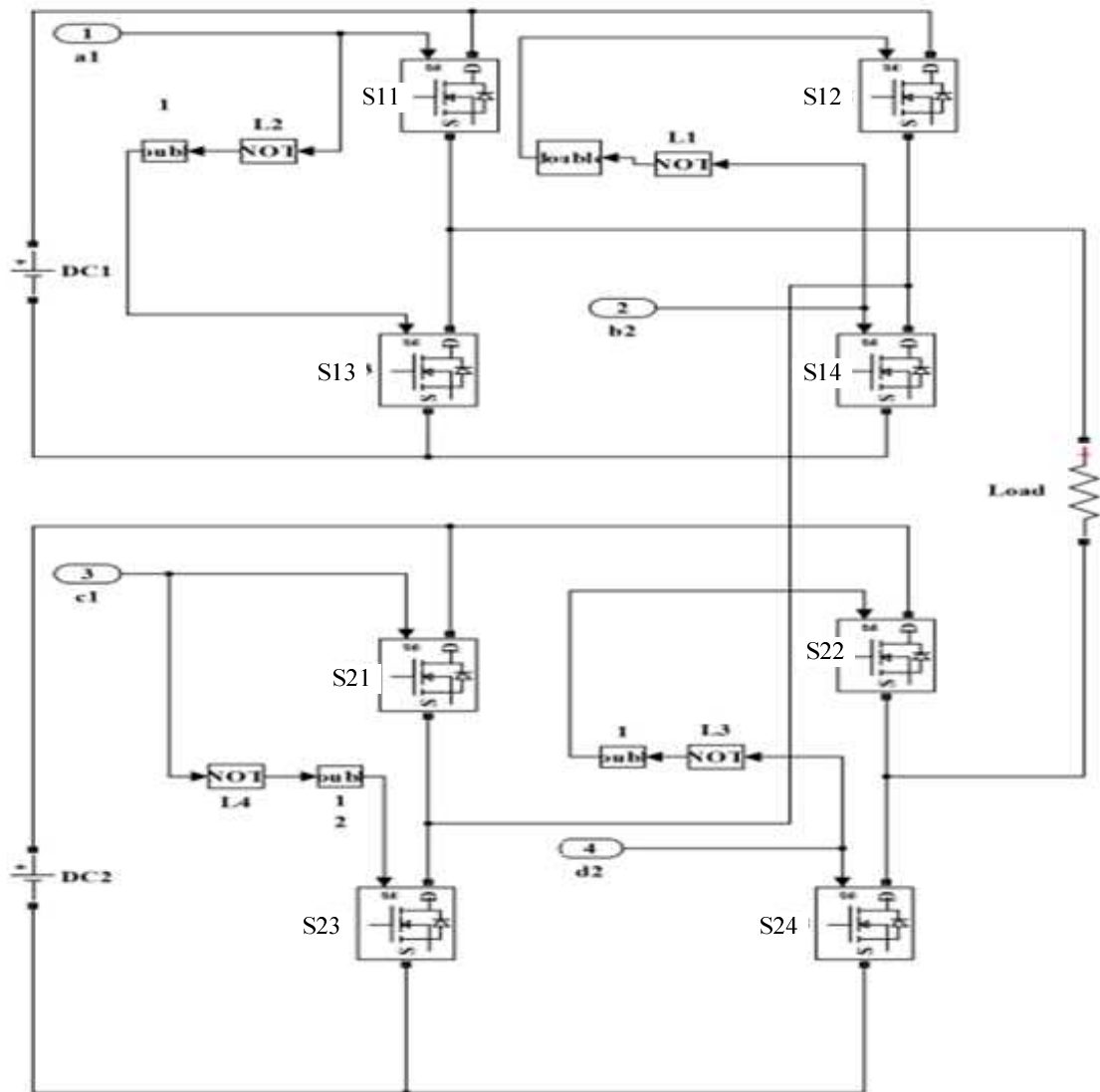


Figure 3.6. Cascaded H-bridge for single phase five level

Operation of Five Level Cascaded Multilevel Inverter

There are five different states of switching to produce the five level output. The switching operation is explained in the following table.

Table 3.1 Switching sequence of five level cascaded multilevel inverter

S11	S12	S13	S14	S21	S22	S23	S24	Output
On	Off	Off	On	On	Off	Off	On	2vdc
On	Off	Off	On	Off	Off	Off	Off	Vdc
On	Off	Off	On	Off	On	On	Off	0
Off	Off	Off	Off	Off	On	On	Off	-Vdc
Off	On	On	Off	Off	On	On	Off	-2vdc

3.4 MATLAB implementation of 3 Phase Seven CMLI Level Inverter

This circuit consists of 36 MOSFET's with 12 for each phase. These 12 MOSFET's are connected as H-bridge with two legs having two switches each. These three bridges are connected in series for a single phase as shown in the figure 3.5.

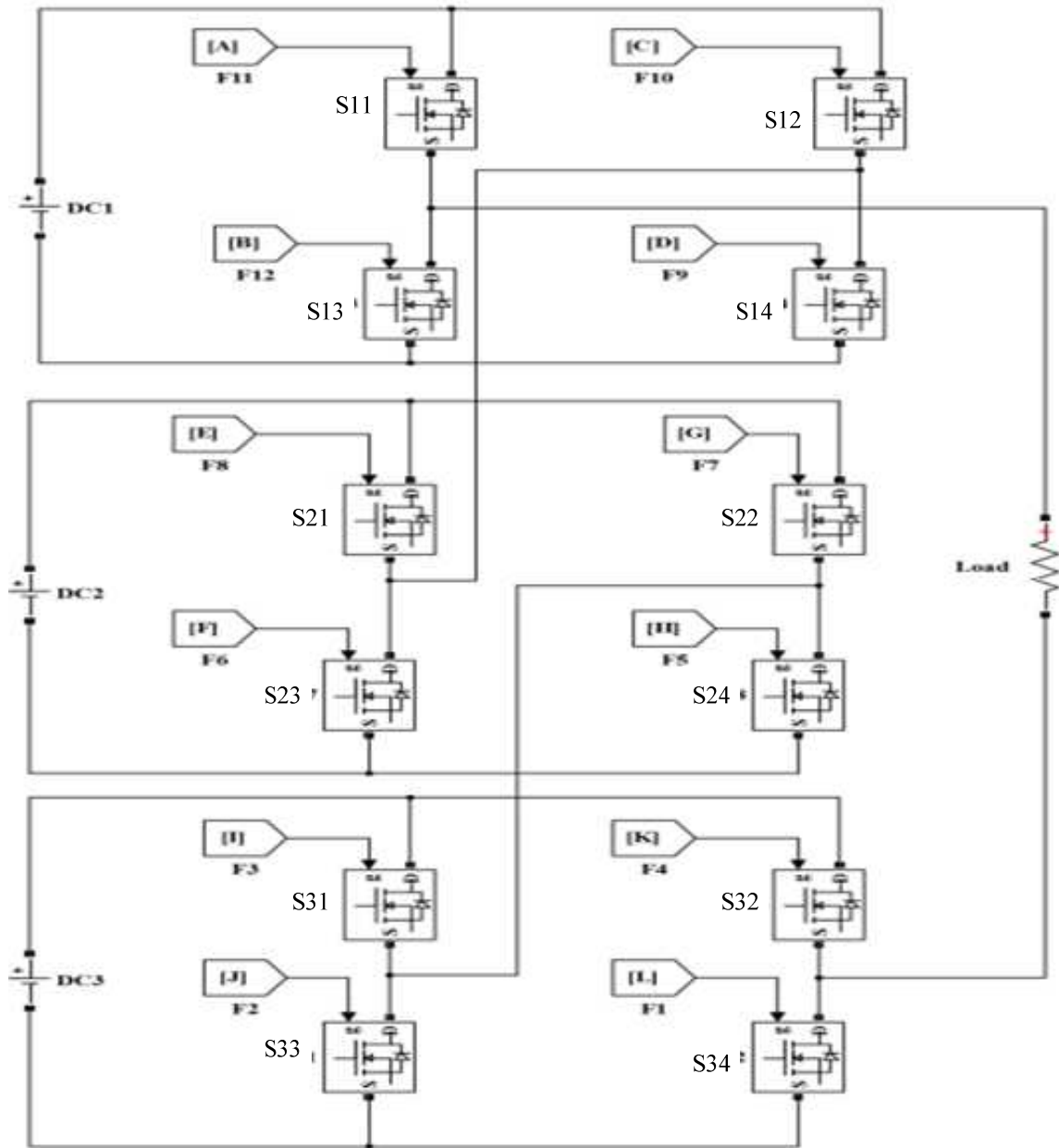


Figure 3.7. Cascaded H-bridge for single phase seven level

Operation of seven level cascaded multilevel inverter

There are seven different states of switching to produce the seven level output. The switching operation is explained in the following table.

Table 3. 2 Switching sequence of seven level inverter

S11	S12	S13	S14	S21	S22	S23	S24	S31	S32	S33	S34	Output
On	Off	Off	On	On	Off	Off	On	On	Off	Off	On	3vdc
On	Off	Off	On	On	Off	Off	On	Off	Off	Off	Off	2vdc
On	Off	Off	On	Off	Off	Off	Off	Off	Off	Off	Off	Vdc
On	Off	Off	On	Off	On	On	Off	Off	Off	Off	Off	0
Off	Off	Off	Off	Off	On	On	Off	Off	Off	Off	Off	-Vdc
Off	Off	Off	Off	Off	On	On	Off	Off	On	On	Off	-2vdc
Off	On	On	Off	Off	On	On	Off	Off	On	On	Off	-3vdc

3.5 PID Controller

A proportional–integral–derivative controller (PID controller) is a generic loop feedback (controller) widely used in industrial control systems – a PID is the most commonly used feedback controller. A PID controller calculates an "error" value as the difference between a measured process variable and a desired set point. The controller attempts to minimize the error by adjusting the process control inputs. Some applications may require using only one or two actions to provide the appropriate system control. This is achieved by setting the other parameters to zero. A PID controller will be called a PI, PD, P or I controller in the absence of the respective control actions. PI controllers are fairly common, since derivative action is sensitive to measurement noise, whereas the absence of an integral term may prevent the system from reaching its target value due to the control action. Hence the research uses the PI controller for adjustable speed control of three phase squirrel cage induction motor in this thesis work [32].

PID Controller theory:

The PID control scheme is named after its three correcting terms, whose sum constitutes the manipulated variable (MV). The proportional, integral, and derivative terms are summed to calculate the output of the PID controller. Defining $u(t)$ as the controller output, the final form of the PID algorithm is:

$$u(t) = MV(t) = K_p e(t) + K_i \int_0^t e(\tau) d\tau + K_d \frac{d}{dt} e(t)$$

Where:

K_p = Proportional gain, a tuning parameter

K_i = Integral gain, a tuning parameter

K_d =Derivative gain, a tuning parameter

e =Error =SP-PV

SP=Set Point

PV=Process Variable

t: Time or instantaneous time

Tuning Methods of PI Loop

There are several methods for tuning a PI loop. The most effective methods generally involve the development of some form of process model, and then choosing P, I, and D based on the dynamic model parameters. Manual tuning methods can be relatively inefficient, particularly if the loops have response times on the order of minutes or longer.

The choice of method will depend largely on whether or not the loop can be taken "offline" for tuning, and the response time of the system. If the system can be taken offline, the best tuning method often involves subjecting the system to a step change in input, measuring the output as a function of time, and using this response to determine the control parameters.

Ziegler–Nichols method:

The Ziegler–Nichols method, introduced by John G. Ziegler and Nathaniel B. Nichols in the 1940s. The K_i and K_d gains are first set to zero. The P gain is increased until it reaches the ultimate gain, K_u , at which the output of the loop starts to oscillate. K_u and the oscillation period P_u are used to set the gains as shown in table 3.3 [31].

Table 3.3 K_p, K_i, K_d values using Ziegler–Nichols method [31]

Ziegler–Nichols Method			
Control Type	K_p	K_i	$1K_d$
P	$0.50 K_u$	-	-
PI	$0.45 K_u$	$1.2 \frac{K_p}{P_u}$	-
PID	$0.60 K_u$	$2 \frac{K_p}{P_u}$	$\frac{K_p P_u}{8}$

3.6 MATLAB implementation of 3 Phase Five Level CMLI for Induction Motor

The modulating signal fed the control signal in order to generate the appropriate voltage level in the case five level cascaded multilevel inverter. The following diagram shows the MATLAB implementation of three-phase IM fed with five cascaded multilevel inverter for the case open loop speed control.

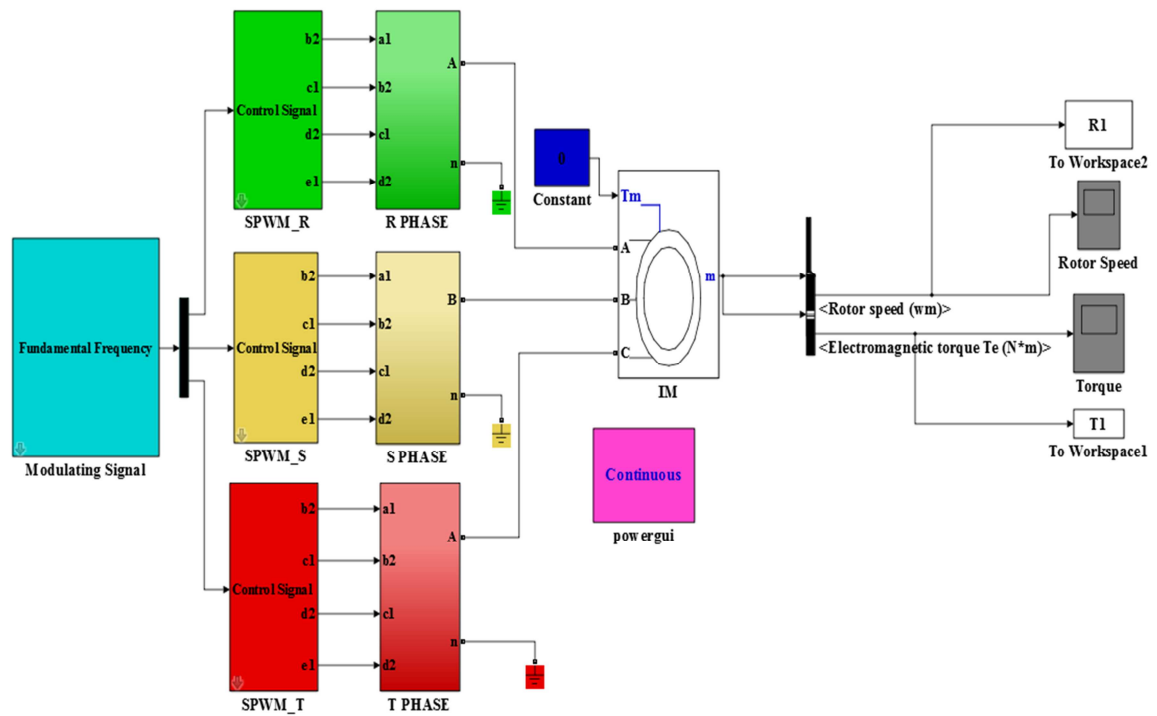


Figure 3.8 Three phase IM feed with open loop five CML inverter

The three-phase IM fed with five cascaded multilevel inverter in the case of open loop speed and torque response is shown in the figure 4.12 and figure 4.14. Each system block and their respective function in the system are described as follows.

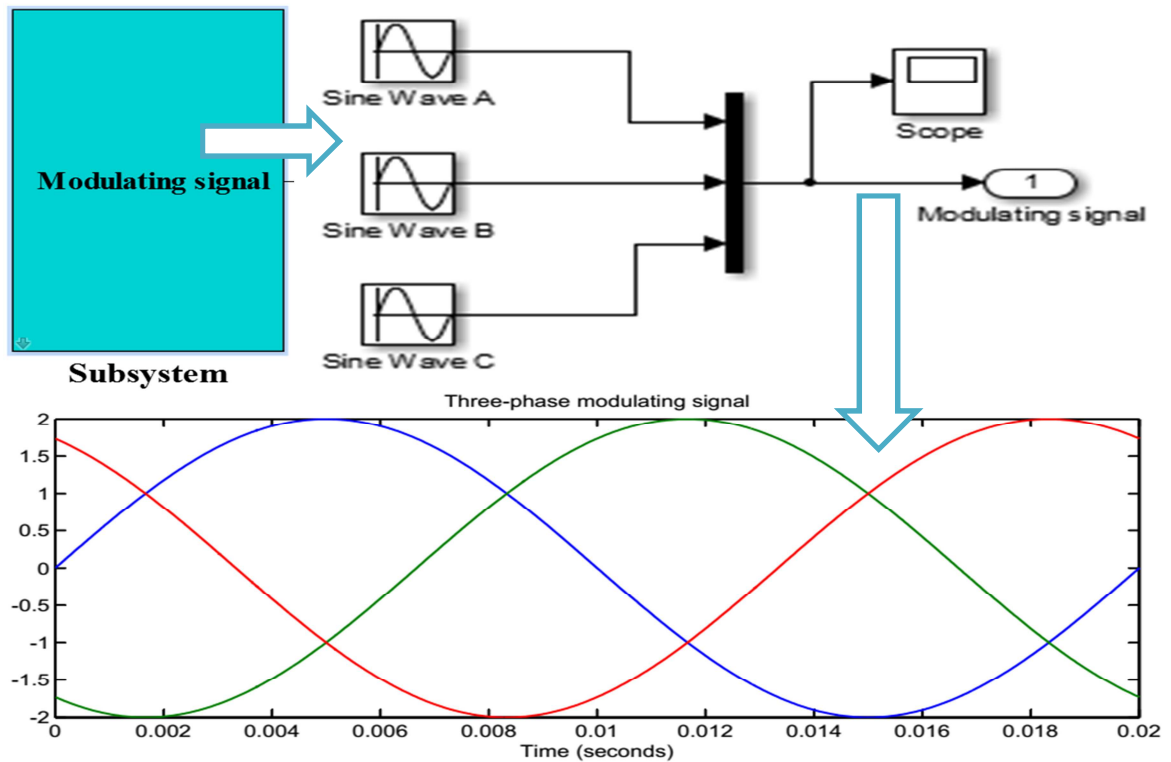


Figure 3.9 Description of modulating signal block and their out put

The modulating signal is given to the control signal. In such a way that the control signal is generate the pulse that given to the cascaded multilevel inverter for the case R_PHASE, S_PHASE and T_PHASE which is shown in the Figure 3.5. The main function of this subsystem is to producing the modulated signal from the fundamental frequency according to the firing angle.

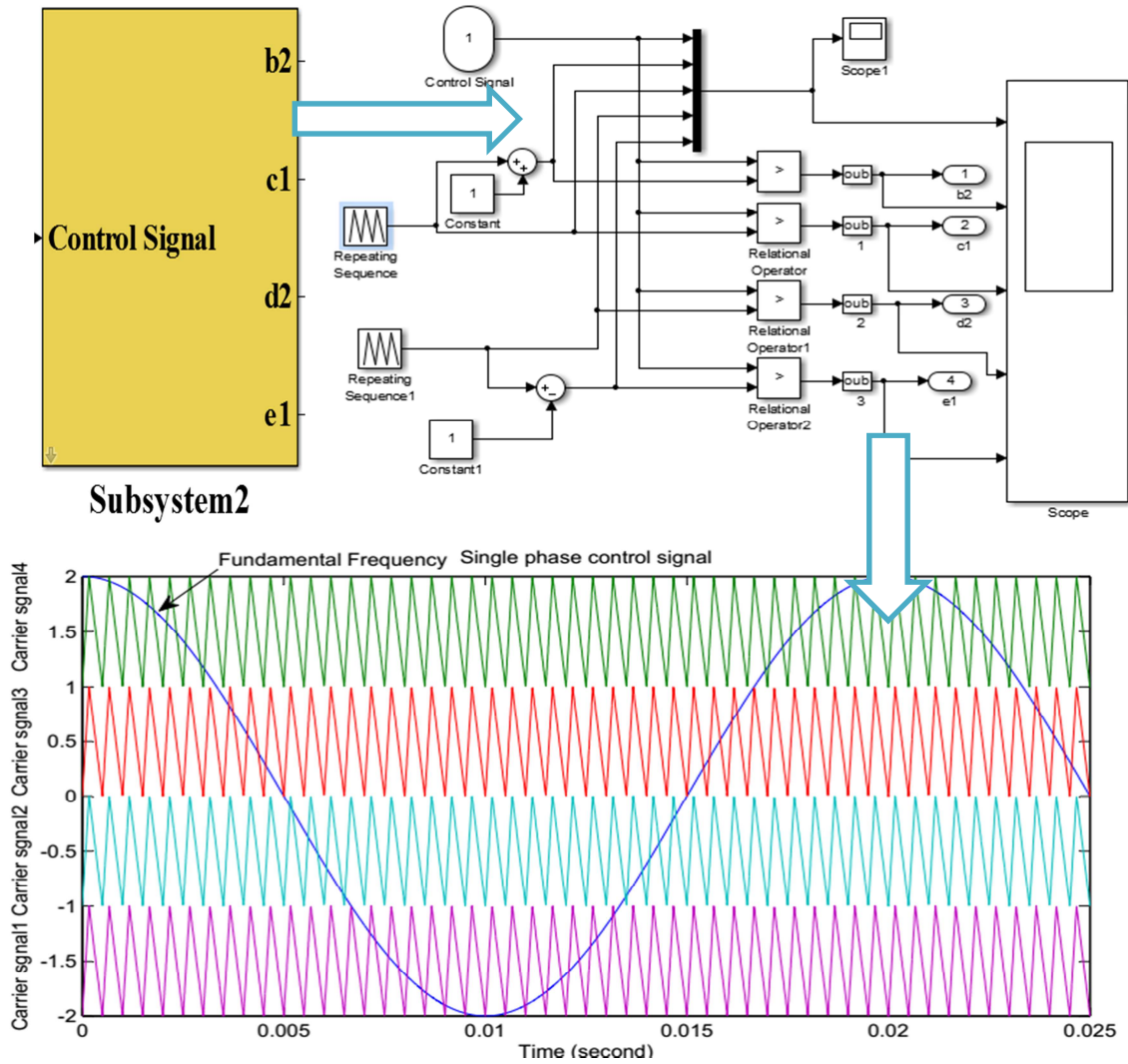


Figure 3.10 Description of control signal block of five level CMLI and their output

By comparing the fundamental frequency and carrier frequency the pulse generated. These generated pulse given to the cascaded multilevel inverter, in this case five level inverter which shown in Figure 3.6. The rest block of Figure 3.8 i.e. subsystem1 and subsystem3 are designed in the fashion as the one described in the above but it feed the left two leg of the cascaded multilevel inverter. Accordingly all the three-phase control signal generate the pulse and arranged switching sequence produce the output voltage as described in Table 3.1.

The signal generator fed the control signal in order to generate the appropriate voltage level in the case five level cascaded multilevel inverter. The following diagram shows the MATLAB implementation of three-phase IM fed with five cascaded multilevel inverter for the case closed loop speed control. This block diagram has one another more diagrams from that Figure 3.8 called PI controller block and hence it is called closed loop speed control system.

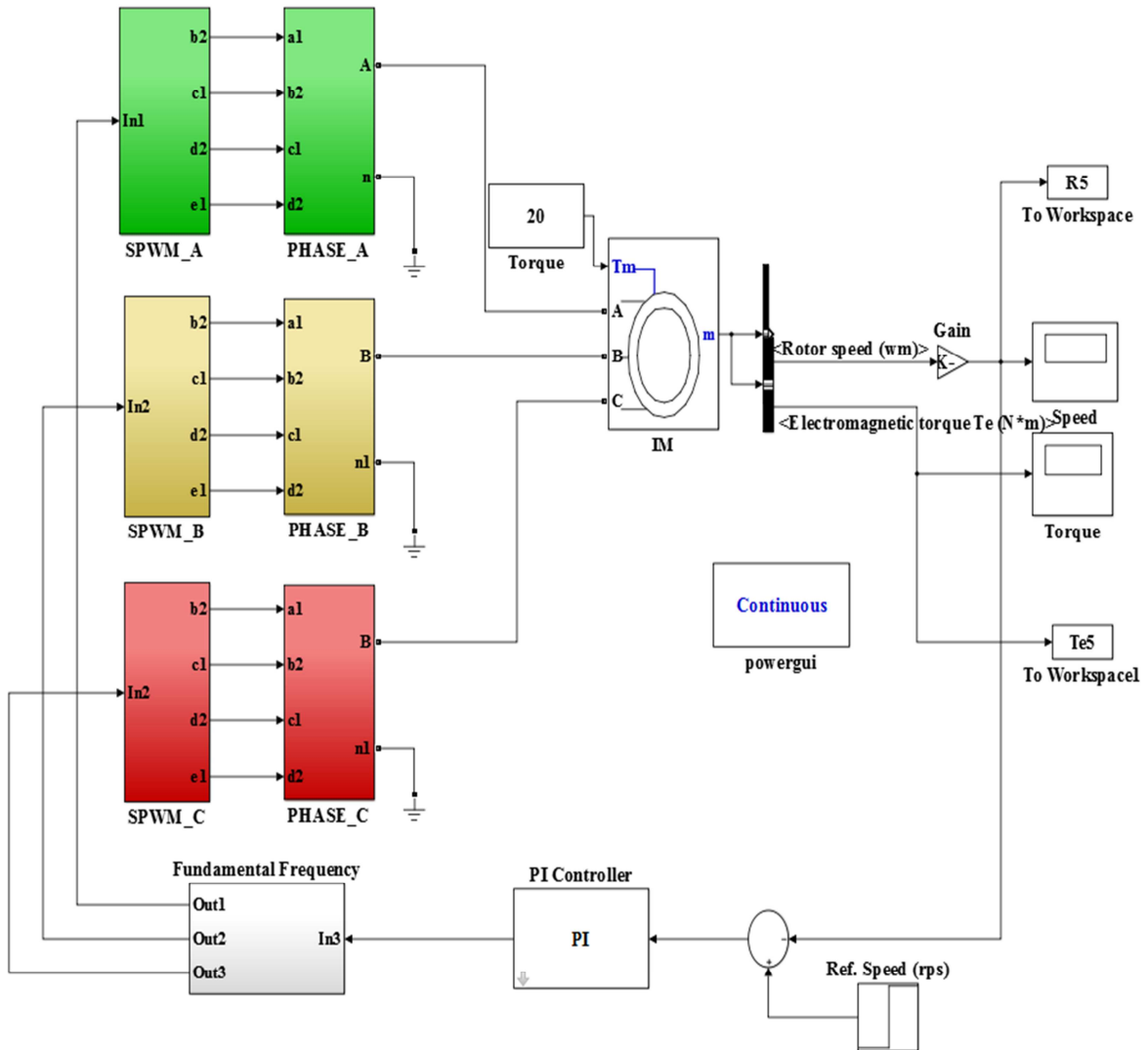


Figure 3.11 Three-phase IM fed with closed loop five CML inverter

The three-phase IM fed with five cascaded multilevel inverter in the case of closed loop speed and torque response is shown in the Figure 4.16 and Figure 4.17 respectively. The function and internal description of this subsystem is the same as the system described for Figure 3.7. But Figure 3.10 block have one additional feedback block named PI controller block and reference speed. The effect of PI controller block in system designed for the speed control of three-phase squirrel cage IM illustrated in chapter four of this thesis work.

3.7 MATLAB implementation of 3 Phase Seven Level CMLI for Induction Motor

The modulating signal fed the control signal in order to generate the appropriate voltage level in the case seven level cascaded multilevel inverter. This cascaded multilevel inverter is different from that of five cascaded multilevel inverter that seven cascaded multilevel inverter has one more H-bridge in it as shown in Figure 3.6. The following diagram shows the MATLAB implementation of three-phase IM fed with seven cascaded multilevel inverter for the case open loop speed control.

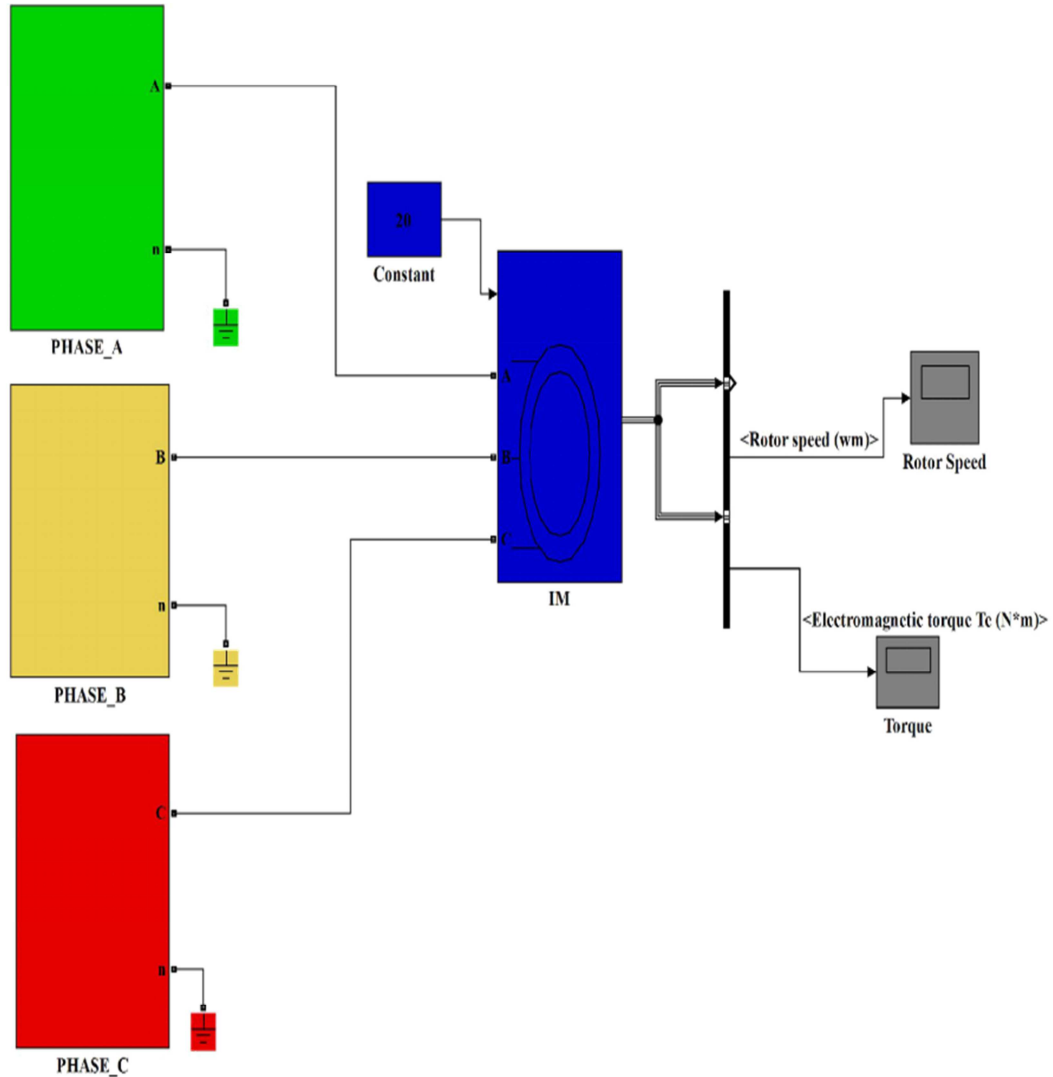


Figure 3.12 Three phase IM feed with open loop seven CML inverter

The three-phase IM fed with seven cascaded multilevel inverter in the case of open loop speed and torque response is shown in the Figure 4.13 and Figure 4.14 respectively. The internal block of PHASE_A is illustrated as in the Figure 3.12. Since the design is for three-phase, the internal block of PHASE_B and PHASE_C has the same system design and the same function for that of PHASE_A.

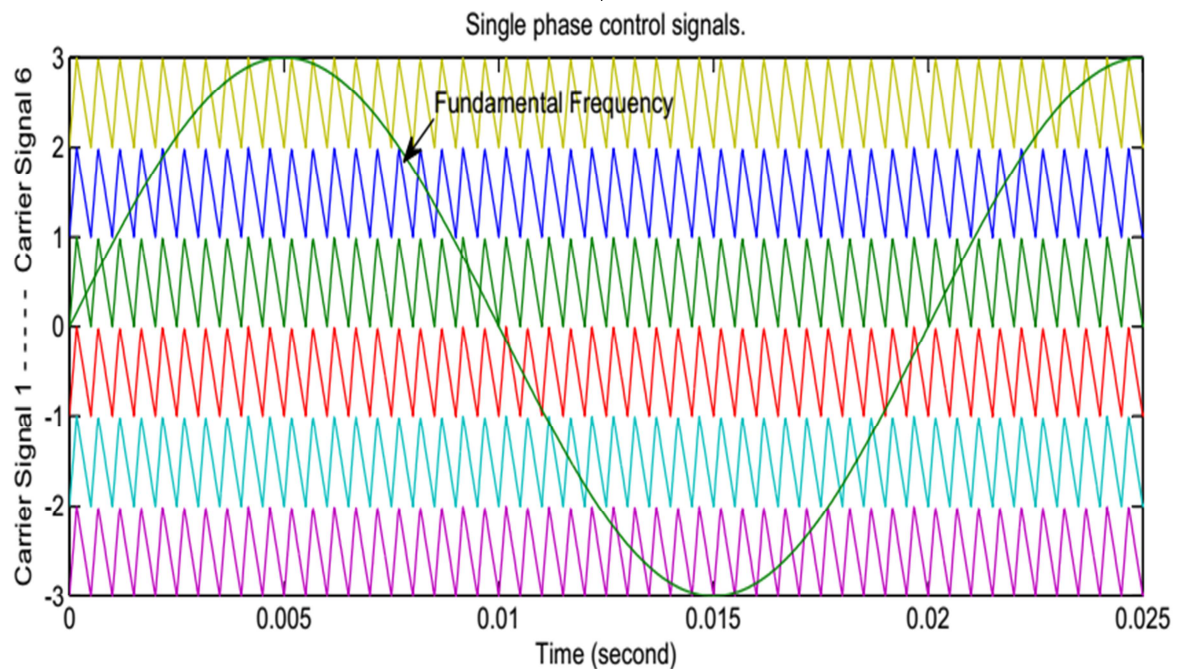
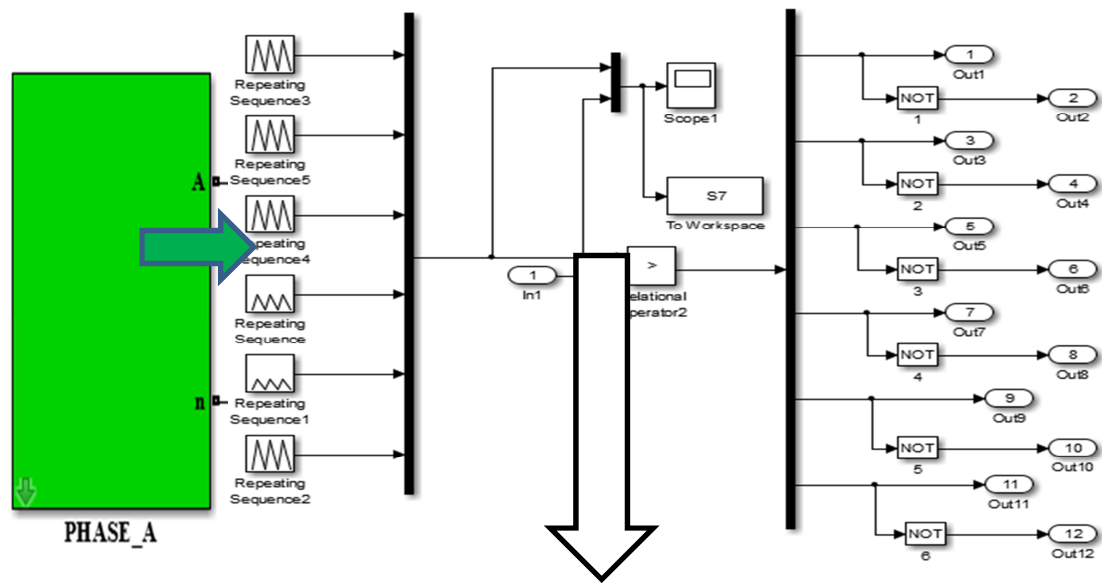


Figure 3.13 Description of control signal block for seven level CMLI and their output

By comparing the fundamental frequency and carrier frequency the pulse generated. These generated pulse given to the cascaded multilevel inverter, in this case seven level inverter which shown in Figure 3.6. The rest block of Figure 3.12 i.e. subsystem of PHASE_B and PHASE_C are designed in the fashion as the one described in the above but it feed the left two leg of the cascaded multilevel inverter. Accordingly all the three-phase control signal generate the pulse and arranged switching sequence produce the output voltage as described in Table 3.2.

The signal generator fed the control signal in order to generate the appropriate voltage level in the case seven level cascaded multilevel inverter. The following diagram shows the MATLAB implementation of three-phase IM fed with seven cascaded multilevel inverter for the case closed loop speed control. This block diagram has one another more diagrams from that Figure 3.12 called PI controller block and hence it is called closed loop speed control system.

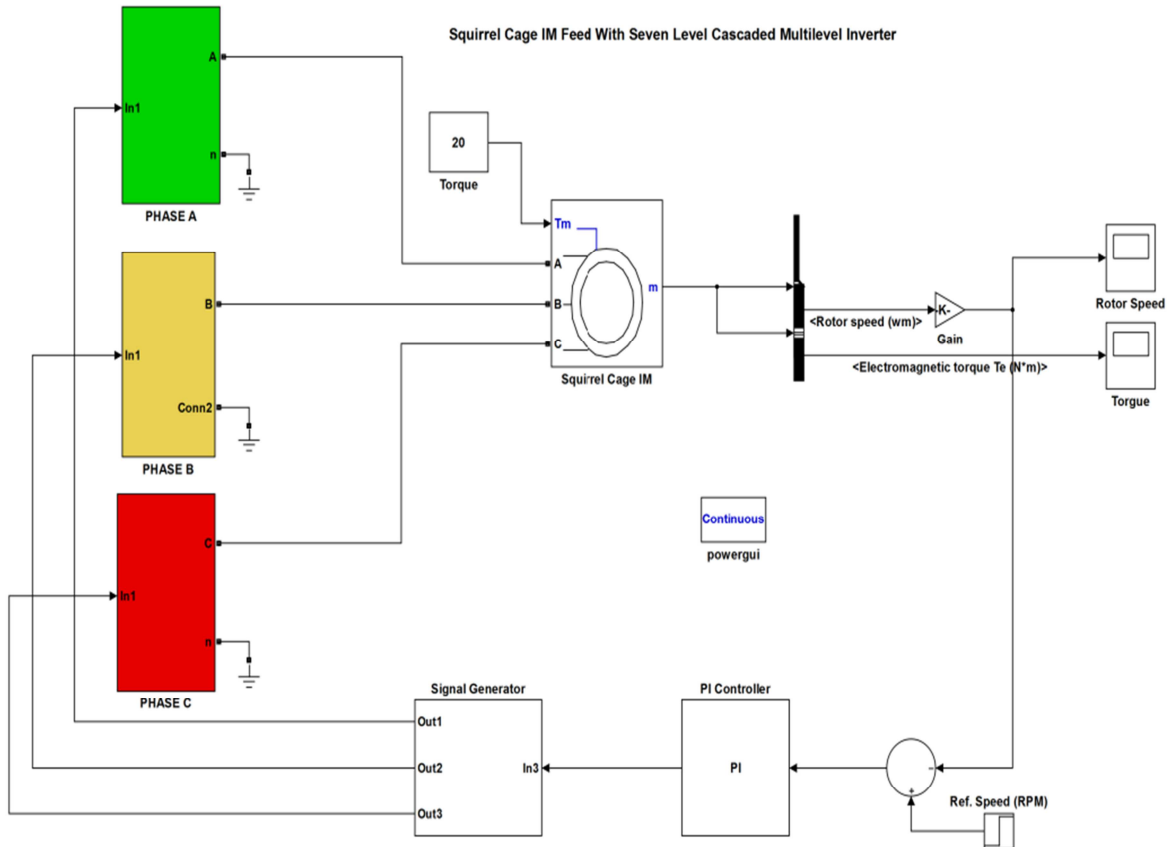


Figure 3.14 Three-phase IM fed with closed loop seven CML inverter

The three-phase IM fed with seven cascaded multilevel inverter in the case of closed loop speed and torque response is shown in the Figure 4.16, Figure 4.17 and Figure 4.18 respectively. The description of system block of Figure 3.12 is the same with system block of Figure 3.14 but this system design contain one additional feedback block named PI controller block. In this case the PI controller looks for the correct output by comparing the actual speed and settled reference speed. The effect of PI controller in speed control of three-phase squirrel cage induction motor explained in chapter.

CHAPTER FOUR

Results and Discussions

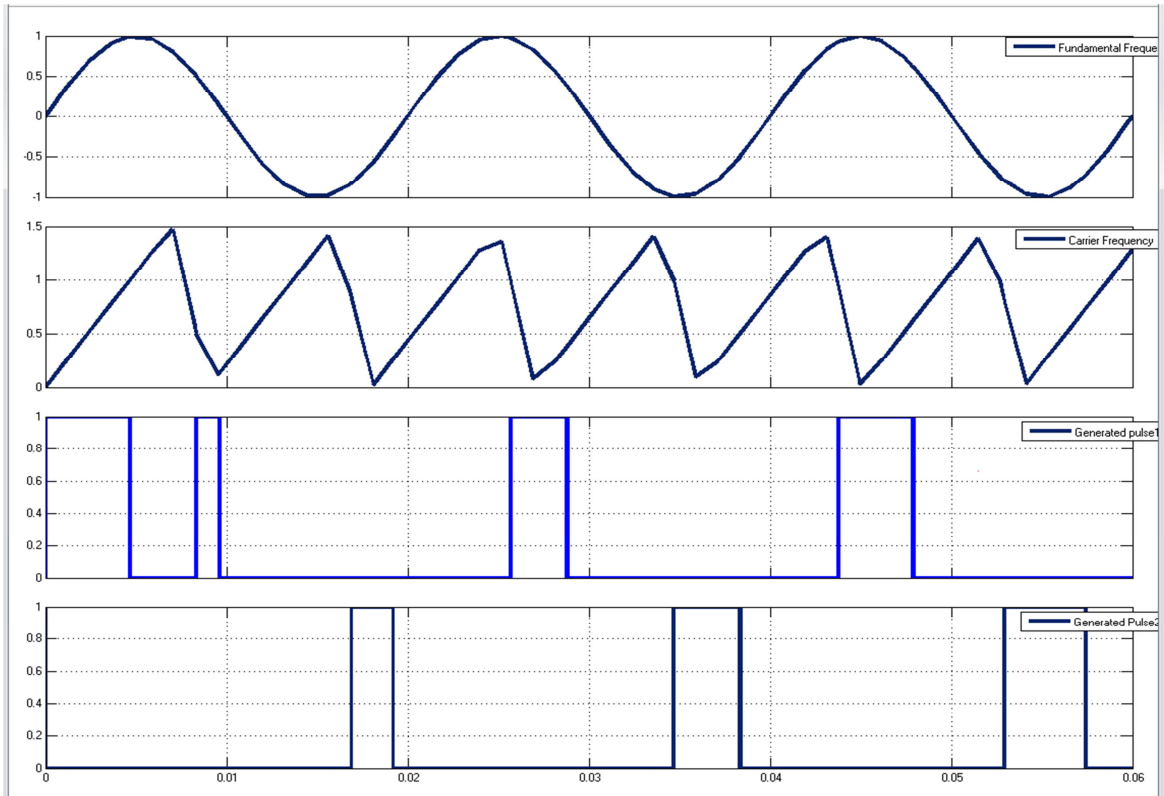


Figure 4.1 Simulated output of SPWM technique

The above generated pulses explain the basic structure sinusoidal PWM. The pulses of the five levels and seven levels are generated with the same concept but with the modification of the triangular wave.

The waveforms of the five level pulse width modulation is as follows

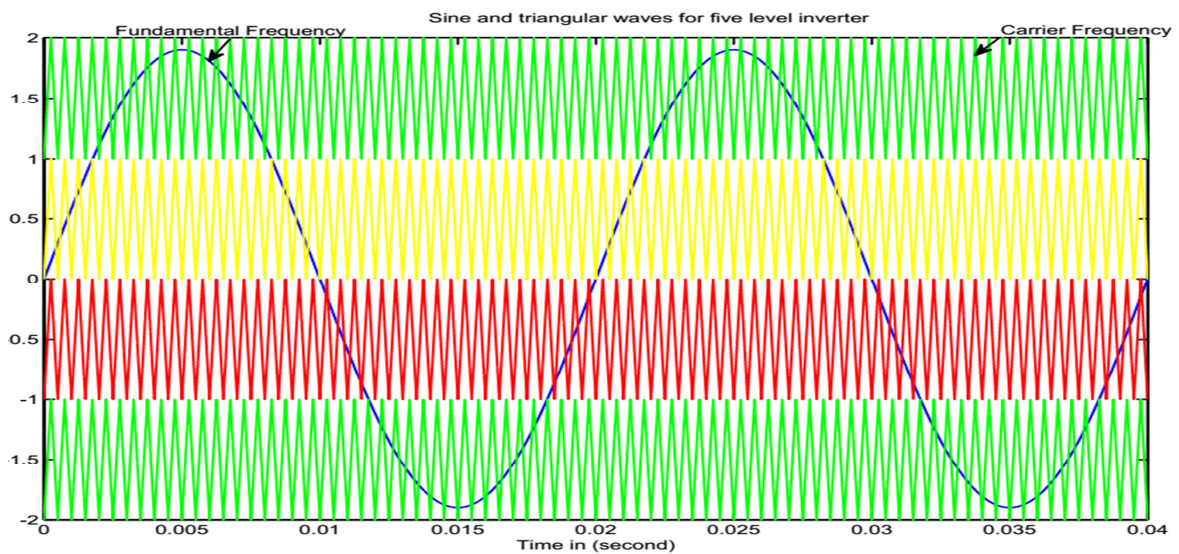


Figure 4.2. Sine and triangular waves for five level inverter

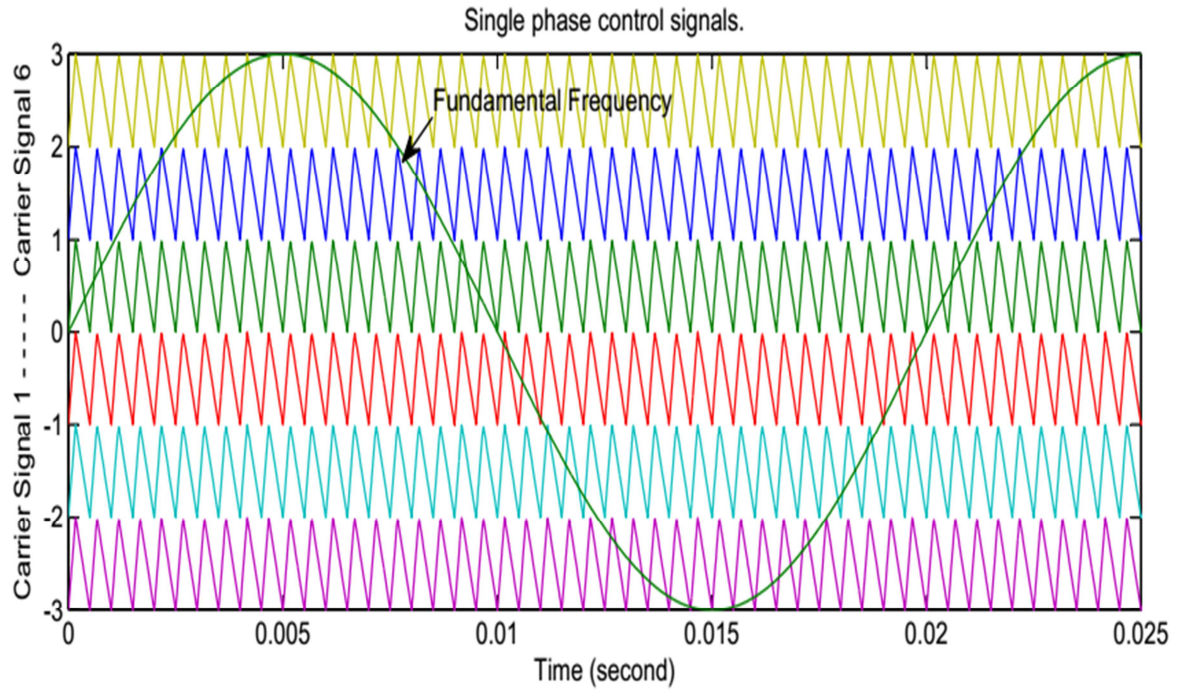


Figure 4.3. Sine and triangular waves for seven level inverter

Figure 4.2 and 4.3 shows the fundamental and carrier frequency wave for single phase five and seven cascaded multilevel inverter respectively. The role of this control signal in the system design is the generate the pulse that control switching sequence of the inverter accordingly.

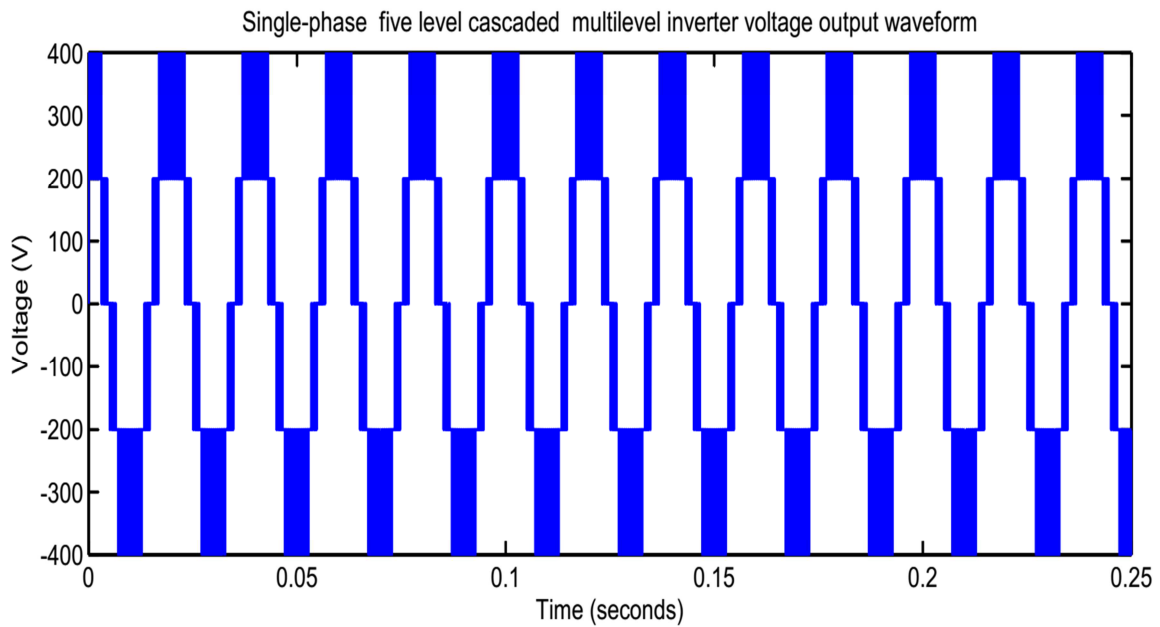


Figure 4.4. Single-phase five level CMLI output waveform

$$(f_m = 50 \text{ Hz}, f_{cr} = 2000 \text{ Hz}, m_a = 1.0)$$

The output waveform of the three phase five level cascaded multilevel inverter

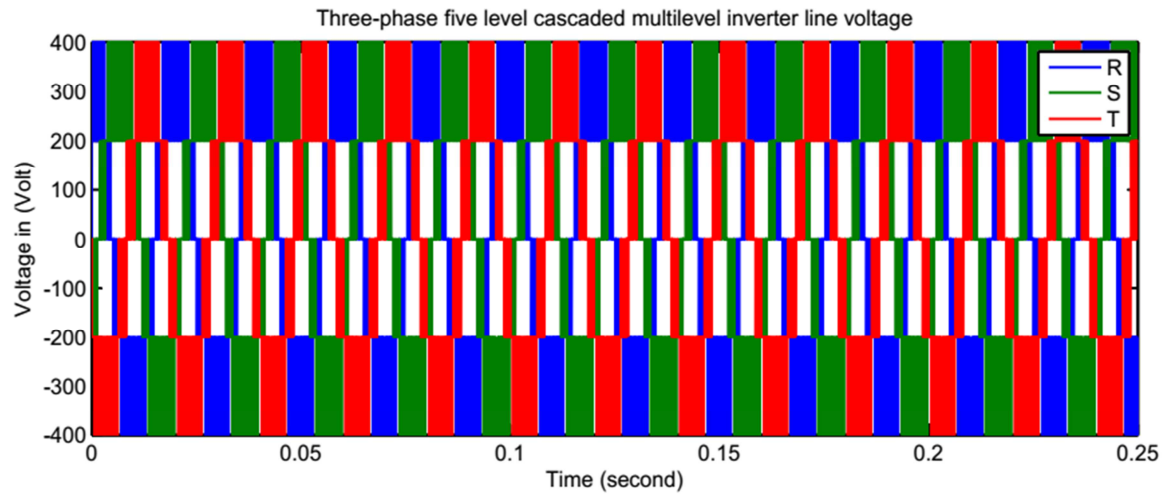


Figure 4.5 Three phase voltage output of five level inverter
 $(f_m = 50 \text{ Hz}, f_{cr} = 2000 \text{ Hz}, m_a = 1.0)$

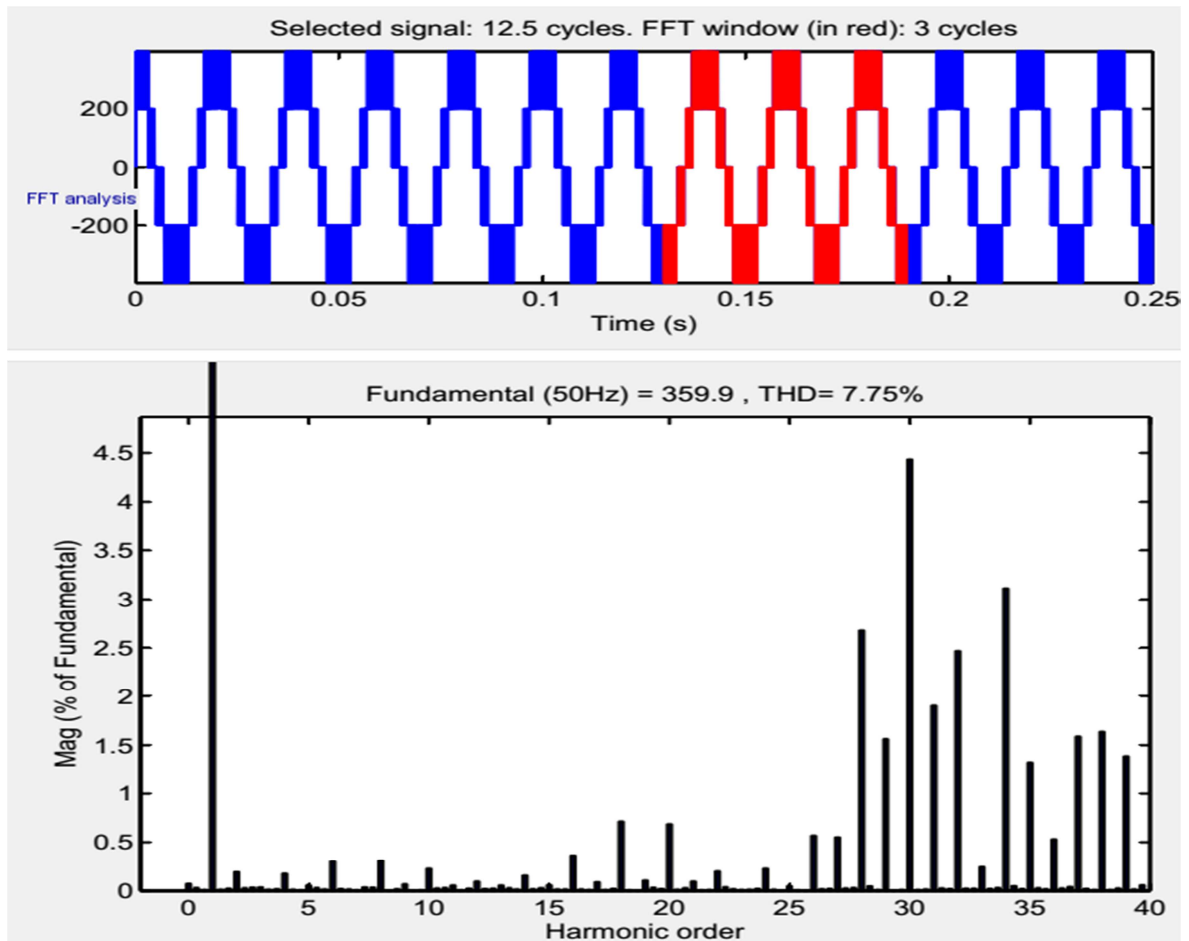


Figure 4.6 Three phase voltage output of five level inverter THD value in percent
 Figure 4.5 and 4.6 indicates the expected output of three-phase voltage for five level cascaded multilevel inverter and its THD measured value.

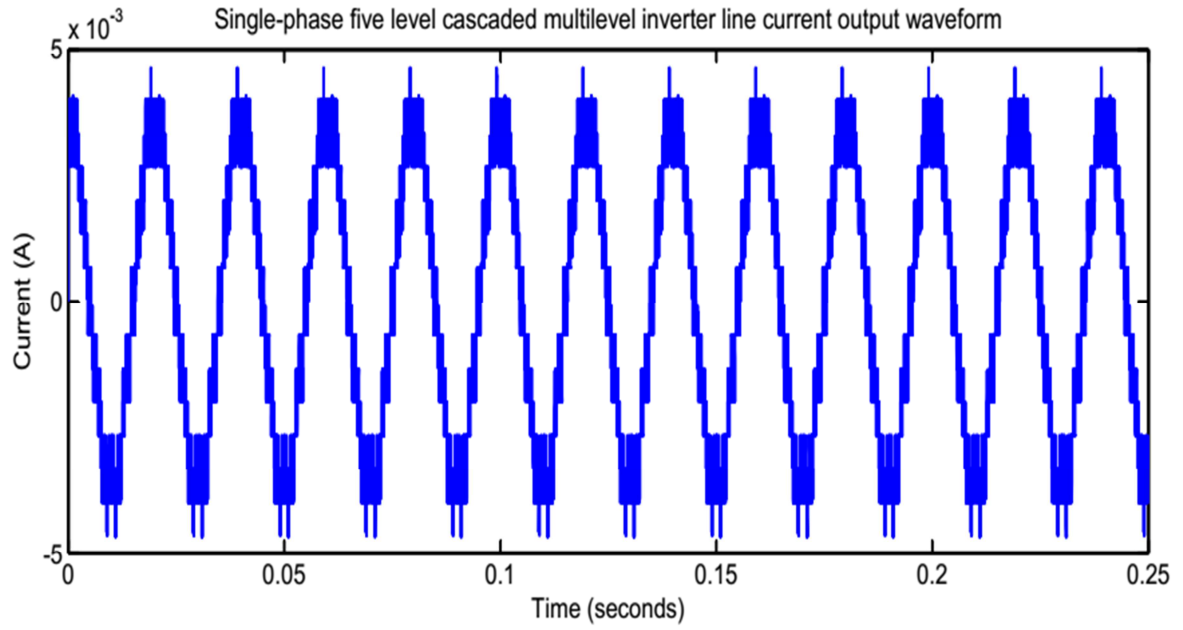


Figure 4.7 Single-phase current output of five level inverter

($f_m = 50$ Hz, $f_{cr} = 2000$ Hz, $m_a = 1.0$)

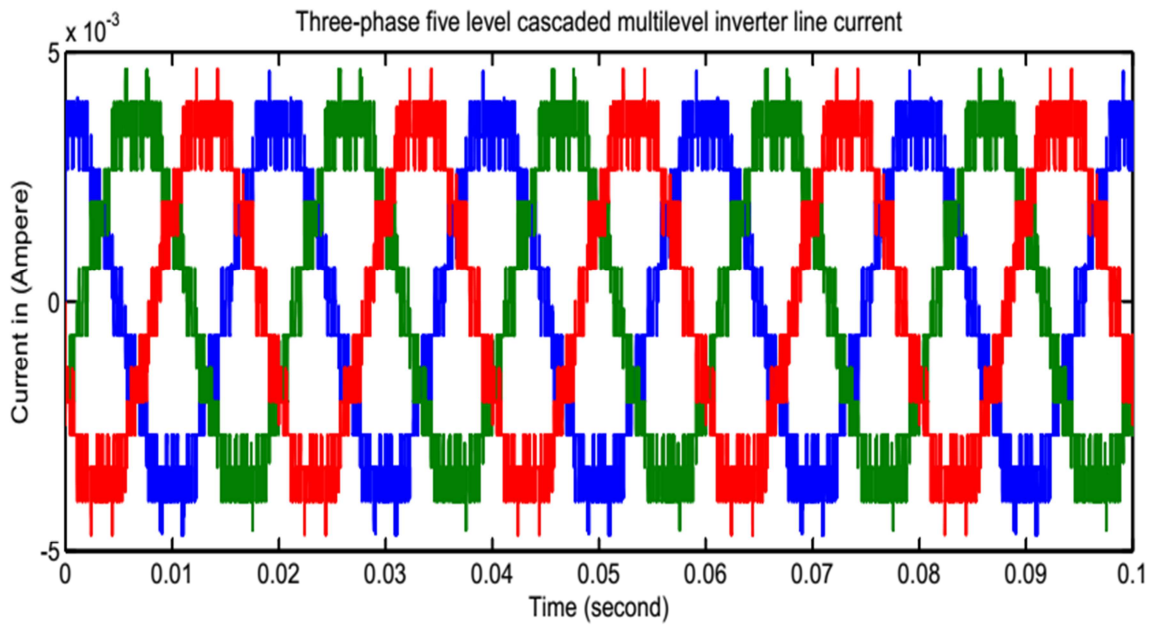


Figure 4.8 Three phase current output of five level inverter

($f_m = 50$ Hz, $f_{cr} = 2000$ Hz, $m_a = 1.0$)

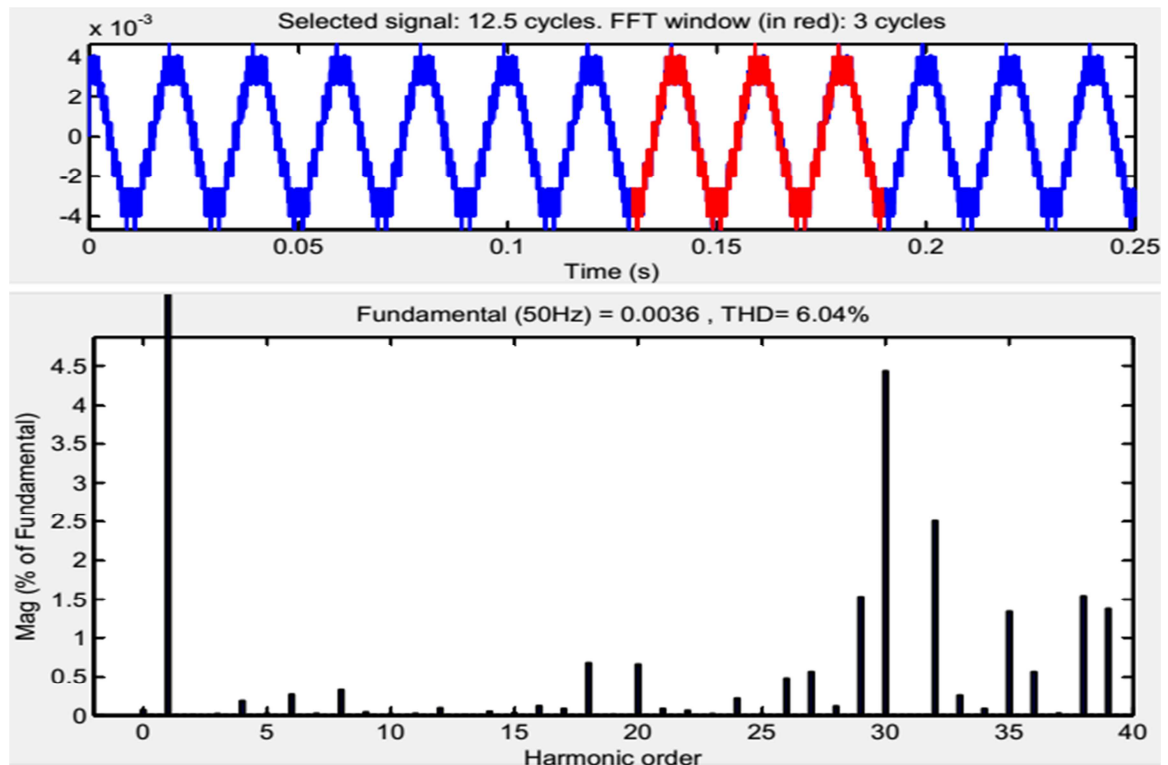


Figure 4.9 Three phase current output of five level inverter THD value in percent
 $(f_m = 50 \text{ Hz}, f_{cr} = 2000 \text{ Hz}, m_a = 1.0)$

Figure 4.8 and 4.9 indicates the expected output of three-phase current for five level cascaded multilevel inverter and its THD measured value. This THD value of current too reduces enough comparing to the THD value measure from the company (Appendix A3). The THD value of five cascaded multilevel inverter is about 6.06% without using filter circuit but even if the company use filtering circuit the measured value of THD value is about 49.00% (Appendix A3).

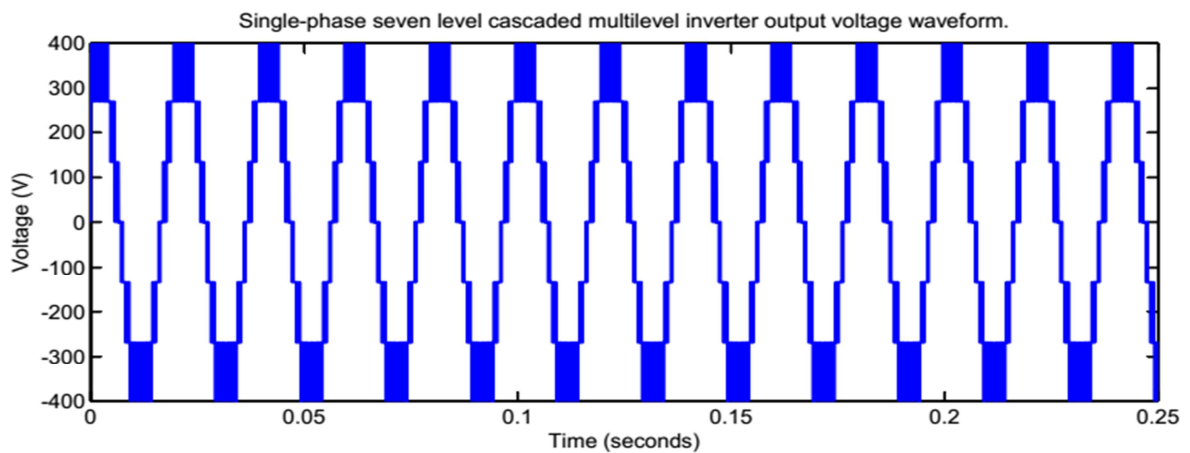


Figure 4.10 Three phase voltage output of seven cascaded multilevel inverter
 $(f_m = 50 \text{ Hz}, f_{cr} = 2000 \text{ Hz}, m_a = 1.0)$

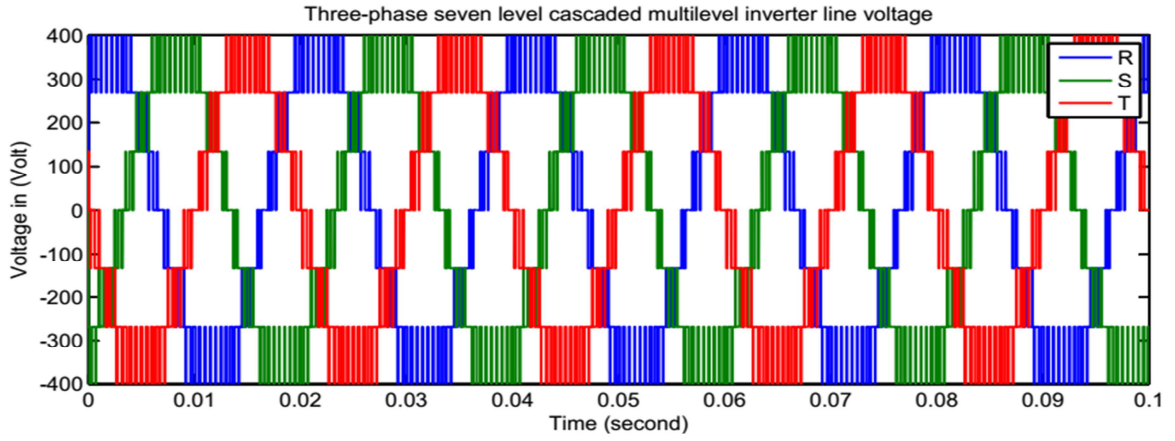


Figure 4.11 Three phase voltage output of seven cascaded multilevel inverter

$$(f_m = 50 \text{ Hz}, f_{cr} = 2000 \text{ Hz}, m_a = 1.0)$$

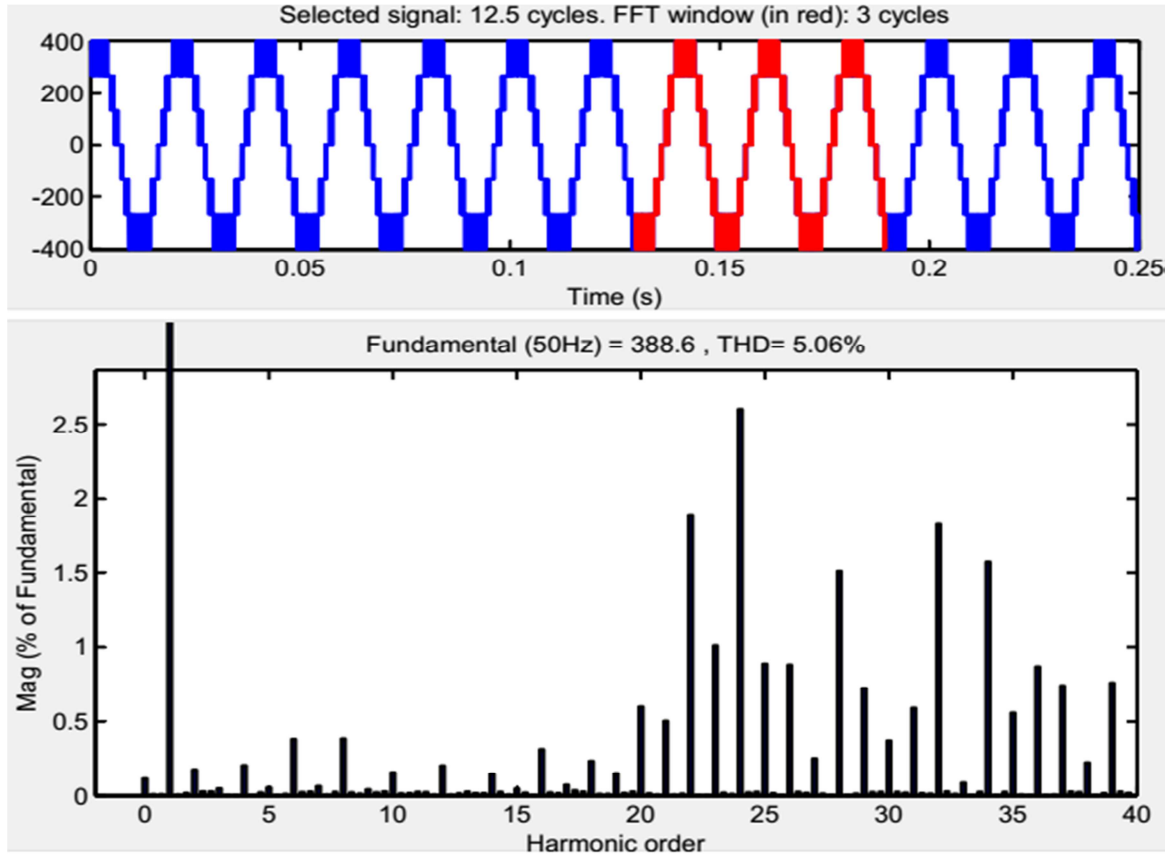


Figure 4.12 Three phase voltage output of seven cascade multilevel inverter THD

$$(f_m = 50 \text{ Hz}, f_{cr} = 2000 \text{ Hz}, m_a = 1.0)$$

Figure 4.11 and 4.12 indicates the expected output of three-phase voltage for seven level cascaded multilevel inverter and its THD measured value. This THD value meet standard as well reduce enough comparing to THD value of company which about 7.10% (AppendixA3)

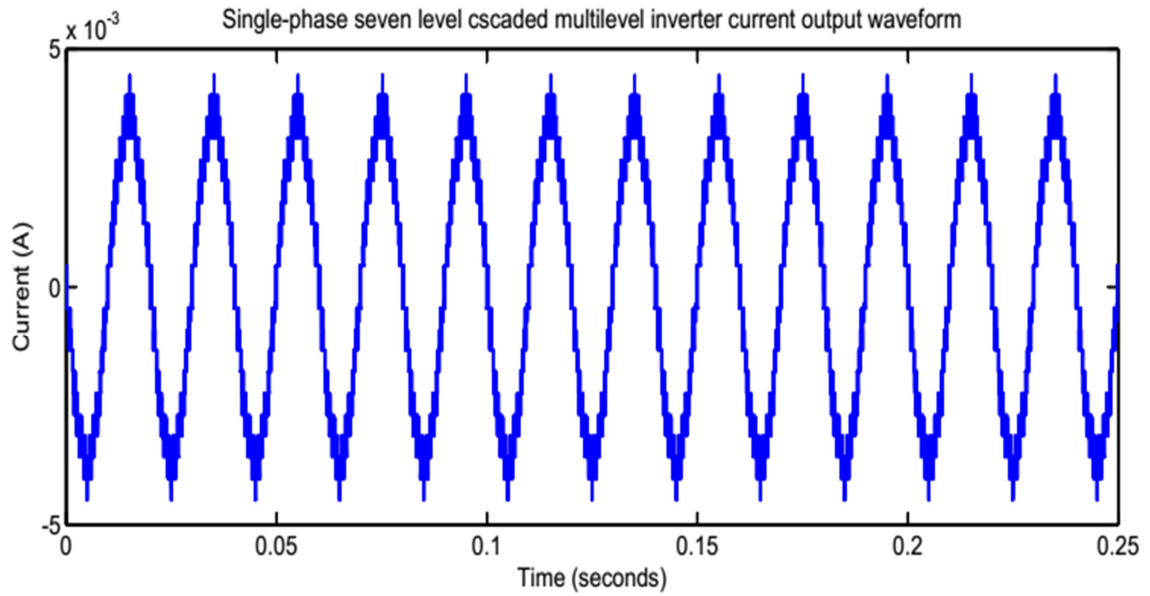


Figure 4.13 Single-phase current output of seven cascade multilevel inverter

($f_m = 50$ Hz, $f_{cr} = 2000$ Hz, $m_a = 1.0$)

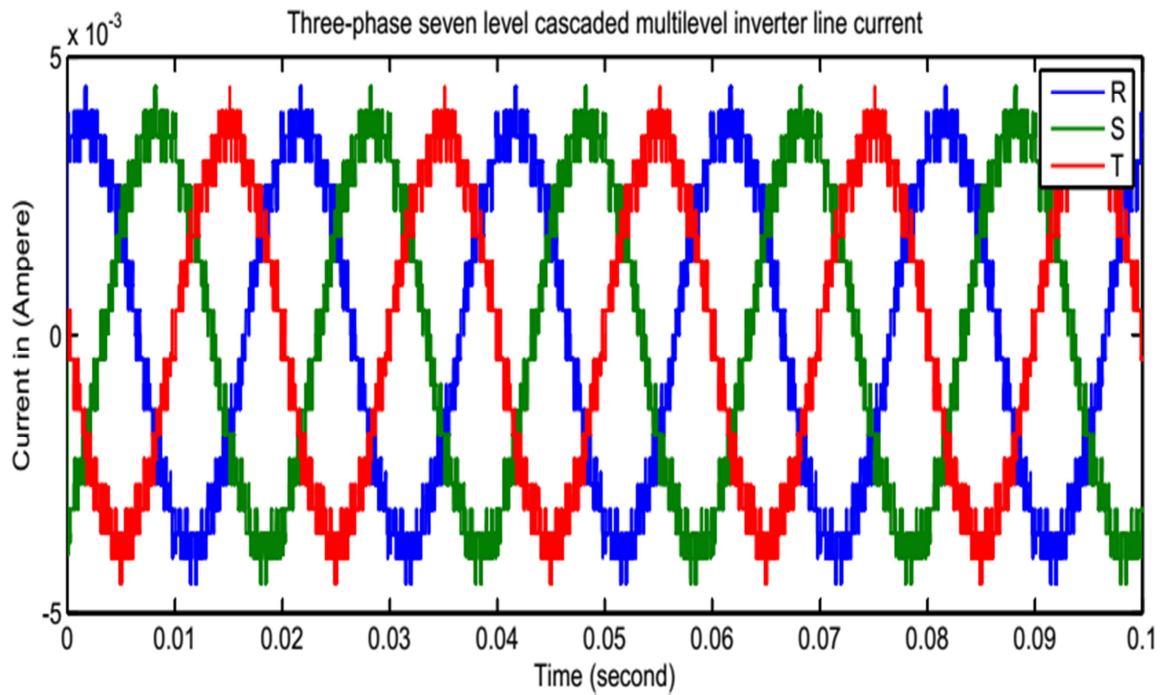


Figure 4.14 Three phase current output of seven cascade multilevel inverter

($f_m = 50$ Hz, $f_{cr} = 2000$ Hz, $m_a = 1.0$)

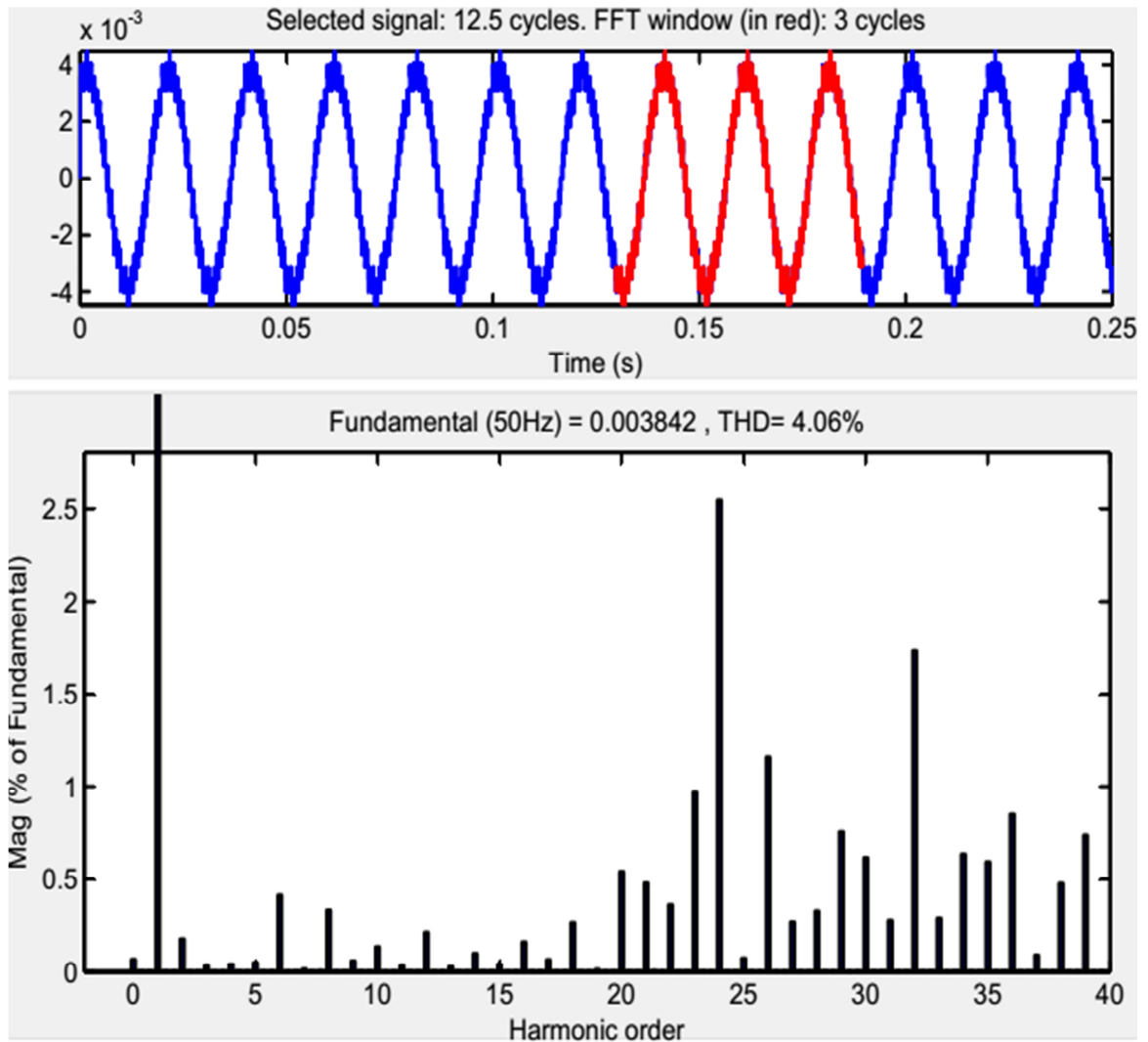


Figure 4.15 Three phase current output of five cascaded multilevel inverter THD

$$(f_m = 50 \text{ Hz}, f_{cr} = 2000 \text{ Hz}, m_a = 1.0)$$

Figure 4.14 and 4.15 indicates the expected output of three-phase current for seven level cascaded multilevel inverter and its THD measured value. This THD value of current too reduces enough comparing to the THD value measure from the company (Appendix A3). The THD value of five cascaded multilevel inverter is about 4.06% without using filter circuit but even if the company use filtering circuit the measured value of THD value is about 49.00% (Appendix A3).

4.1.Comparison of THD for different modulation indexes at different levels

The 'm' value is changed with the change in the values of the magnitude of the reference wave (sine). The different values are as shown in the table 4.1.

Table 4.1 Comparison of THD for five and seven cascaded multilevel inverter with different m_f and m_a values

THD for 5-level				THD for 7-level		
Modulating Frequency (m_f)	Modulation Index (m_a)			Modulation Index (m_a)		
	0.8	0.9	1.0	0.8	0.9	1.0
2000	9.34%	7.88%	7.75%	6.37%	5.45%	5.06%
1000	9.22%	7.25%	7.12%	6.35%	5.34%	4.47%
500	7.91%	7.21%	5.71%	6.31%	5.12%	4.21%
250	4.95%	3.99%	3.85%	3.79%	3.56%	3.07%

We observe that the value of the THD decreases as the Amplitude modulation index (m_a) increases. The value of the THD is also improved if the frequency modulation index is decreased.

4.2.Comparison of three-phase IM fed with five CMLI rotor speed response for open and closed loop

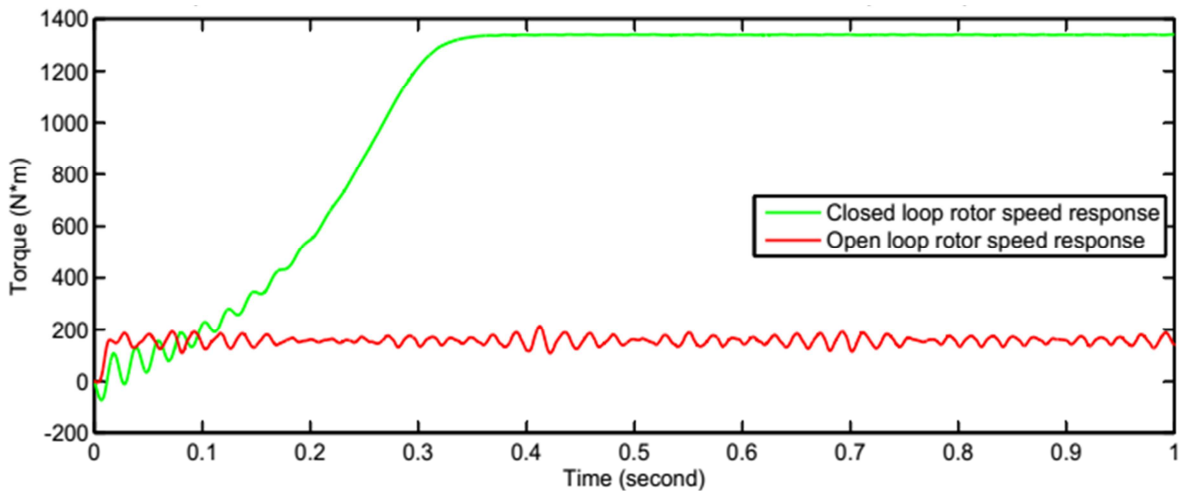


Figure 4.16 Speed comparisons five CMLI with open and closed loop IM under load

Figure 4.16 compare the speed performance of three phase squirrel cage IM fed with five cascaded multilevel inverter for the same rated speed of 1430 RPM and load torque of 20 Nm in both open loop and closed control system. The speed response open loop control is very less when we compare to that of closed loop control system. For settling reference speed 1500 RPM and 1430 RPM rated speed of the motor the speed respond of open loop and closed loop is 150 RPM and 1335 RPM respectively. In the case open loop speed response thought the system no smooth at all. But closed loop speed response indicates that

after 0.3 second the system speed response become smooth and steady state. The IP controller increases the performance of the machine as it shown in the above figure.

4.3. Comparison of three-phase IM fed with five and seven CMLI rotor speed response for open loop

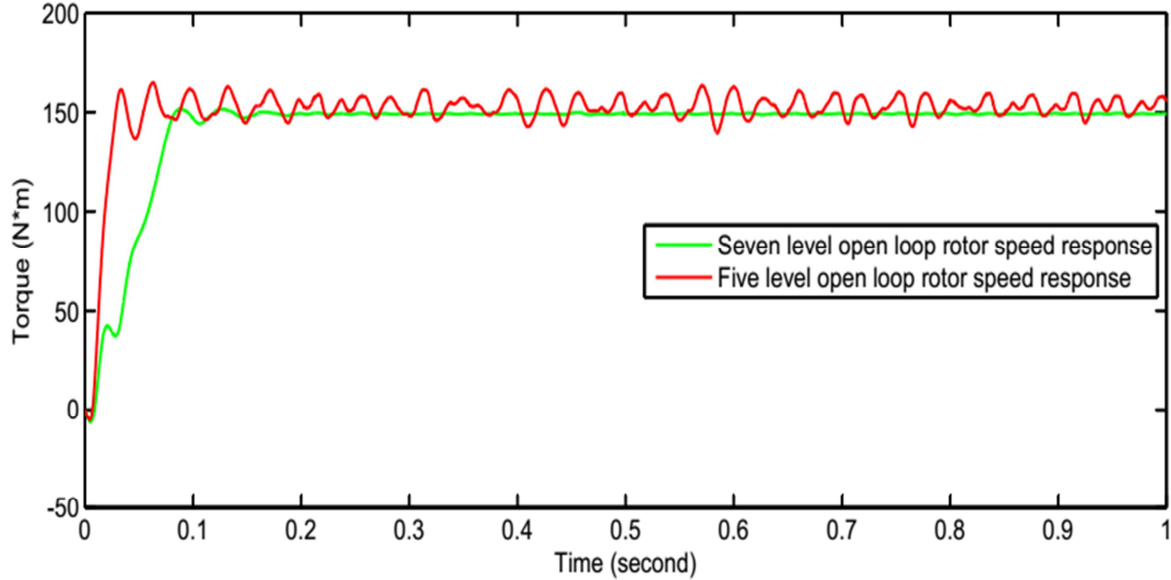


Figure 4.17 Speed comparisons five and seven CMLI with open loop IM under load

The speed response of three-phase IM fed with five and seven cascaded multilevel inverter under load is compared as in Figure 4.17. We observe that for the same rated speed and load the speed response of both five and seven level is clearly shown in the above figure. In the case five cascaded multilevel inverter the system didn't smooth throughout the system. Relatively it shows a fluctuation as indicate on the Figure 4.13. But for the case of seven cascaded multilevel inverter the speed become steady state at 0.1 second and it has no damping when compared to the five cascaded multilevel inverter. Why because the frequency of a waveform is the number of times it repeats (cycles) in one second, the time it takes the waveform to transition from one peak level to the other. Therefore rise time is related to how quickly changes can happen. Hence it proves that as the number of multilevel increase the controllability of the machine also become smooth even if it is open loop system.

4.4. Comparison of three-phase IM fed with five and seven CMLI Load torque response for open a loop

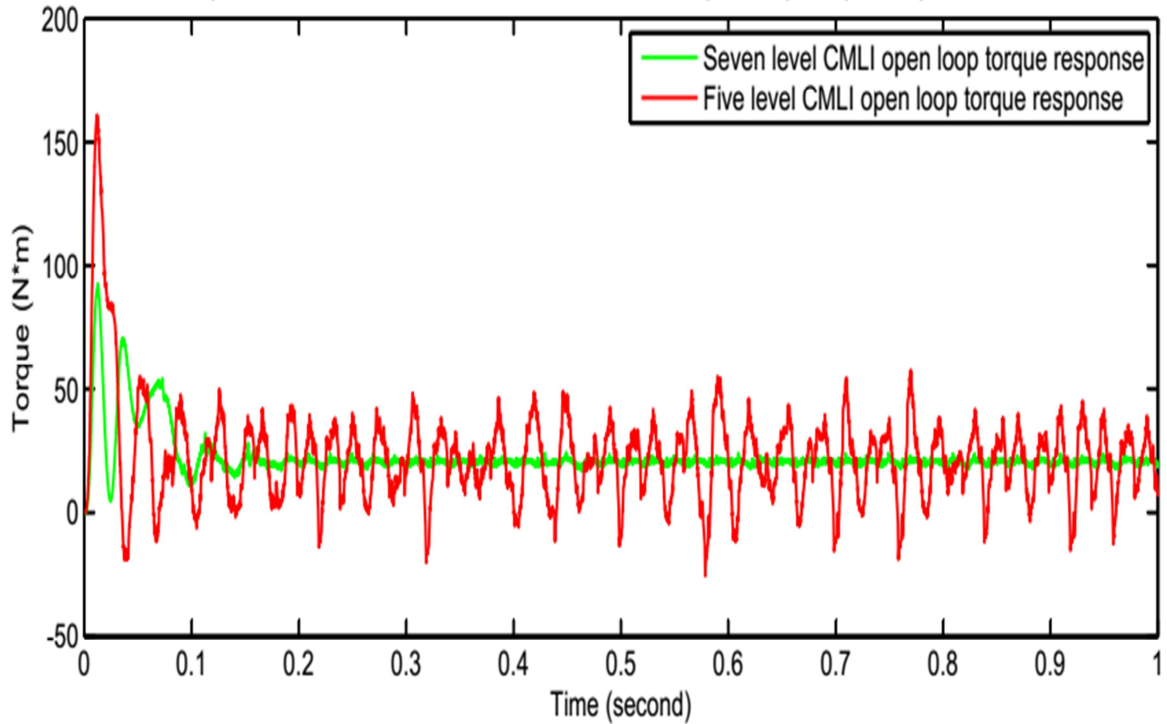


Figure 4.18 Torque comparisons five and seven CMLI with open loop IM under load Under the some rated speed 1430 RPM, load torque 20 Nm and settling time of one second in the case open loop control under the load, torque response is compared in Figure 4.18. The load torque is result in more overshoot and more damping in the case five cascaded multilevel inverter as shown in the Figure 4.16. It doesn't smooth throughout the system which indicate the inefficiency of the system. But in the case of seven cascaded multilevel inverter the load torque result in less overshoot and damping. The torques becomes constant or steady state at time 0.12 second.

In general even if it is open control system figure 4.16 shows the load torque performance of the system as it increase from five cascaded multilevel inverter to seven cascaded multilevel inverter. The system disturbance improved as the number of multilevel increase i.e. from five to seven.

4.5. Comparison of three-phase IM fed with seven CMLI rotor speed response for open and closed loop

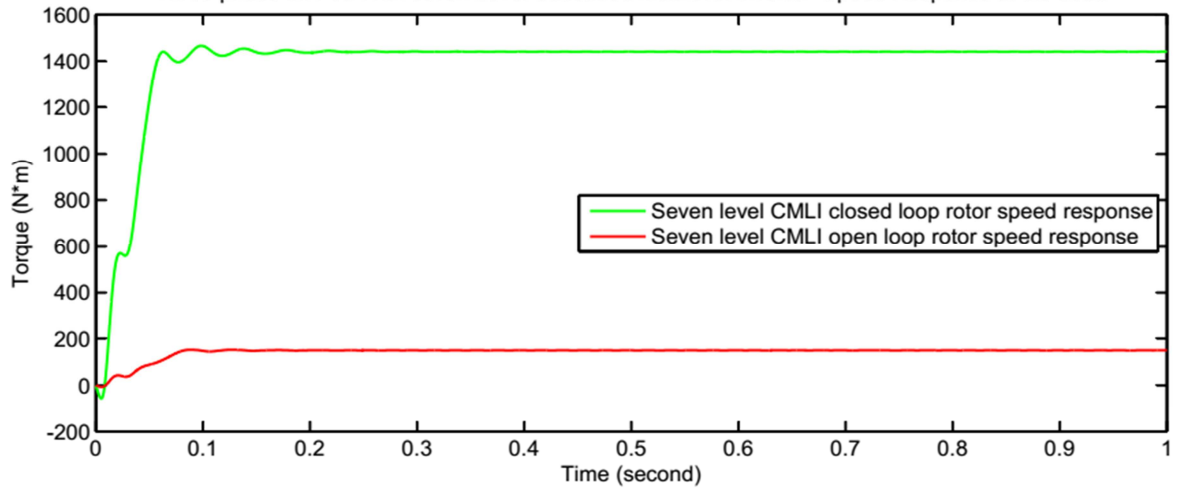


Figure 4.19 Speed comparisons seven CMLI with open and closed loop IM under load

Figure 4.19 compare speed of three phase IM motor feed with seven cascaded multilevel inverter in the case of open loop and closed loop control system i.e. performance of IP controller in the case of closed loop. Under the same load torque 20 Nm, rated speed 1430 RPM and settling time one second speed response shown in figure 4.19. The reference speed of closed loop control 1500 RPM. For the some rated speed, the response of open loop is 150 RPM and whereas the PI controller speed response i.e. closed loop speed response is almost 1430 RPM under the same load which indicate that speed control using PI controller more efficient.

4.6. Comparison of three-phase IM fed with five and seven CMLI rotor speed response for closed loop

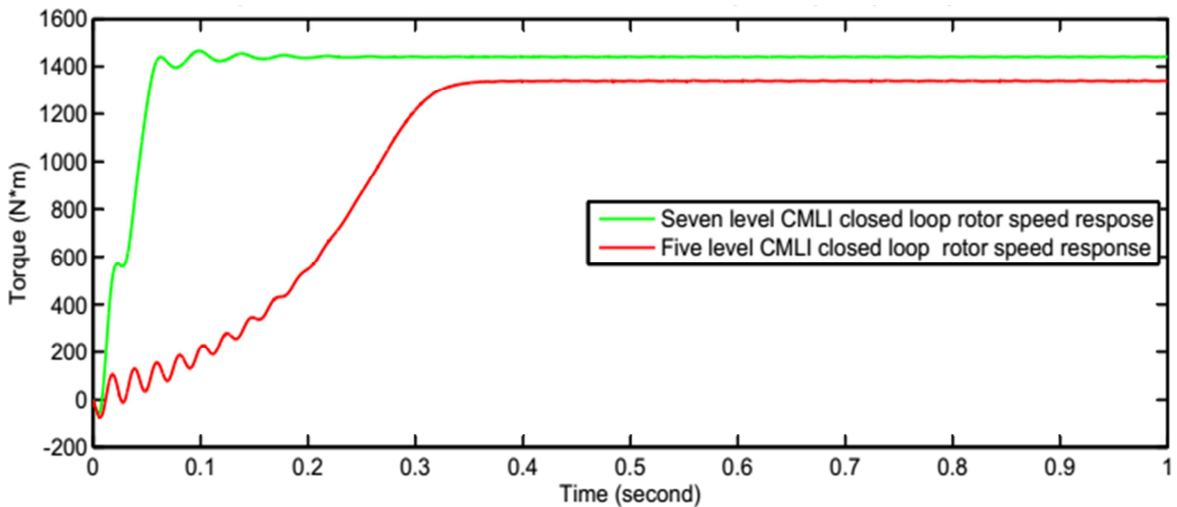


Figure 4.20 Speed comparisons for 5 & 7 level inverter with closed loop IM under load

The PI controller speed has less overshoot. Settling time is one and rise time is also less for a set speed of 1500 RPM and the load torque of 20 Nm. Figure 4.20 shows the PI controller speed response relationship for IM feed with five and seven CML inverter under the same load and same settling time and speed as shown in Figure 4.18. For the rated speed of 1430 RPM, the speed response of five cascaded multilevel inverter is around 1398 RPM and where as in the case seven cascaded multilevel inverter is 1428 RPM as shown in the above Figure 4.20. As we observed from Figure 4.20 after some damping speed becomes steady state at a time 0.31 second in the case of five cascaded multilevel inverter. However in the case of seven cascaded multilevel inverter the speed become steady state almost after 0.15 second with less damping.

4.7. Comparison of three-phase IM fed with seven CMLI rotor speed response for closed loop at no load

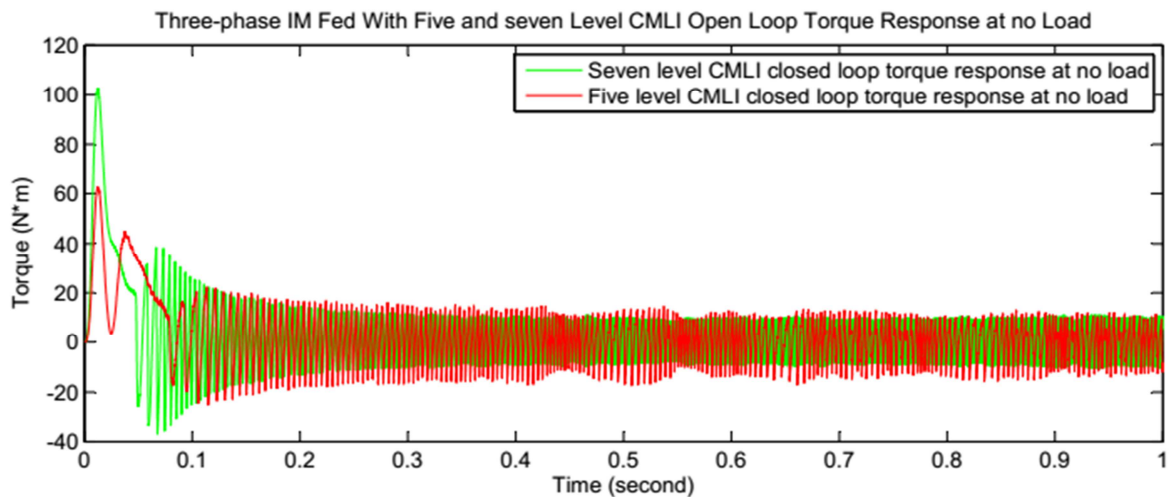


Figure 4.21 Torque comparisons for 5 & 7 level inverter with closed loop IM under no load. Figure 4.21 compares the torque response of three-phase IM feed with five and seven cascaded multilevel inverter under no load case. As we observe from Figure 4.21 the torque response for five level inverter has more damping, not smooth and less settling time than that of seven level inverter. Figure 4.21 clearly shows how much it damped comparing the two no load torque within the same settling time. This proves how the system controllability performance is increased as the number of multilevel increases from five to seven levels.

4.8. Comparison of three-phase IM fed with five and seven CMLI rotor speed response for closed loop at load

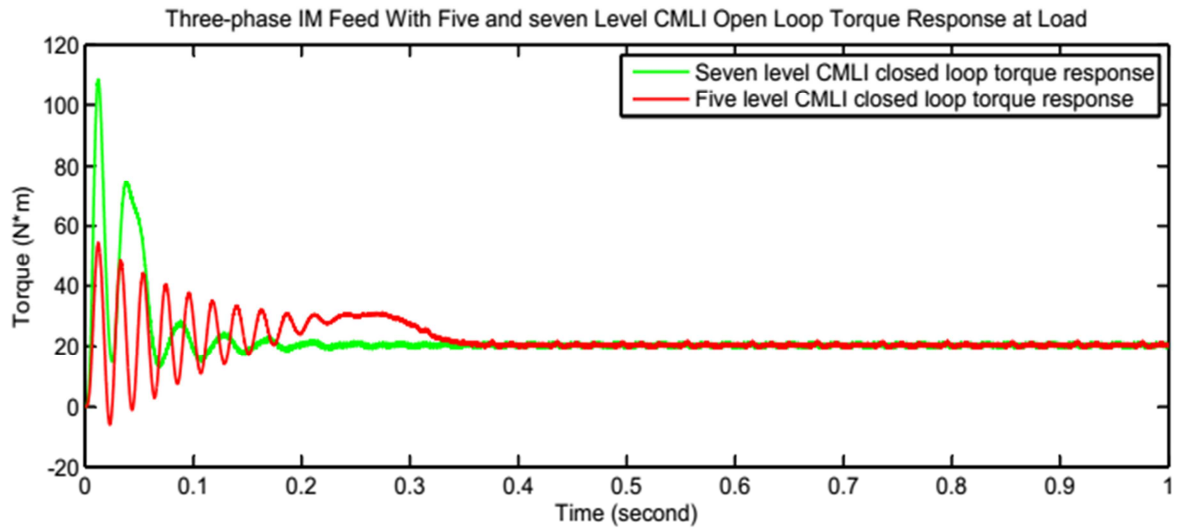


Figure 4.22 Speed comparisons for 5 & 7 level inverter with closed loop IM under load
Figure 4.22 compare the torque response of three-phase IM feed with five and seven cascaded multilevel inverter under load torque 20 Nm. As we observe from Figure 4.22 the torque response for five cascaded multilevel inverter has more damping, not smooth and less settling time than that of seven level inverter as it clear shown in Figure 4.22.

CHAPTER FIVE

Conclusion and Recommendation

5.1 Conclusion

Fundamental multilevel inverter structures and modulation examples including the advantage and disadvantages of each technique have been discussed. In most the thesis emphases on recent and more practical industrial applications of cascaded multilevel inverter. It should be well-known that this thesis cannot cover all multilevel power converter related applications. However the basic principles of different multilevel converters have been discussed precisely. In this thesis work the switching pulses are produced by using the sinusoidal pulse width modulation technique which compares the triangular wave with that of the sine wave and the pulse is produced when the sine is greater than triangular.

This thesis work shows that the value of the THD will decrease as the modulation index (m) is increased. Here the ' m ' is calculated for three different values. Indeed thesis paper also concludes that the value of the THD will be improved as the level of the inverter is increased i.e. from five level to the seven level. The designed cascaded multilevel inverter THD value for voltage and current are 5.06% and 4.06% respectively and that of measured from the company by researcher during instigation for voltage and current are 7.10% and 49.00% respectively. Hence the designed cascaded multilevel is proven over that measured from the company. The outputs of the three phase inverters are given to the three phase squirrel cage induction motor and its speed and torque characteristics are obtained. The speed curve obtained is smooth in the case of seven level compared with that of the five level. Finally, concludes that the speed characteristics are improved as the level of the inverter is improved i.e. from the five level to the seven level. The performance of the machine will be improved when it is fed with multi-level inverter.

5.2 Recommendation

Cascaded multilevel inverter based speed controls is the modern techniques in industrial application today because of the benefit mentioned in this thesis paper comparing to the convention adjustable speed controls of drives. The researcher could be recommended that the expansion of existing convectional inverters with cascaded multilevel inverter based speed control method.

- Since the cascaded multilevel inverter is no need filtering circuit the author recommends the company to shift their existing new version of power electronic device called cascaded multilevel inverters based speed control method.
- Hence the THD value of current and voltage has the negative effects on the performance of the machine; the author recommends Chemical Industry Corporation Muger Cement Factory to look the standard THD value of the currents and voltage during buying. So that the company can free from extra billing for the Utility.
- Author recommendation is goes to Ethiopian Electric Utility to take the measured data of THD value of the customer before sales the power to any industries, so that the company gives notice their own allowable THD value voltage and current. Hence this pre-independent knowing THD values will safe from wastage of energy.

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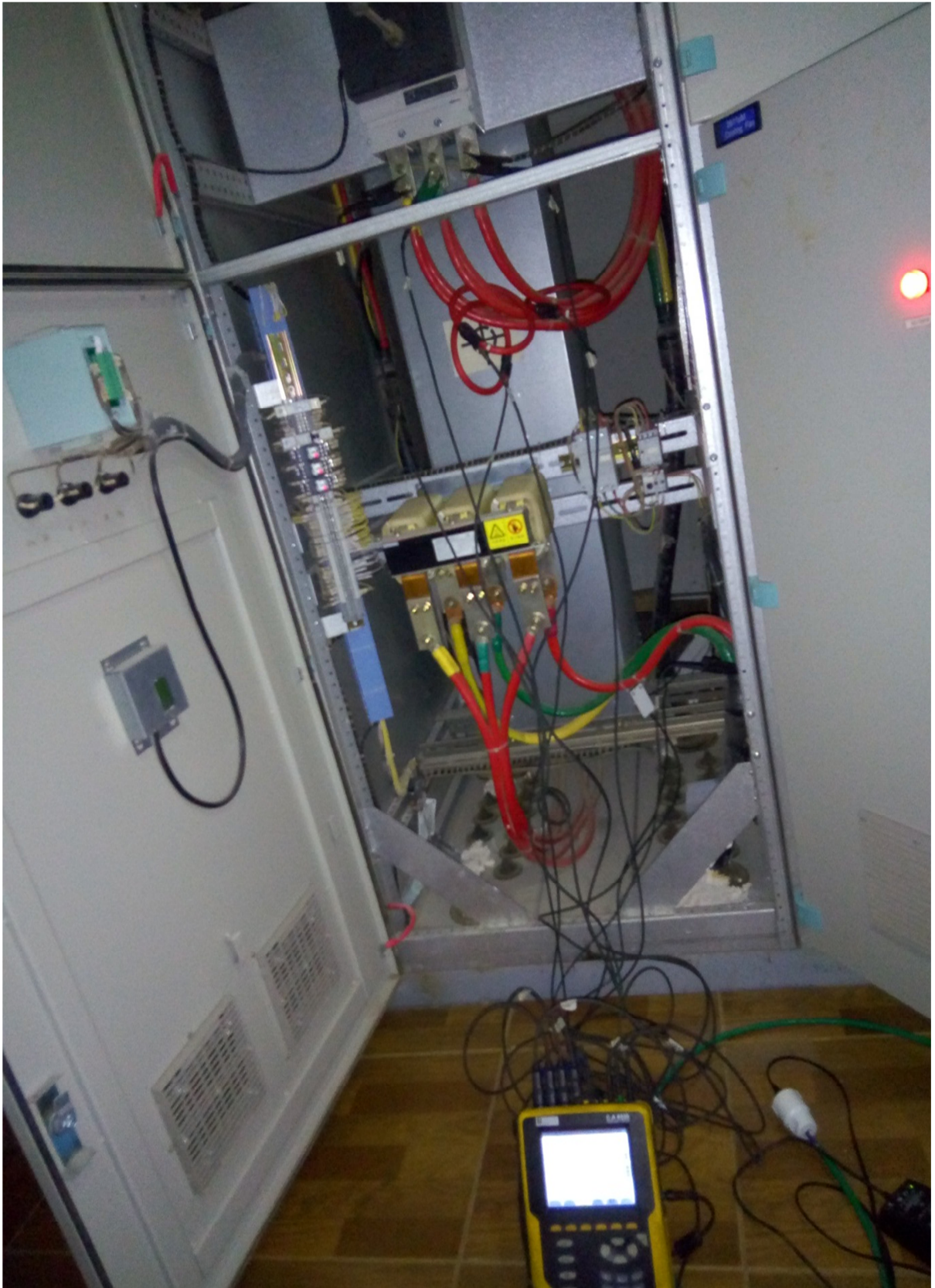
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Appendix A: C.A 8335-212306 2.6 Instrumentation Configuration

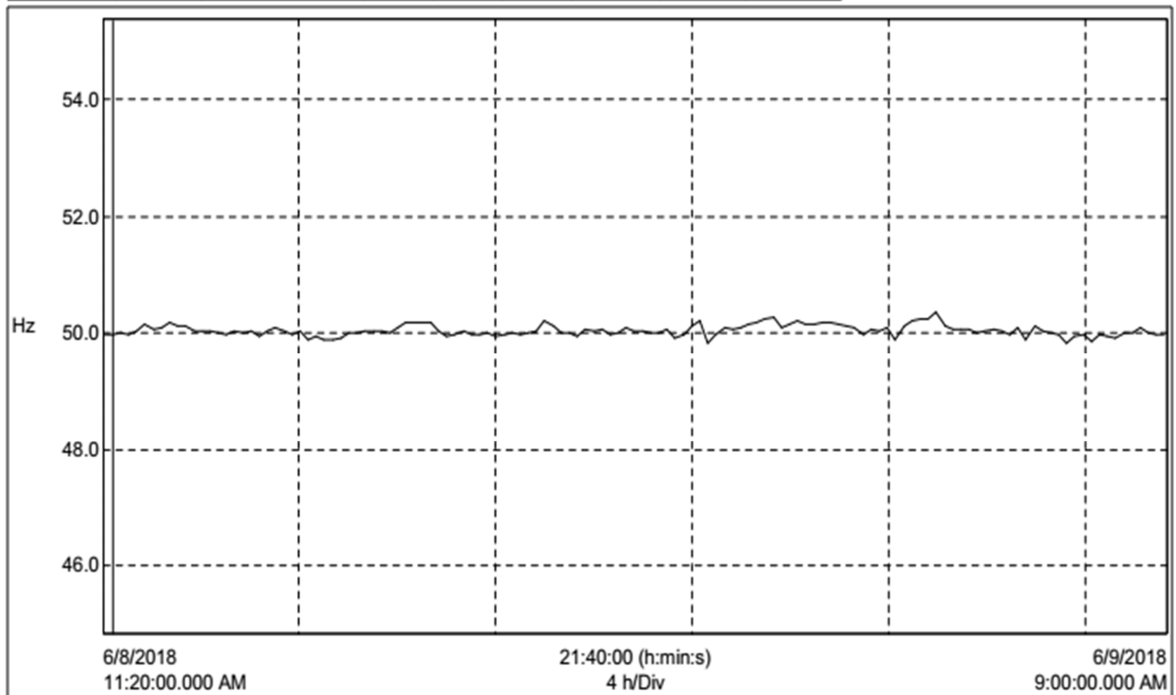
Recording Start Date	6/8/2018
Recording Duration	21:50:00 (h:min:s)
Instrument ID	C.A 8335 - 212306 2.6
Database File Name	Trend ERSTE_1.dvb
Instrument Configuration	Connection Type: 3-Phase 3-Wire A193/MA193 AmpFLEX Reactive values (var) calculation: With Harmonics
Operator Name: Erste Telila	Site Name: Chemical Industry corporation Mughar Cement Factory
Comments	

Qualistar+ (Trend ERSTE_1) - Cover Sheet,





Appendix A1: Inverter fundamental frequency variation

[illegible]

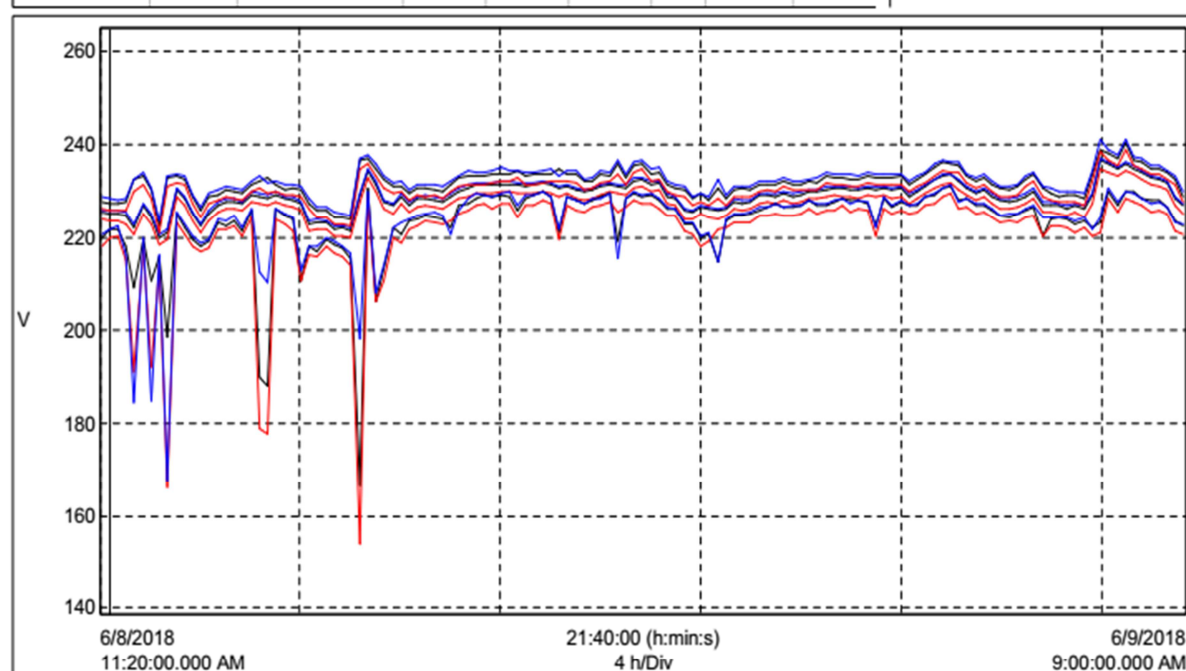
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Channel 2	100.0
Channel 3	100.0
Channel 4	100.0
Channel 5	100.0
Channel 6	100.0
Channel 7	100.0
Channel 8	100.0
Channel 9	100.0
Channel 10	100.0
Channel 11	100.0
Channel 12	100.0
Channel 13	100.0
Channel 14	100.0
Channel 15	100.0
Channel 16	100.0
Channel 17	100.0
Channel 18	100.0
Channel 19	100.0
Channel 20	100.0
Channel 21	100.0
Channel 22	100.0
Channel 23	100.0
Channel 24	100.0
Channel 25	100.0
Channel 26	100.0
Channel 27	100.0
Channel 28	100.0
Channel 29	100.0
Channel 30	100.0
Channel 31	100.0
Channel 32	100.0
Channel 33	100.0
Channel 34	100.0
Channel 35	100.0
Channel 36	100.0
Channel 37	100.0
Channel 38	100.0
Channel 39	100.0
Channel 40	100.0
Channel 41	100.0
Channel 42	100.0
Channel 43	100.0
Channel 44	100.0
Channel 45	100.0
Channel 46	100.0
Channel 47	100.0
Channel 48	100.0
Channel 49	100.0
Channel 50	100.0
Channel 51	100.0
Channel 52	100.0
Channel 53	100.0
Channel 54	100.0
Channel 55	100.0
Channel 56	100.0
Channel 57	100.0
Channel 58	100.0
Channel 59	100.0
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Channel 66	100.0
Channel 67	100.0
Channel 68	100.0
Channel 69	100.0
Channel 70	100.0
Channel 71	100.0
Channel 72	100.0
Channel 73	100.0
Channel 74	100.0
Channel 75	100.0
Channel 76	100.0
Channel 77	100.0
Channel 78	100.0
Channel 79	100.0
Channel 80	100.0
Channel 81	100.0
Channel 82	100.0
Channel 83	100.0
Channel 84	100.0
Channel 85	100.0
Channel 86	100.0
Channel 87	100.0
Channel 88	100.0
Channel 89	100.0
Channel 90	100.0
Channel 91	100.0
Channel 92	100.0
Channel 93	100.0
Channel 94	100.0
Channel 95	100.0
Channel 96	100.0
Channel 97	100.0
Channel 98	100.0
Channel 99	100.0
Channel 100	100.0

Frequency (Hz)			
Date	Time	Val	Units
6/8/2018	11:30:00.000 AM	49.990	Hz
6/8/2018	11:40:00.000 AM	49.990	Hz
6/8/2018	11:50:00.000 AM	50.000	Hz
6/8/2018	12:00:00.000 PM	49.970	Hz
6/8/2018	12:10:00.000 PM	50.040	Hz
6/8/2018	12:20:00.000 PM	50.160	Hz
6/8/2018	12:30:00.000 PM	50.060	Hz
6/8/2018	12:40:00.000 PM	50.090	Hz
6/8/2018	12:50:00.000 PM	50.180	Hz
6/8/2018	1:00:00.000 PM	50.120	Hz
6/8/2018	1:10:00.000 PM	50.130	Hz
6/8/2018	1:20:00.000 PM	50.030	Hz
6/8/2018	1:30:00.000 PM	50.030	Hz
6/8/2018	1:40:00.000 PM	50.040	Hz
6/8/2018	1:50:00.000 PM	50.010	Hz
6/8/2018	2:00:00.000 PM	49.980	Hz
6/8/2018	2:10:00.000 PM	50.030	Hz
6/8/2018	2:20:00.000 PM	50.010	Hz
6/8/2018	2:30:00.000 PM	50.050	Hz

6/8/2018 - 11:30:00.000 AM
Value
49.99 — Frequency

Appendix A2: RMS value of current and voltage

Name	Date	Time	Avg	Min	Max	Units	Duration	Units
V1 RMS	6/8/2018	11:20:00.000 AM	229.027	220.100	236.600	V	21:50:00	(h:min:s)
V2 RMS	6/8/2018	11:20:00.000 AM	227.438	218.400	235.000	V	21:50:00	(h:min:s)
V3 RMS	6/8/2018	11:20:00.000 AM	229.541	220.700	237.100	V	21:50:00	(h:min:s)
V1 RMS MAX	6/8/2018	11:20:00.000 AM	231.937	222.500	240.400	V	21:50:00	(h:min:s)
V2 RMS MAX	6/8/2018	11:20:00.000 AM	230.408	221.300	239.000	V	21:50:00	(h:min:s)
V3 RMS MAX	6/8/2018	11:20:00.000 AM	232.656	223.800	241.200	V	21:50:00	(h:min:s)
V1 RMS MIN	6/8/2018	11:20:00.000 AM	223.433	166.500	231.200	V	21:50:00	(h:min:s)
V2 RMS MIN	6/8/2018	11:20:00.000 AM	221.188	154.100	229.600	V	21:50:00	(h:min:s)
V3 RMS MIN	6/8/2018	11:20:00.000 AM	223.706	167.700	231.500	V	21:50:00	(h:min:s)



Channel Name : V1 RMS

Voltage Ratio : 1

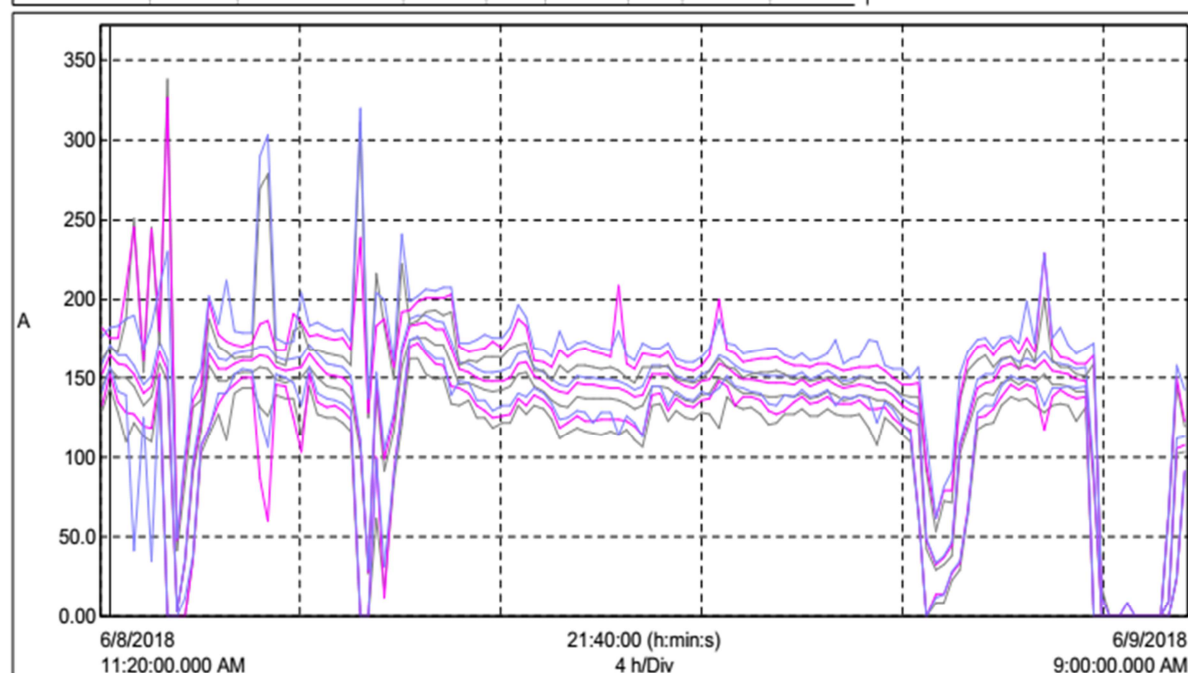
V1 RMS (V)			
Date	Time	Val	Units
6/8/2018	11:30:00.000 AM	225.50	V
6/8/2018	11:40:00.000 AM	225.30	V
6/8/2018	11:50:00.000 AM	225.20	V
6/8/2018	12:00:00.000 PM	224.70	V
6/8/2018	12:10:00.000 PM	222.40	V
6/8/2018	12:20:00.000 PM	226.90	V
6/8/2018	12:30:00.000 PM	224.50	V
6/8/2018	12:40:00.000 PM	220.10	V
6/8/2018	12:50:00.000 PM	221.30	V
6/8/2018	1:00:00.000 PM	230.40	V
6/8/2018	1:10:00.000 PM	228.40	V
6/8/2018	1:20:00.000 PM	225.20	V
6/8/2018	1:30:00.000 PM	222.50	V
6/8/2018	1:40:00.000 PM	225.30	V

6/8/2018 - 11:30:00.000 AM

Value

225.3 — V1 RMS
 223.8 — V2 RMS
 226.0 — V3 RMS
 227.5 — V1 RMS MAX
 226.0 — V2 RMS MAX
 228.4 — V3 RMS MAX
 221.8 — V1 RMS MIN
 220.0 — V2 RMS MIN
 222.0 — V3 RMS MIN

Name	Date	Time	Avg	Min	Max	Units	Duration	Units
A1 RMS	6/8/2018	11:20:00.000 AM	125.404	0.000	175.400	A	21:50:00	(h:min:s)
A2 RMS	6/8/2018	11:20:00.000 AM	132.231	0.000	185.700	A	21:50:00	(h:min:s)
A3 RMS	6/8/2018	11:20:00.000 AM	136.798	0.000	189.900	A	21:50:00	(h:min:s)
A1 RMS MAX	6/8/2018	11:20:00.000 AM	151.080	0.000	338.000	A	21:50:00	(h:min:s)
A2 RMS MAX	6/8/2018	11:20:00.000 AM	156.550	0.000	325.500	A	21:50:00	(h:min:s)
A3 RMS MAX	6/8/2018	11:20:00.000 AM	163.168	0.000	319.000	A	21:50:00	(h:min:s)
A1 RMS MIN	6/8/2018	11:20:00.000 AM	103.992	0.000	162.500	A	21:50:00	(h:min:s)
A2 RMS MIN	6/8/2018	11:20:00.000 AM	109.351	0.000	172.500	A	21:50:00	(h:min:s)
A3 RMS MIN	6/8/2018	11:20:00.000 AM	112.198	0.000	176.500	A	21:50:00	(h:min:s)



Channel Name : A1 RMS

Current Ratio : 1

A1 RMS (A)			
Date	Time	Val	Units
6/8/2018	11:30:00.000 AM	144.90	A
6/8/2018	11:40:00.000 AM	156.30	A
6/8/2018	11:50:00.000 AM	150.60	A
6/8/2018	12:00:00.000 PM	150.70	A
6/8/2018	12:10:00.000 PM	144.90	A
6/8/2018	12:20:00.000 PM	133.20	A
6/8/2018	12:30:00.000 PM	138.20	A
6/8/2018	12:40:00.000 PM	159.20	A
6/8/2018	12:50:00.000 PM	147.80	A
6/8/2018	1:00:00.000 PM	2.9000	A
6/8/2018	1:10:00.000 PM	34.000	A
6/8/2018	1:20:00.000 PM	90.200	A
6/8/2018	1:30:00.000 PM	116.20	A
6/8/2018	1:40:00.000 PM	158.00	A

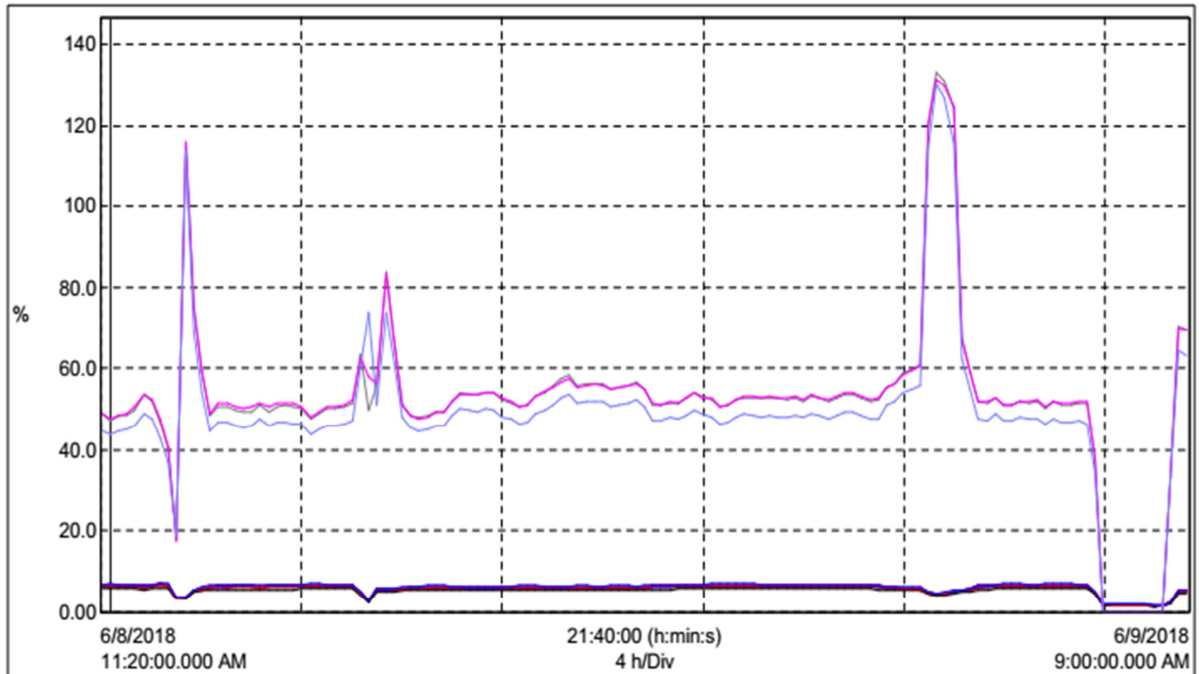
6/8/2018 - 11:30:00.000 AM

Value

156.3 — A1 RMS
 165.0 — A2 RMS
 170.9 — A3 RMS
 169.0 — A1 RMS MAX
 176.0 — A2 RMS MAX
 182.0 — A3 RMS MAX
 144.0 — A1 RMS MIN
 152.5 — A2 RMS MIN
 157.5 — A3 RMS MIN

Appendix A3: Inverter THD value of voltage and current

Name	Date	Time	Avg	Min	Max	Units	Duration	Units
A1 THD	6/8/2018	11:20:00.000 AM	52.363	0.000	133.200	%	21:50:00	(h:min:s)
A2 THD	6/8/2018	11:20:00.000 AM	52.576	0.000	131.500	%	21:50:00	(h:min:s)
A3 THD	6/8/2018	11:20:00.000 AM	48.644	0.000	130.100	%	21:50:00	(h:min:s)
U1 THD	6/8/2018	11:20:00.000 AM	5.820	1.500	6.800	%	21:50:00	(h:min:s)
U2 THD	6/8/2018	11:20:00.000 AM	5.786	1.600	6.700	%	21:50:00	(h:min:s)
U3 THD	6/8/2018	11:20:00.000 AM	6.107	1.800	7.100	%	21:50:00	(h:min:s)
V1 THD	6/8/2018	11:20:00.000 AM	5.350	1.600	6.200	%	21:50:00	(h:min:s)
V2 THD	6/8/2018	11:20:00.000 AM	6.154	1.600	7.100	%	21:50:00	(h:min:s)
V3 THD	6/8/2018	11:20:00.000 AM	6.314	1.800	7.300	%	21:50:00	(h:min:s)



Channel Name : A1 THD

A1 THD (%)			
Date	Time	Val	Units
6/8/2018	11:30:00.000 AM	49.000	%
6/8/2018	11:40:00.000 AM	47.400	%
6/8/2018	11:50:00.000 AM	48.600	%
6/8/2018	12:00:00.000 PM	48.700	%
6/8/2018	12:10:00.000 PM	50.000	%
6/8/2018	12:20:00.000 PM	53.600	%
6/8/2018	12:30:00.000 PM	52.100	%
6/8/2018	12:40:00.000 PM	46.800	%
6/8/2018	12:50:00.000 PM	40.300	%
6/8/2018	1:00:00.000 PM	18.100	%
6/8/2018	1:10:00.000 PM	115.90	%
6/8/2018	1:20:00.000 PM	75.200	%
6/8/2018	1:30:00.000 PM	59.400	%
6/8/2018	1:40:00.000 PM	48.400	%

6/8/2018 - 11:30:00.000 AM

Value

6.600 — U1 THD
 6.500 — U2 THD
 6.900 — U3 THD
 6.000 — V1 THD
 6.900 — V2 THD
 7.100 — V3 THD
 47.40 — A1 THD
 47.70 — A2 THD
 43.70 — A3 THD

Appendix B: Induction motor parameters for five and seven level CML inverters

The induction motor used for the simulation has the following parameters. It's a three phase squirrel cage motor with the stator reference frame.

- $P = 5.4\text{HP}(4\text{KW})$
- $V_{\text{rms}}=400\text{V}$
- $f = 50\text{Hz}$
- $R_s=1.405\Omega$
- $L_s=0.005839\text{H}$
- $R_r=1.395\Omega$
- $L_r=0.005839\text{ H}$
- $L_m=0.1722\text{ H}$
- $J=0.0131\text{ Kg.m}^2$
- $F=0.002985\text{ N.m.s}$
- $V_{\text{dc}}=100\text{ V}$
- $R=10\text{k}\Omega$
- $L=0.15\text{mH}$