Design and Optimization of Junction-Less Nanowire Tunnel FET for Low-Power Analog Application

Rabiya Abdulnassir Hussein

A Thesis Submitted To

The Department of Electronics and Communication Engineering School of Electrical and Computing

Presented in Partial Fulfillment of The Requirement for the Degree of Master's in

Electronics and Communication Engineering

Office of Graduate Studies

Adama Science and Technology University

June 2023

Adama, Ethiopia

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APPROVAL PAGE OF M.SC THESIS

We hereby confirm that the thesis review committee's recommendations and suggestions have been successfully incorporated into the final thesis entitled "**Design and Optimization of Junction-Less Nanowire Tunnel FET for Low-Power Analog Application**" by Rabiya Abdulnassir Hussein.

Major Advisor	Signature	Date
Co-advisor	Signature	Date

We, the undersigned, members of the Board of Examiners of the thesis by Rabiya Abdulnassir Hussein have read and evaluated the thesis entitled "**Design and Optimization of Junction-Less Nanowire Tunnel FET for Low-Power Analog Application**" and examined the candidate during open defense. This is, therefore, to certify that the thesis is accepted for partial fulfillment of the requirement of the degree of Master of Science in Electronics and Communication Engineering.

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Final approval and acceptance of the thesis is contingent upon submission of its final copy to the Office of Postgraduate Studies (OPGS) through the Department Graduate Council (DGC) and School Graduate Committee (SGC).

Department Head	Signature	Date
School Dean	Signature	Date
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DECLARATION

I hereby declare that this Master Thesis, entitled "Design and Optimization of Junction-Less Nanowire Tunnel FET for Low-Power Analog Application" is my original work. That is, it has not been submitted for the award of any academic degree, diploma, or certificate in any university. All sources of materials are used for this thesis have been duly acknowledged through citation.

Rabiya Abdulnassir Hussein _____ _____

Student Name Signature Date

RECOMMENDATION

We, the advisors of this thesis, hereby certify that we have read the revised version of the thesis entitled "**Design and Optimization of Junction-Less Nanowire Tunnel FET for Low-Power Analog Application**" prepared under our guidance by Rabiya Abdulnassir Hussein submitted in partial fulfilment of the requirements for the degree of Masters of Science in Communication Engineering. Therefore, we recommend the submission of a revised version of the thesis to the department following the application procedures.

Dr. Avtar Singh	_____	_____
Major Advisor	Signature	Date
DR. Dereje Tekilu	_____	_____
Co-advisor	Signature	Date

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2-D	Two Dimensional
3-D	Three Dimensional
BGN	Bandgap narrowing
BTBT	Band-to-band tunneling
CB	Conduction Band
DC	Direct current
DIBL	Drain-induced barrier-lowering
EOT	Effective Oxide thickness
RF	Radio Frequency
JLTFET	Junction less Tunnel Field Effect Transistors
GAA	Gate All Around
MOSFETs	Metal oxide semiconductor Field effect transistor
SS	Subthreshold slop
SCE	Short- channel effects
SOI	Silicon on insulation
SRH	Shockley- Read-Hall
TCAD	Technology Computer-Aided Design
TFET	Tunnel Field Effect transistor
VB	Valance Band

ABSTRACT

Researchers worldwide are engaged in developing innovative approaches to achieve the objectives outlined in the International Technology Roadmap for Semiconductors, with the ultimate goal of sustaining Moore's Law. Among various studies, some are focused on novel device architecture, while others are exploring methods for improved channel control. In this pursuit, the tunnel FET and the junction-less FET have emerged as promising candidates for low-power applications. In this thesis we have studied the Junction-less nanowire Tunnel Field Effect Transistor (JLN-TFET), which takes the combined advantage of Tunnel Field Effect Transistor (TFET) and junction-less Field Effect transistor (JLFET) by utilizing Channel Engineering and Gate Engineering. Gate Engineering modulates the carrier density in the nanowire channel and creates a tunneling barrier that allows for effective charge transport. Whereas Channel Engineering is used to modify the channel region. The integration of gate engineering and channel engineering was explored with a Hetero-structure device comprising germanium (Ge) and Silicon (Si). A uniform high doping concentration (10-19 cm-3) has been used to make the structure junction-less. The gate work function is set at 4.5 eV while the source work function is 5.93 eV. The optimized gate all around hetero junction less nanowire tunnel field effect transistor (GAA-H-JLNTFET) exhibit notable performance compare to junction less nanowire tunnel FET (JLTFET). Both the structures are compared and analyzed using the extensive TCAD simulation. As an application, the proposed structure was found suitable for the low power biosensor and to check the performance of the biosensor, sensitivity is calculated. The drain current is taken as the sensitivity parameter. The proposed structure GAA-H-JLNTFET exhibits the ON current (I_{ON}) $6.5x10^{-5}$ μA/m, the off current (I_{OFF}) measures $5.7x10^{-18}$ μA/m, the subthreshold slope (SS) is 12mV/Dec, and I_{ON}/I_{OFF} is $1.37x10^{13}$ which makes them immune to short channel effect and suitable to low power application in Nano regime. For the simulation and analysis, the Silvaco Atlas 2D simulator is used.

Keywords*: - Tunnel FET, Junction-less, subthreshold slope, high-k dielectric, Silvaco Atlas 2D, Hetero-structure, Junction-less nanowire Tunnel Field Effect Transistor*

CHAPTER ONE
INTRODUCTION

1.1 Motivation

Arise from the limitations of traditional transistor technologies, such as CMOS, in achieving low-power operation. As technology scales down, transistors encounter challenges in reducing power consumption while maintaining performance. Tunnel FETs (TFETs) have emerged as a potential solution due to their ability to operate at lower supply voltage. However, TFETs have limitations in terms of low ON current. By focusing on the design and optimization of Junction-less Nanowire TFETs, this research aims to address this limitation, enhance the device ion, and reduce the subthreshold swing. The findings from this study will contribute to the development of low-power analog applications.

This chapter is organized as follows; it begins with an overview, operations, a Statement of the problem, the Objective of the study, the Significance of the study, and the scope of the study contribution of this study.

1.2 Introduction to TFET and Operations

Due to MOSFETs' inability to maintain their performance immunity to downscaling, the semiconductor industry has been searching for alternatives. The goal currently is to create devices that operate on a different concept from MOSFETs. According to the needs of the semiconductor industry today, researchers have proposed innovative devices with good prospects when compared to MOSFETs in terms of performance. The tunnel transistors were invented by T.Baba in 1992 as one of the promising alternatives to the conventional MOSFET based on the parameters like: - the possibility of subthreshold swing below 60mV/Dec, support low voltage and power, lower leakage current, immunity to Short channel effect (Turkane & Kureshi, 2016). TFET is a family of Field Effect transistors (FET), a voltage-controlled device with 3 terminals named Gate, Source, and Drain with a P-I-N structure. It uses an electric field for controlling the flow of current. When the voltage is applied at the gate terminal, it causes negative charge carriers to accumulate at the oxide-silicon interface, which results in the conduction of current at the channel in the case of n-TFETs. The gate terminal called the electrode is a heavily doped metal whose work functions are isolated from the silicon by a thin gate oxide layer.

However, TFET also suffers from different drawbacks, which are low ON current and Severe ambipolar Current (Iamb) (Abdi & Kumar, 2015). TFET required a highly doped junction, to achieve, Sharpe band-to-band at source, effective band-to-band tunneling (BTBT), and high ON current, which in return involved complex high temperature (Ionescu & Riel, 2011).Due to the dopant atoms migrating into the channel from source to drain, those requirements are difficult to meet (Damrongplasit, Kim, & Liu, 2013). Therefore, there is a need for a new way to solve this issue.

The term "Junction-less Transistor" refers to a revolutionary nanowire transistor that was recently developed (J.-P. Colinge et al., 2010). It is without a junction, there is no formation of the doping gradient. In addition, uses high doping concentration, which is uniformly doped for all region's source, channel, and drain side with (n+ or p+). Junction-less Transistors do not require expensive ultra-fast annealing techniques (B. Singh et al., 2016). Figure 1.1 shows the types of FET to get a clear idea of their difference.

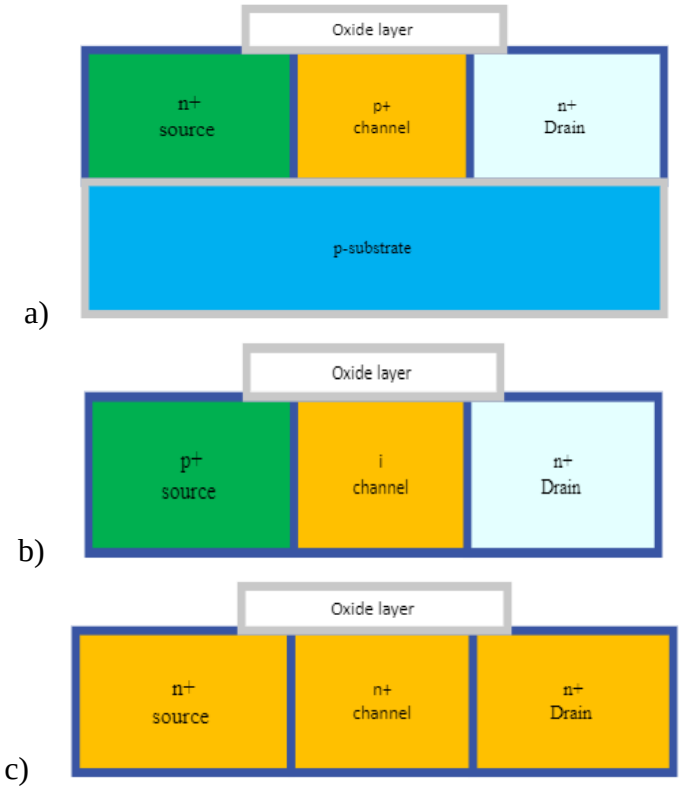


Figure 1.1 Device Structure a) MOSFET b) TFET c) JLTFET

Figure 1.2 shows the device structure, (a) shows the n-type MOSFTE which has four terminal (source, drain, gate and substrate or body), (b) device structure of N-type TFET where it has P-I-N structure and (c) shows n+ doped functionless transistor structure.

1.2.1 Transfer characteristics of TFETs

The behavior of the device's current flow in the ON state and OFF state is described. The transfer property of the transistor property is shown in the band energy diagram and work function and subthreshold slope is described.

1.2.2 OFF state

For TFETs to be in an OFF state (VGS=0, VDS>0), So in an off state the charge carrier from the conduction band of the channel will drift to the drain which results in the generation of current (Datta, Chattopadhyay, Mallik, & Omura, 2020). However, in TFET the source side is P-type, so the conduction band contains few electrons, which can inject very few electrons into the channel. This crates a significant OFF state current (Jossy & Vigneswaran, 2014). In the OFF state, the electron in the valence band of the source had no energy state to tunnel.

1.2.3 ON state

When VGS >0, VDS>0) the TFET is in an ON state, In the ON state current flows in the device and electrons are injected into the conduction band of the channel (Li, Liu, Wang, Chen, & Yang, 2017). In TFET charge carriers are created from the valency band of the source region, which makes a significant free electron in the conduction band of the P-type source. At the positive values of the gate voltage valance band and conduction ban will align, the gate voltage in which this arrangement of the source valance band and conduction band occurs is the start of the ON state of the TFET (Baruah, 2015). Whereas in junction less the work function difference between the gate and the nanowire silicon (~1.1eV) will shift the flat band voltage and turns the threshold voltage into a passive value. Which makes the JLT normally on State devices in ON state the device is in a flat band condition (J. P. Colinge et al., 2011).

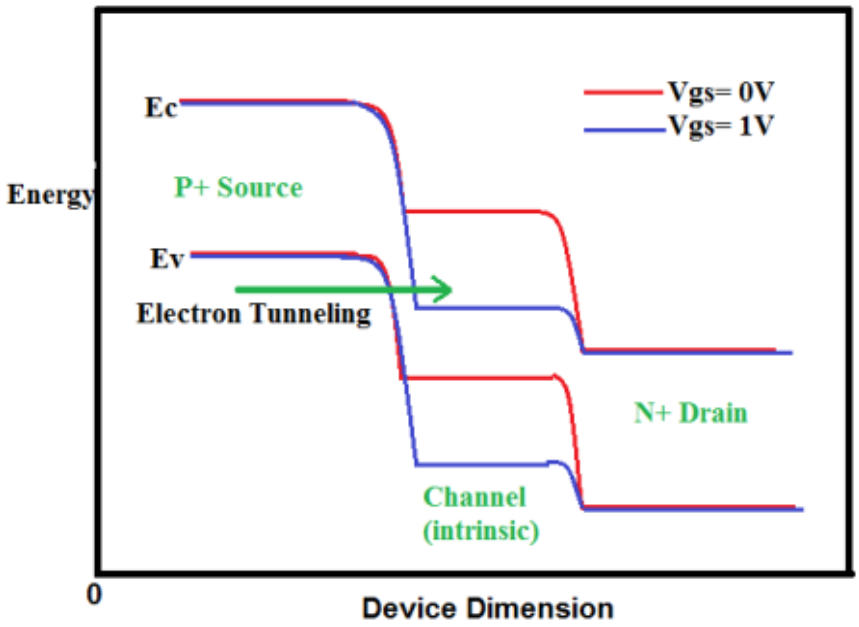


Figure 1.2 Band Energy Diagram

Figure 1.2 shows the ON and OFF state of the device where the red line is indicates OFF state and the blue one indicates the OFF state of the TFET devices.

1.2.4 Work function

A fundamental property of solid material, which is a work function and defined as an energy required to remove electrons from the fermi level to the vacuum. It is typically measured in electron volts (eV). Work function can be influenced by several factors including, the material composition, crystal structure, temperature, and surface preparation (Bergveld, Hendrikse, & Olthuis, 1998).

1.2.5 Subthreshold slope

Subthreshold slope (SS) is a measure of how sleepy the drain current increase as the gate voltage is increasing in the subthreshold region. A subthreshold region is a range below the sub-threshold voltage (Vt) where the transistor is fully turned on but still conducts some current. Whereas the subthreshold slope is measured in millivolts per decade (mV/Dec). The subthreshold slope (SS) is a critical parameter in the design of low-power circuits, as it dictates the minimum voltage necessary to maintain a desired level of current through the transistor. A smaller SS is highly desirable for low-power applications.

1.2.6 Property of Junction-less transistors (JLT)

- Without P-N Junction
- Carrier modulation is controlled by the gate work function and gate voltage
- High doping
- No doping gradient
- Normally ON state device
- Surface based conduction

1.3 Statement of the problem

In the semiconductor industry, performance, power consumption, and device reliability are currently top priorities. The feature size of the semiconductor device has scaled down to the nanoscale regime to increase devise performance and decrease power conception, which results in reliability difficulties. The development of low-power bio-sensing technology is essential for their integration into portable and wearable devices. However, traditional biosensors often required high operating voltage, limiting them in low-power applications.

1.4 Objective

1.4.1 General objectives

The main objective of this thesis is to study the structural design and optimization of Junction-less Nanowire Tunnel FET for low-power applications.

1.4.2 Specific objectives

The specific objectives of the study are

- Design the structure and evaluate current-voltage characteristics
- Analyzing different oxide types and work functions
- To achieve the highest possible ON current and lowest possible subthreshold slope (SS), Increasing the BTBT generation at the source channel interface
- To improve the device performance by adjusting parameters such as doping concentration, and the thickness of the dielectric and make it optimum to low power applications.

1.5 Significance of the Study

The significance of JLNTFET is to provide a high-performance and low-cost effective alternative to the traditional FET. This type of device is ideal for applications where power conception and performance are critical, such as high-speed computing and communication circuits. JLNTFET are built using nanowire technology, which involves depositing a thin layer of conducting material over the semiconductor substrate. This layered material serves as a tunneling barrier between the drain and the source of the device, allowing the electron to tunnel through the barrier, resulting in a high-performance device with a low-power application. The primary focus when discussing JLNTFET and low-power applications is on reducing power consumption while maintaining the device's performance. To do this it has been used high mobility materials like Germanium (Ge), high k material and high doping concentration. Somehow, the low voltage should be used to run the device to save energy. The proposed device have high OON current and low subthreshold slope which make it suitable for Switching and low power bio sensing application.

1.6 Scope of the Study

JLNTFET is an advanced type of TFET that is used for low-power applications due to its improved performance and low-power requirements. This paper discusses the effect of high-k material as a dielectric and the effect of using Hetero-Structure in the device and for application biosensor is used and optimized to work on low voltage. The study was done using an industry-grade design package, Silvaco Atlas TCAD (Silvaco), which can realistically represent and simulate the TFET structure using JLTFET. It has an efficient tool for designing, simulating, and eventually recording the desired performance and characteristics, which can then be processed further. This thesis focuses on the design and optimization of JLNTFET for low-power analog applications.

1.7 Limitations of the Study

The fabrication process has not been included and analytical analyses have not been included in this thesis.

1.8 Contribution

This thesis uses a combination of Gate engineering and Dielectric engineering for low-power applications and application biosensors have been included. The thesis includes the following difference from those (P. Kumar & Raj, 2022).

- Use of Hetero-Structure (Si and Ge)
- Substitution of low dielectric (Sio2) with high-k dielectric (Hfo2)
- Improved I_{ON} maintaining the I_{ON}/ I_{OFF} ratio
- Reduction of the subthreshold slope (SS)
- Applied on Biosensor

1.9 Organization of the Thesis

This thesis discusses the design and optimization of Junction-less Tunnel FET for low-power analog applications for the fulfillment of the master program.

The first chapter, chapter 1, provides the introduction part of the study, the problem statement, the Objective of the study, the significance of the study, the contribution, and limitations.

In next chapter, chapter2 discusses the review of the existing literature on tunnel FET AND Junction-less structure as hetero-structure Gate Al Around structure and comparison summery of the existed literature

In the chapter3, simulation methodology, device structure, software used Silvaco Atlas, simulation flow chart, biosensor application, and device structure

Chapter 4 discusses the result and discussion for the proposed structure, Performance description of GAA-H-JLTFET and Application of GAA-H-JLNTFET as low power Biosensor

Final Chapter 5 provides a conclusion and some recommendation as future woks

CHAPTER TWO
LITERATURE REVIEW

2.1 Overview

The development of integrated circuit technology has brought a new era of electronics with tremendous computational capacity. The most typical MOSFET dimensions have continued to be decreased by research and development efforts in the electronics community over the past few decades, enabling better circuit densities and greater functionality at lower prices. The co-founder of Intel, Gordon Moore, anticipate that semiconductor chips would double in power every two years and eventually shrinks to the point that they could be installed in the building, vehicles, and mobile devices (Goswami, Ghosh, & Asthana, 2014).

With the resource provided by recent development in the semiconductor industry different techniques investigated for further reducing the size of transistor density and improving performance. Traditional transistor MOSFETs are dependent on semiconductor Junction that is silicon on insulation (SOI) by doping atoms to produce p-type and n-type area. However, the MOSFET's performance is limited to different scaling issues, such as drain-induced barrier lowering (DIBL), short channel effect (SCE), Velocity saturation, etc. (Chaudhry & Kumar, 2004; Troutman, 1979). Scaling down MOSFETs devices channel length and oxide thickness decrease while substrate doping increases (Dennard scalability). However, due to DIBL and SCE channel length and oxide thickness-scaling technology experienced increasing in IOFF (Leakage current).

Since the transistor needs to have a steep gradient in coping concertation, shrinking their size to the lower end of the nanoscale makes it difficult to maintain connection distance from one other. Realizing junction-less transistors is among the most promising approaches to solving this problem (Nowbahari, Roy, & Marchetti, 2020).

The concept of the Junction-less transistor (JLT) was first introduced in 1920 by J.E.Lilienfeld (Edgar, 1930). The junction-less transistor is a device that characteristic lacks a P-N junction, and no doping concentration gradient. It makes the manufacturing of transistors smaller than 10nm easier. To say the device is junction-l to condition needs to be satisfied, first, the whole regions should be doped with a high uniform doping concentration (10-19), and second, the

channel thickness must be within 10 Nanometers (nm) (Ansari, Chaudhary, Sunkaria, Singh, & Raj, 2022).

2.2 Review of related work

(Asthana, Ghosh, Rahi, & Goswami, 2014) has proposed a SOI Hetero-Junctionless Tunnel FET for ultra-low power switching applications. They used Hfo2 as gate dielectric and the doping concertation used is $10^{-18}cm^{-3}$. They investigate transconductance (Gm), and output conductance GD. They have found ION ~0.23mAμm-1 I_{OFF} ~$2.2x10^{-17}$ Aμm-1, I_{ON}/I_{OFF} of ~1013, Vth of 0.11V DIBL of ~93mV V-1 subthreshold slope (SS) ~12 mV/Dec.

A Gate All-Around A vertical junction-less nanowire TFET has been proposed by (P. Kumar & Raj, 2022) they have optimized the structure varying different device parameters like, oxide thickness variation, and work function variation, for the gate region. They observed that as the work function is reducing the current in the drain side is increasing, they have used a uniform doping concertation for all side source, channel, and drain sides which is 10-19cm-3. By maintaining, the lower space between the conduction band of the channel and the valence band of the source the tunneling mechanism was archived at the source channel interface.

(Rahimian & Fathipour, 2016) has proposed an asymmetric Junction less nanowire they have used a dielectric pocked between and source and channel interface without the need for any separate implantation or epitaxial growth. The source side n+ pocket provides a reduction of tunneling width at the source-to-channel interface when the device is in on state.

(Rahimian & Fathipour, 2017) They proposed Junction-less nanowire TFET using Hetero-gate-dielectric. They have induced a local dip in the conduction band edge at the tunneling junction which creates an abrupt transition between the on and off-states. They have used a platinum (Pt) contact region to convert the n+ doped region into P+ region with a 5.93eV work function on the source side. They have used non-local band-to-band tunneling (BTBT). The difference between the high-k and Sio2 creates a band diagram modification. A uniform doping concertation of 10^{-19} cm^{-3} and achieving a subthreshold of 45 mV/Dec, I_{ON} $8.6x10^{-6}$ $A\mu m^{-1}$ I_{OFF} $1.1x10^{-11}$ $A\mu m^{-1}$, I_{ON}/I_{OFF} of ~15 .

(Ragavendran & Ramachandran, 2018) they proposed a Hetero-structure, which contains a different material source and channel drain, without any metallurgical junctions between them. The device has a control gate (Cg) and Auxiliary gate. The doping concertation is $10^{-19}cm^{-3}$

through the source to channel-drain. They used hafnium oxide, and Sio2 as gate oxide and spacer respectively between the control gate and auxiliary gate. Aluminum is used for the control gate with work function 4.2eV and platinum for auxiliary gate work function 5.2eV.

(Ghosh & Akram, 2013) they proposed a double gate Junction less Tunnel field effect transistor. They investigate a double gate, which uses two gate two isolate (control gate and polar gate) that uses two different work function to make it behave like TFET. In the simulation they have used a high-k material which is TiO2 and with gate length 20nm. They have obtained subthreshold slop (SS) of ~38mV/Decade, I_{ON}/I_{OFF} ratio of ~$6x10^{8}$.

(Medhi, 2014) has proposed A junction less double-gate TFET using a charge plasma concept which forms a source and drain region without doping by choosing appropriate work function

For both drain and source electrodes. They study the threshold voltage, as the length of the channel is almost zero. They found a subthreshold slope of 56.7mV/decade with a channel length of 50nm

(K. Kumar, Kumar, & Sharma, 2023) They proposed Charge plasma based JLTFET using novel coalescence of SiGe/GaAs and Heterogeneous gate dielectric and investigate the electrical performance improvement. Their work contains a dual-dielectric material with gate length 20nm. The device contains SiGe compound for the source side and GaAs compound at drain side and channel. They obtain I_{ON} of $6.4x10^{-5}$ $A\mu m^{-1}$ I_{OFF} $1.7x10^{-16}$ $A\mu m^{-1}$ and I_{ON}/ I_{OFF} $3.7x10^{11}$.

(Nigam, Singh, & Kwatra, 2021) has proposed Stack based oxide polarity JLTFET in the presence of interface trap charges, The design include a Heterogeneous gate dielectric polarity gate by making a high-k gate dielectric which is HfO2 on the tope of low-k gate dielectric which is SiO2 layer to improve the device performance. This stack approach of oxides leads to a decrease in leakage current at the gate-channel interface by maintenance quality of the device. They have analyzed the study of analog and RF parameters. The study has been compared with a polarity gate JLTFET structure and shows an improvement.

Table 2. 1: Summery of different Junction less device structure

Author	Title	Performance	Limitations
(P. Kumar & Raj, 2022	Parametric investigation and Design of Junction-less nanowire Field effect transistor	Studied the effect of oxide thickness, gate length, work function, and length of nanowire on the drain current.	Low I_{ON}
Rahimian & Fathipour, 2016	Asymmetric Junction less nanowire TFET with built in n+ source pocket emphasizing on energy band modifications	They have implemented a pocket on the source side and achieves a high I_{ON}	Low I_{ON}/I_{OFF} and ~38 SS
Rahimian & Fathipour, 2017	Improvement of electrical performance in junction less nanowire TFET using Hetero-dielectric	They have used a low-k and high-k dielectric	Comparatively Low and I_{ON}
K. Kumar, Kumar, & Sharma, 2023	Electrical performance improvement of charge plasma based junction less TFET using novel coalescence of SiGe/GaAs and heterogeneous gate dielectric	They work on 20nm dual-dielectric with dual gate with different work function and they study the analog parameters like trans-conductance.	Low I_{ON}/I_{OFF}
Asthana, Ghosh, Rahi,& Goswami, 2014	Optimal design for high performance H-JLTFET using HfO_2 as gate dielectric for ultra-low power switching application	They were able to achieve a better I_{ON}. it is work on very low power vg=0.7	The effects of the oxide used is not included
Ragavendran & Ramachandran, 2018	Low power and low area Junction less FETs	Studies the how hetero-structure can achieve a high on current.	Only the effect of hetero- and homo structure is discussed

CHAPTER THREE

SIMULATION METHODOLOGY AND DEVICE STRUCTURE

3.1 Overview

This section lists software requirements, and simulation parameter flow chart. Device structure, design parameter, and comparison of the device structure of TFETs.

3.2 Material Requirement (software)

- Silvaco Atlas technology computer-aided design (TCAD) version of 5.5.10.R
- Origin software
- Visio software

In this thesis, the simulation and design of the device structure was done using a 2-D Silvaco Atlas simulator. Origin software is used for graphical analysis and clarifying the graphical result of Silvaco. Whereas Visio for doing the structure and flow-chart of the simulation process.

3.2.1 Description of simulation Software

The Silvaco Atlas TCAD is a one, two, and three dimensional device simulator. It is a series of tools for process and device simulation that enables users to perform and graphically examine the outcomes of the electrical characteristics i.e. (ID_VG) of the device and simulated based semiconductor design. Atlas framework can address both analog and digital application areas (Santa Clara, 2014).

3.2.2 Atlas input and outputs

In atlas simulation, there are two input files. The first one consists of an Atlas command text file. The second input defines the structure file. Additionally, Atlas simulator generated three output files those are Runtime output, indicates the simulation's progress and error, log file that store values of the voltage and current for all terminals, a lastly the solution file, which store two -dimensional (2-D) variable inside device at specific bias points (Santa Clara, 2014).

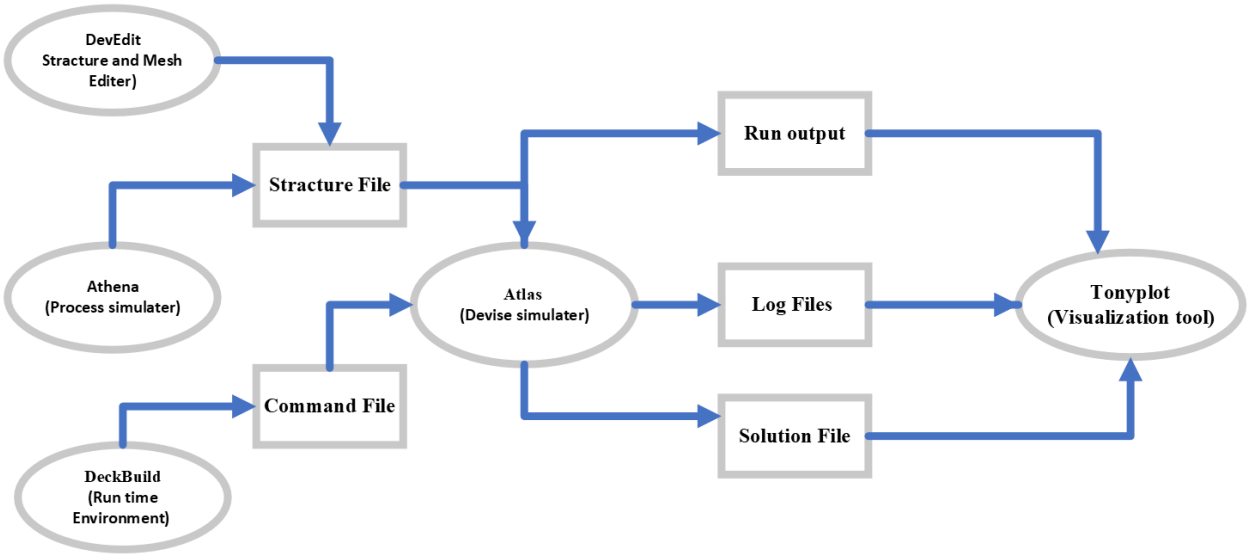


Figure 3. 1: Atlas input and output files (Santa Clara, 2014)

3.2.3 Atlas Syntax

A command used to perform and execute is called Atlas command file. This file is an ASCII text file, which is created with in a DECK BUILD, which is an editor in Silvaco (Santa Clara, 2014).

3.2.4 Defining a structure

In Atlas, the structure of the devices can be specified in three methods. The first method is to read an existing structure from a file. ATLAS produces the device structure. The mesh, location, electrode positions, and structural doping are loaded using the MESH statement.

The second option is to use DECK BUILD Automatic Interface tools to transfer the ATHENA or DEVEDIT input structure. The third method uses the Atlas command language to build or create a structure. This study makes or generates all the structures using the ATLAS command language (Santa Clara, 2014).

3.3 Design Methodology

3.3.1 Simulation flow chart

Different Atlas programming steps are included in this section to simulate and design the structure, meshing defining, defining a region, doping of region, models, I-V characteristics, parameter extraction.

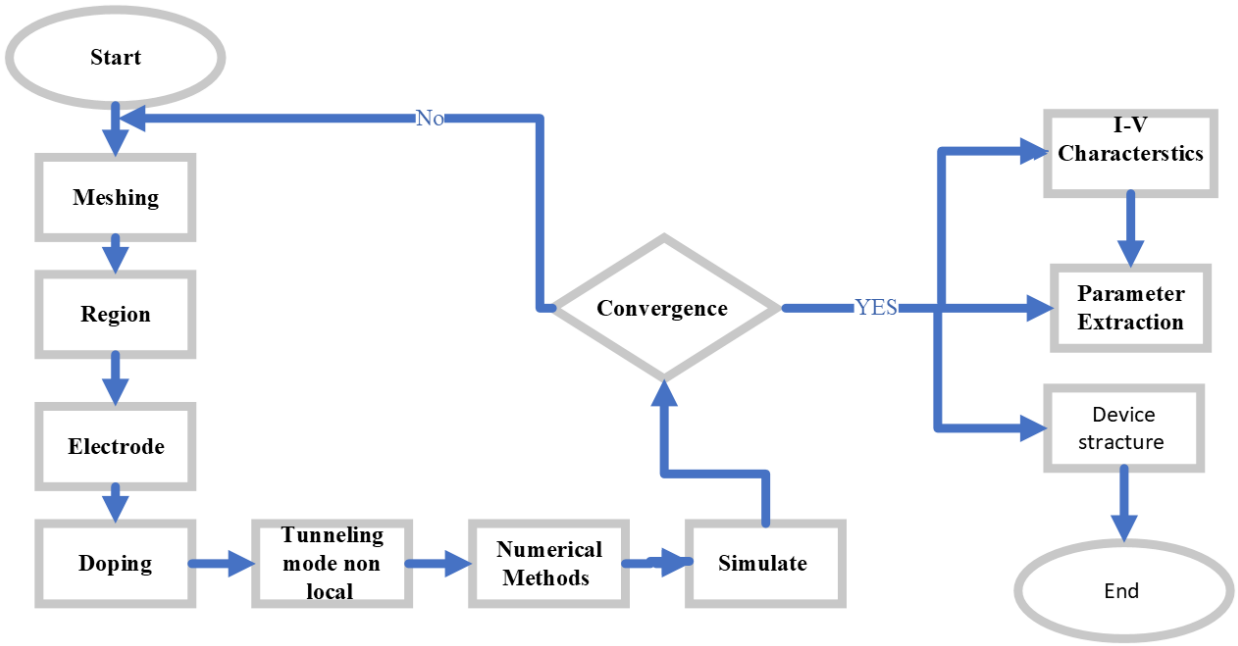


Figure 3.2: Atlas resolution algorithm of GAA-H-JLTFET

3.3.2 Simulation Procedures and Devices

The device structure of Gate All-Around (GAA) Junction less nanowire TFET follows the designing steps starting from Mesh, Region, Electrodes, Doping, Contact and work function and models, Methods as shown in table 3.1.

3.3.3 Meshing

It is a very critical part of the design, it defines the device structure in 2-D in Cartesian grid. The x-axis side mesh (X.mesh) occur on the left to the right and y-axis mesh (Y.mesh) is from bottom to top (Santa Clara, 2014).

3.3.4 Regions

Region is the statement, which separate the initial mesh into blocks and the material parameters; each block is given its own region number. In region definition the area the mesh location should be specified from the lowest to highest (Santa Clara, 2014). The region format is

Region < Region number> < location parameter > name=<material>

Table 3.1: Atlas command group

Group	Statements
Specification of Structure	Mesh, Region, Electrode, Doping
Specification of material and models	Material, Models, Contacts, Interfaces
Numerical models	Newton, Gummel, Block
Solution Specifications	Solve, Log, Load, Save
Analysis	Tony plot, Extraction

3.3.5 Electrode

For the electrical analysis electrode are introduced to the region once the region is established. The electrode can be given to any part of the region Atlas have electrode including Gate, Source, and drain electrodes. For the definition of the following command is used

Electrode<location parameter>name<electrode name>

The location of the parameter like x.max, x.min, y.min, and y.max they are defined in micrometers if the electrode are given the same name the they share the common electrical contact (Santa Clara, 2014).

3.3.6 Doping

In structural specification, doping is the last step. The doping statement assigns the doping level within the previously defined region statement. To specify the semiconductor doping method variety of feature can be added to the doping statement to specify whether the region doped is n-type or p-type. To define the doping the statement is as follow

Doping<distribution type><dopant type><position parameter>

There are Gaussian, Abrupt, and uniform doping profiles; however, the doping profile we use is uniform doping profile.

3.3.7 Material

This statement assigns a physical parameter to the mesh. The Atlas has already established material and parameters, which are crucial for the semiconductor and do not need to be altered. In silicon (Si) the location of the built-up tunnel connection, which has been extensively studied and documentations, for this study large models of library used from atlas.

3.3.8 Simulation models

The most common BTBT model in Silvaco Atlas is the local BTBT. Which is a model that approximates a barrier and assumes that the lateral electric field is constant throughout the tunneling area. However, a non-local BTBT model considers the electrical field change in the tunneling region. Therefore, a non-local dynamic BTBT model to simulate BTBT current in TFET accurately and, it is used that Kane BTBT model to find the generation carrier due to band to band tunneling. The model expressed.

$$G(E) = A\frac{|E|^2}{\sqrt{E_g}}\exp(-B\frac{E_g^{3/2}}{|E|}) \tag{3.1}$$

Where is |E| is the magnitude of an electric field, which is explained as $|E|=E_x + E_y$ and Eg is energy gap. However, the nonlocal BTBT is used in this study. Which is nonlocal in nature and considers the special variation of energy band. Furthermore, and it takes into account -the fact that the rate of generation and recombination at each place is not only dependent in electric field there (Medhi, 2014). Shockley-Read-Hall recombination model and Auger recombination had been included for high impurity concentration in the channel region. BGN band-gap-narrowing has been included for highly doped regions since all the regions are highly doped. The Fermi-Dirac model has been included to govern and decrease the charge carrier concentration. Both field dependent and concentration dependent mobility are included. Nonlocal BTBT is used for tunneling and the direction was specified in y.dir = 0.

After the device is designed and simulated, different numbers of parameters are obtained by drawing a cut line along an arbitrary direction specified by two-point in XY plane. The variation of different parameters, such as electric field (vertical and horizontal directions), electron concentration, Band gap energy, and the extraction of parameter as done by the simulator 2-D Atlas Silvaco simulator.

Table 3.2: Description of model used

Model	Syntax	Comments
Band-to-band tunneling (nonlocal)	BBT.NONLOCAL	Allows modeling of forward and reverse tunneling
Concentration Mobility	CONMOB	They are used for low-field mobility to the impurity
Field dependent mobility	FLDMOB	Field mobility
Auger recombination	AUGER	Used in high current density
Shockley-Read-Hall	SRH	Used in fixed recombination life time
Band-gap-narrowing	BGN	Used in heavily doped region
Lombardi (CVT) model	CVT	To account high field mobility effect

3.3.9 Output

The output statement has a default structure that contains several values such as electron concentration, electric field, doping I-V curve, etc. The output statement is (Santa Clara, 2014).

Output con.band val.band j.electron j.hole j.cocnduction ex.field ey.filed e.mobility h.mobility

3.3.10 Specification of solutions

For creating data, files in Atlas Simulator solve/log/save instructions are used. Those instructions (solve/log/save) work together to analyses and generate data. To analyses the device structure these statements are used drain current with respect to gate voltage (Santa Clara, 2014).

3.4 Device structure and simulation description

The design device structure is Gate All Around Junction-less Nanowire TFET (GAA-H-JLNTFET) with a Hetero-structure (Si and Ge) and high-k gate dielectric. The study of GAA-

H-JLNTFET is compared with a conventional silicon only JLTFET, as it is shown in figure 3.3 the Hetero-structure Si and Ge is included due to its advantages like enhance carrier transport, lower subthreshold slop (SS), tunable bandgaps, compatible with existing silicon technology, and reduce leakage current (IOFF) which make it suitable for low power analog applications. The higher the k value of Hfo2, the thinner layer can produce the same capacitance value as thicker sio2 layer. Which lead to a reduction in equivalent oxide thickness (EOT), which allows better integration and scaling of device. The channel length is 20nm and a metal work function, which kept constant at 4.5eV. The length of the source and the drain is 30nm. The all regions the source, drain and the channel doped with a uniform doping concentration that is (10-19 cm-3) (P. Kumar & Raj, 2022).

Table 3.3: List of Parameter used

Parameter	Values
Channel length and thickness	20nm and 15nm
Gate work function	4.5eV
Source length and thickness	27nm and 5nm
Drain length and thickness	27nm and 5nm
Channel doping	1e19 cm^{-3}
Source doping	1e19 cm^{-3}
Drain doping	1e19 cm^{-3}
Source work function	5.93eV
Dielectric length and thickness	74nm and 2nm

In the design structure all the regions are doped with a highly doping concentration with n+-type with no junction no doping concentration and the electric filed is controlled by the work function from the source and gate work function a voltage being applied to the gate terminal. The structure device profile in the figure 3.3

- Region one is SiO_2 it defined for all meshing dimension 74nm length and 13nm thickness
- Region two is HfO_2 layer 2nm top of the silicon substrate region 74nm length

- The third region is the Drain and channel regions 47nm length and 5nm thickness
- The fourth region is Ge region length of 27nm and 5nm thickness
- Region five is again HfO_2 layer 2nm top of the silicon substrate region 74nm length

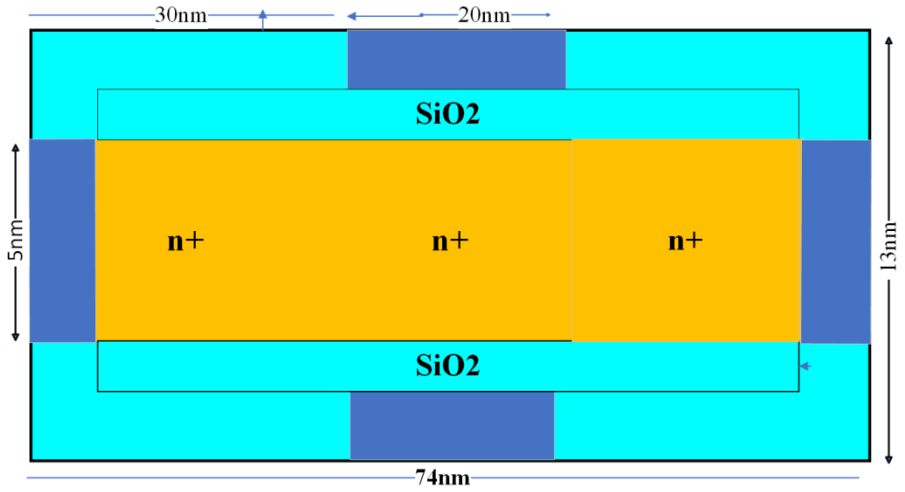
The doping profile of the device in figure 3.3.

- Uniform doping with n-type for region 3, 1e19 cm^{-3}
- Region 4 uniform doping n-type, 1e19 cm^{-3}

3.4.1 Dielectric materials

Table 3.4: List of Dielectric and their properties

Dielectric material	**Property**	
	Energy bandgap(eV)	Permittivity (K)
Sio_2	9	3.9
Hfo_2	5.7	25
Si_3N_4	5	7.5
Al_2O_3	8.7	9



a)

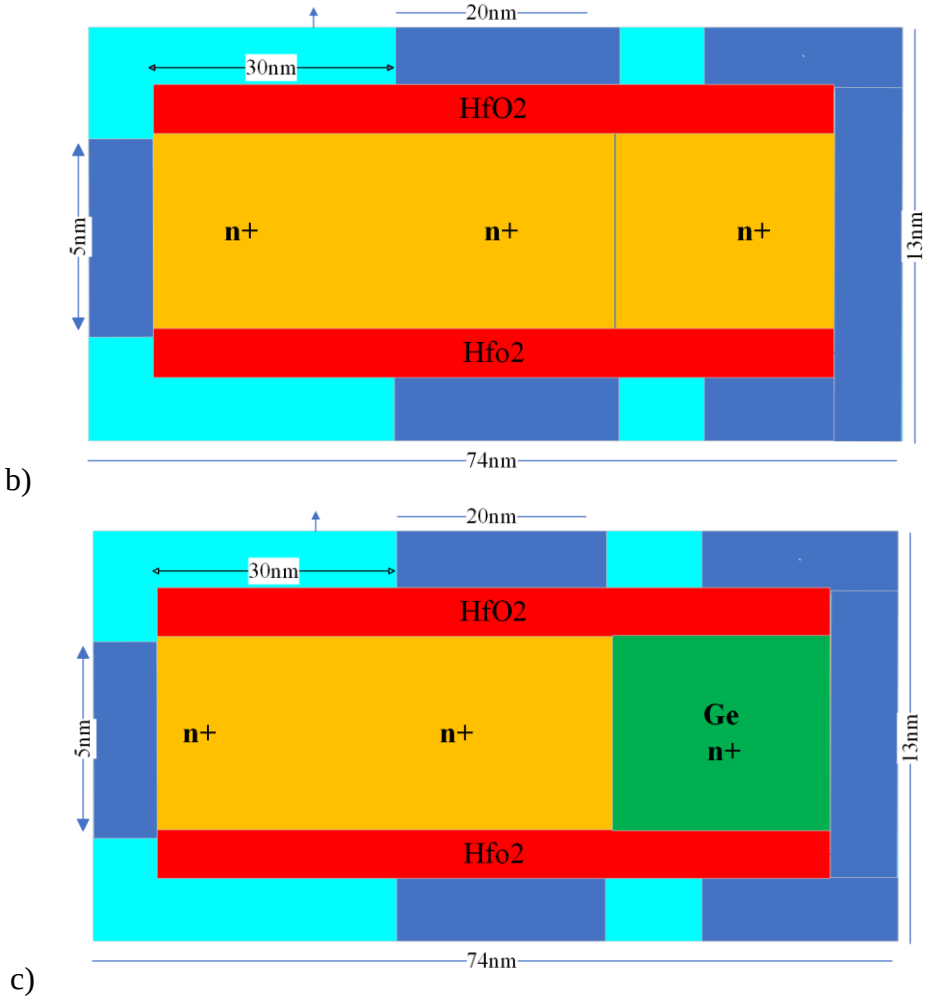


Figure 3.3: Device structure of a) conventional b) GAA-JLTFET c) GAA-H-JLTFEL

In figure 3.3 The 2-D device structure of the conventional JLTFET and GAA-H-JLNTFET structure is shown with the same parameter and dimension being defined except that the Hetero stricture and high- dielectric is used. Using Hetero-structure result in increasing the I_{ON} and reduction of the I_{OFF} and result in the reduction of the Subthreshold slop (SS).

3.4.2 Why Hetero-structure Silicon and Germanium

- It enhances carrier transport
- Help to achieve Lower SS
- Tunable bandgap by adjusting the Ge composition material
- Compatibility with silicon
- Si and Ge Hetero-structure can suppress the OFF-state Leakage current which result in improved performance

3.4.1 Why High-K dielectric (HfO_2)

- HfO_2 has high dielectric constant than SiO_2 which all HfO_2 in increased charge storage capacitance in the gate dielectric
- EOT (Equivalent Oxide Thickness), due to high K values thinner HfO_2 can give same as capacitance as thicker SiO_2 which lead in reduction in EOT and make the device suitable for scaling and integration.
- HfO_2 exhibit low gate leakage current which make it suitable for low-power applications

3.5 Biosensor application

3.5.1 Overview

Biosensors are becoming increasingly significant in human life as technology advances, and their widespread usage has restricted efforts by scholars to discover alternative methods for comprehending biomolecules (D. Singh et al., 2016). Due to their good detection ability, low-power conception, cheap cost, label-free molecule identifications dielectric modulated based FET (DM-FET) has drowned interest. However, as their technology advanced the device dimensions are scaled down which led to problems like short channel effect (SCE), off state leakage current redaction, high power dissipation which make in degradation of DM-FET. So, to address the above issues, different researchers proposed TFET based biosensors which work on the principal Band-to-band tunneling (BTBT) which allows the device, lower power dissipation, its steep sub-threshold swing (SS), High sensitivity, and quick response(Verma, Sharma, Pandey, Nigam, & Kondekar, 2017) time. Since TFET encounters a very sharp doping profile at the Junction the device fabrication complexity and cost are increased. So, to solve this problem JLTFET was introduced. JLTFET also has low I_{ON} so to address this issue GAA-H-JLNTFET structure was proposed.

3.5.2 The simulation steps

For the definition of region for the cavity after the mesh is defined the command used

Region number user. Material = d1 <location of the parameter>

Whereas this “d1“is defined like this, Material material=d1 user. Group = insulator

User. Default = oxide permittivity=5

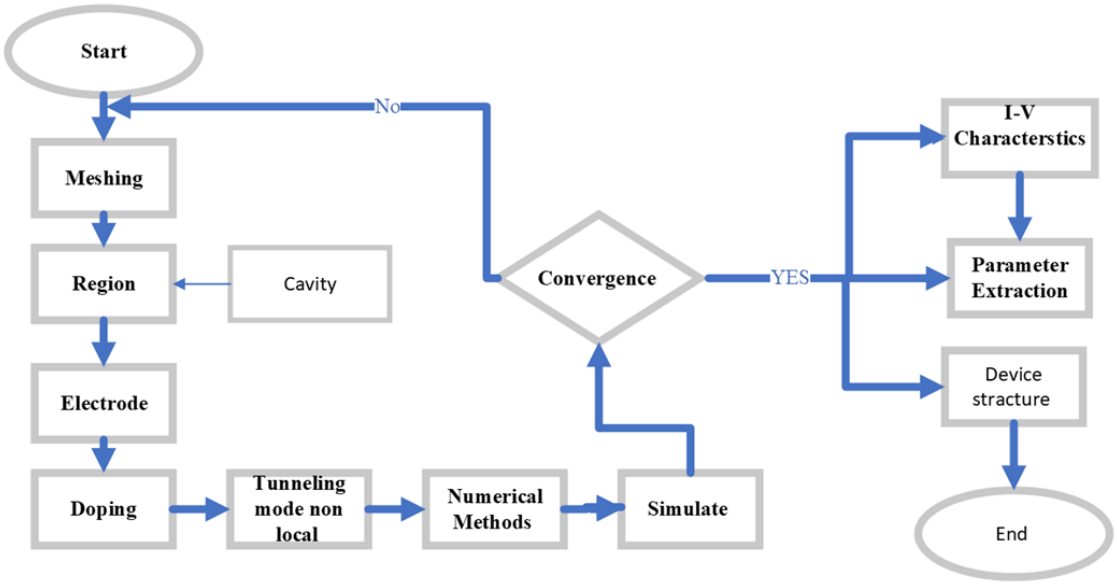


Figure 3.4: Atlas Resolution Algorithm for Biosensor application

3.6 JLTFET biosensor

The simulated device contains a cavity length of 47nm and 9nm thickness, which allows the structure to immobilize the biomolecules that are coming. The device is varied with respective of different neutral biomolecules sensitivity of permittivity values such as urease k=1.64, streptavidin k=2.1, biotin k=2.63, Ferrocytochrom k=4.7,bacteriophage k=6.3,keratin k=8 and gelatin=12 (Dharmender, Nigam, & Kumar, 2022) in order to analyses the performance of the proposed devices The structure of the device is shown in the figure 3.5

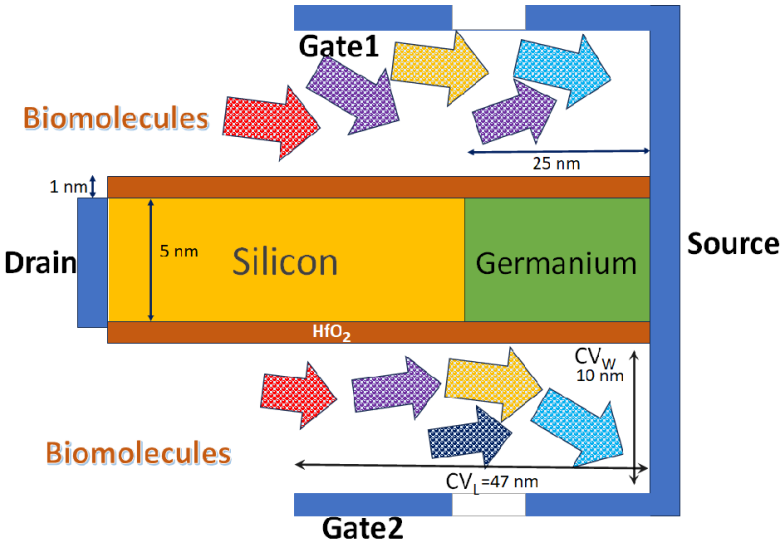


Figure 3.5: Device structure of GAA-HJLTF for biosensor

For the representation of the cavity, length, and thickness (width) the symbol used are CV_L and CV_W respectively, where CV_L = 47nm and CV_W=20nm it in both part of the source side. In addition, cavity is the confined space or region within the sensor where the biological or chemical biomolecules interaction takes place. In biosensor, the cavity is engineered to optimize sensitivity and selectivity.

In table3.5, a list of parameters used to design the biosensor device structure is listed. The parameter and the dimensions are the same as figure 3.3 b). In the biosensor, the cavity region is added in both side and it is open to create a larger space for the biomolecule to immobilize to the device. The length of the whole device became 29nm and the width of the whole device is same 74nm. For the biosensor, the doping concertation is also reduced which is 1e18 cm^{-3}.

Table 3.5: List of parameters used for biosensor

Parameter	Values
Channel length and thickness	20nm and 15nm
Gate work function	4.5eV
Source length and thickness	27nm and 5nm
Drain length and thickness	27nm and 5nm
Channel doping	1e18 cm^{-3}
Source doping	1e18 cm^{-3}
Drain doping	1e19 cm^{-3}
Source work function	5.93eV
Dielectric length and thickness	74nm and 2nm
Permittivity of the cavity	K=1.64, 2.63,4.7,63, 8 12
cavity Length and thickness	47nm and 10nm

CHAPTER FOUR

4. SIMULATION RESULTS AND ANALYSIS

4.1 Overview

The structural design result was evaluated using the Silvaco Atlas TCAD simulator. This chapter discusses the results based on the TCAD simulation. It has been studied and analyzed the simulate transfer characteristics (I_D-V_G), Electron BTB generation rate, Energy bad diagram, Electric field in the (horizontal direction), and electron concentration of GAA-H-JLNTFET. As application, biosensor is studied and simulated in the proposed structure and the device is studied and analyzed the parameters like sensitivity by varying the permittivity of natural biological molecules, and electrical characteristics (I_{ON}, I_{OFF}, I_{ON}/ I_{OFF} and SS,) of the devices

A) Performance description of GAA-H-JLTFET

In figure 4.1 it shows the drain current to gate voltage graph for both conventional and proposed GAA-HJLTFET structure with a work function for gate being 4.5eV and source work function 5.93eV and gate length of 20nm. The proposed structure in figure 4.1 shows a better ION and IOFF that is ~10^{-5} and ~ 10^{-18} with being it subthreshold being improved SS to 12mV/Dec.

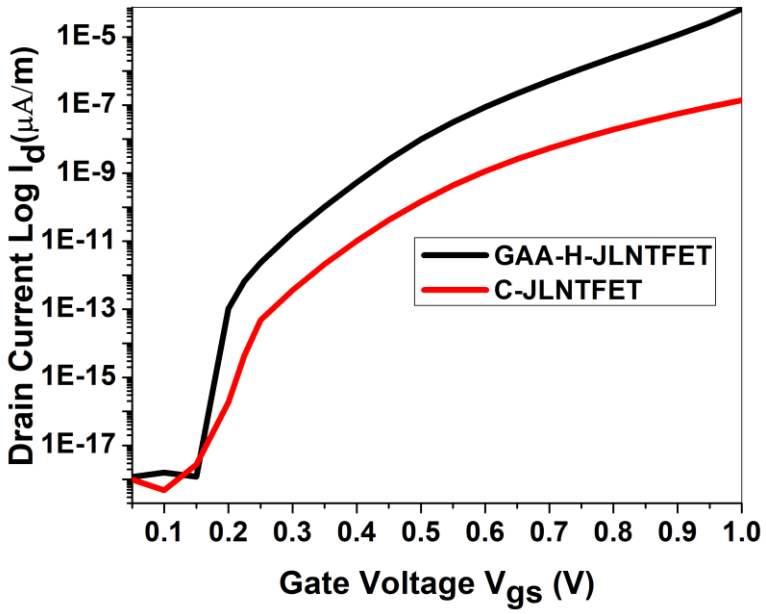


Figure 4.1 Transfer characteristic

The presence of Hetero-structure in GAA-JLNTFET has its own effect on the I_D-V_G cure. Germanium (Ge) has higher carrier mobility than silicon which mobility of charge Transport, the band gap of Ge is also smaller than that of silicon, which also enhances the Transfer characteristics of the device. The presence of high-k dielectric has its own role as it affects the EOT of the device, which has a direct relationship with Gate capacitance.

$$Cg = \frac{(COx * EOT * W)}{l} \tag{4.1}$$

Whereas cox is capacitance oxide, EOT effective oxide thickness, W=width, l=length

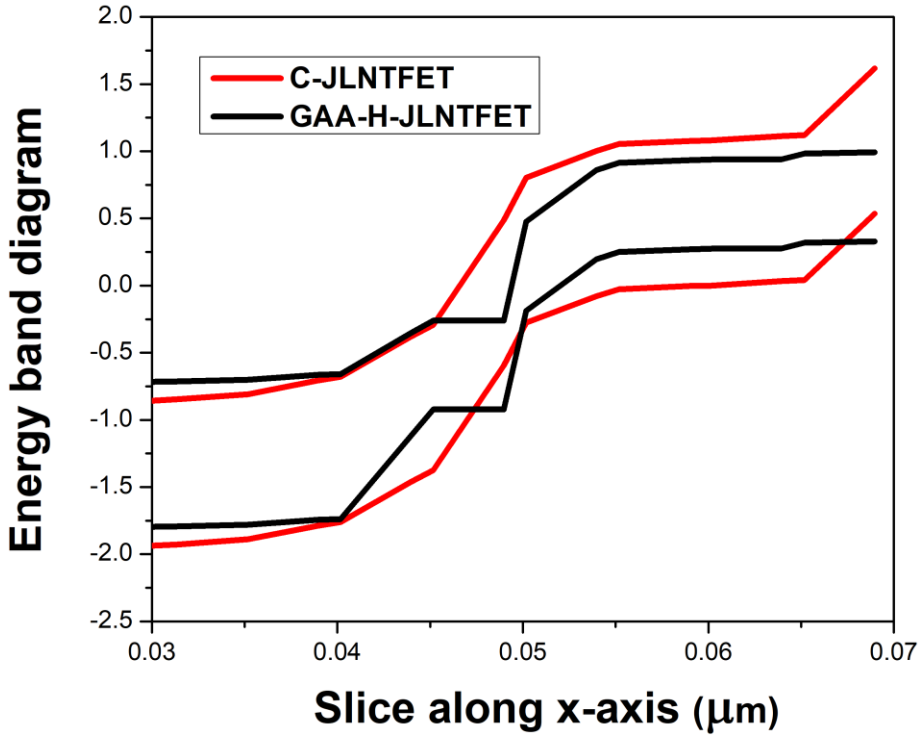


Figure 4.2 Energy band diagram

Figure 4.2 shows the energy band diagram in the on state and shows the proposed structure in black color is showing a narrow band gap in source channel interface which make the tunneling of carrier form valance band VB to conduction band easier CB. Therefore, the narrow band in the source and channel region facilitates the band-band tunneling, which improves the device performance.

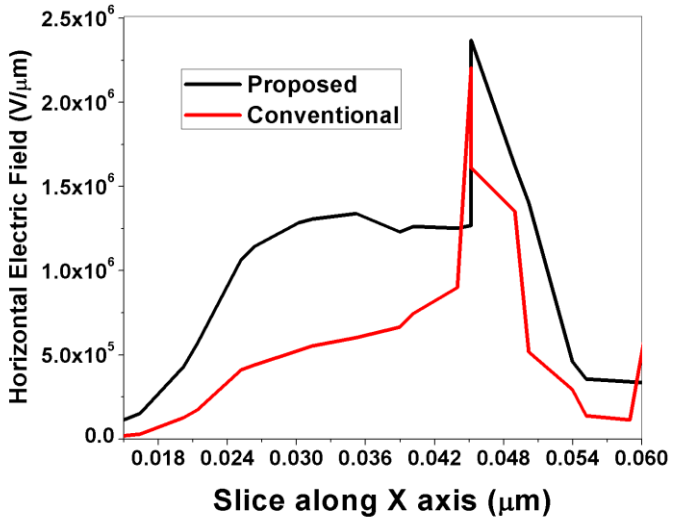


Figure 4.3 Electric field in X-direction

In figure 4.3, the effect of electric field in X-direction is shown the electric field of the proposed structure is showing high electric field. This is because electric filed affected by dielectric type (high-k or low-k). Compared to the traditional SiO_2. HfO_2 gives high electric field since using thinner high-k dielectric as gate oxide material can provide as equal value as a thicker value of low-k dielectric while maintaining the desire capacitance. The thicker dielectric oxide reduces the electric field strength accords the gate capacitance. In Hetero-structure Si and Ge band, gap modification is possible which also affects the electric filed strength in the device.

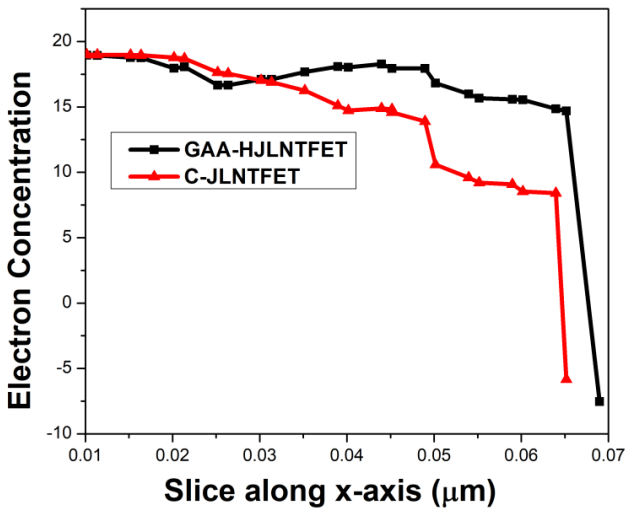
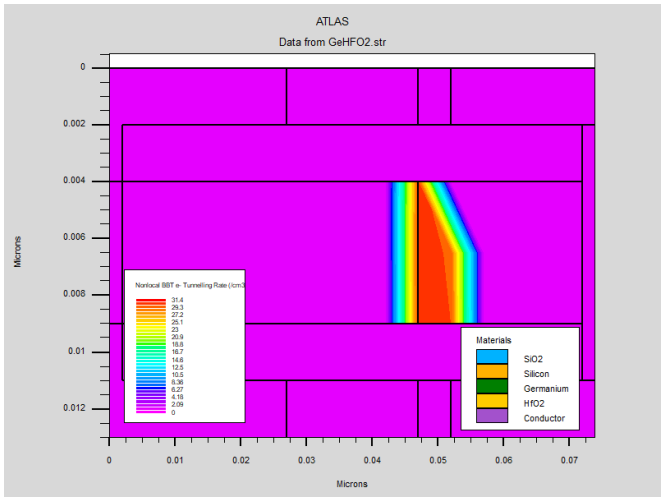
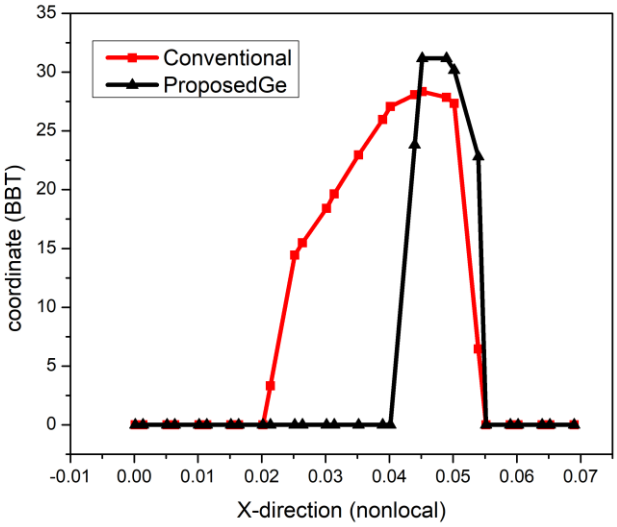


Figure 4.4 Electron concentration in X-direction

The point, which is a crucial factor, is electron concertation; it refers to the density of electron present in semiconductor material. It represents the number of electrons per unit volume in a specific direction. In figure 4.4 shows, electron concertation of in X-direction for both conventional and proposed GAA-HJLNTFET the proposed structure is having better electron concentration, which is important for achieving high-speed device, it enables the effective charge transfer and mobility of electron through material and allowing better conductivity and current flow.

a)





b)

Figure 4.5: BTBT in X-direction a) contour b) Transfer curve

Band-to band tunneling is an important parameter in TFET. It is a phenomenon in which carriers charge across the energy bandgap in semiconductor device over a significant distance, beyond the immediate vicinity of the tunneling region. The tunneling mechanism used in the simulation is a nonlocal band-to band model, which enhances current and reduces the leakage current in OFF state of the device by facilitating a controlled tunneling along the distance. In figure 4.5 the band-to-band tunneling in X-direction a) contour view and log file and shows the band- to band proposed and conventional JLTFET and the proposed is showing a narrow band-to-band tunneling which offers a promising for low power application. This property of having narrow band-to bandwidth also allows for efficient switching, lower leakage current, high I_{ON}/I_{OFF} ratio, and reduced short channel effect (SCE).

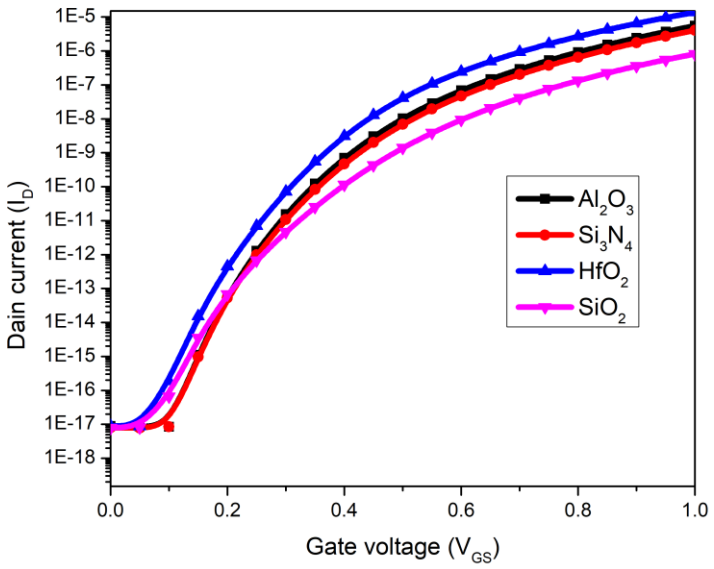


Figure 4.6 Transfer characteristic of different oxides

Figure 4.6 shows the effects of different types of oxide that have been investigated on the proposed structure and their effete on the I_D-V_G curve on the (drain current) for V_{GS}=1v and V_{DS}=1v.

- SiO_2 is one of the mostly used oxides in semiconductor devices it normally called low – k dielectric has high band gap energy of 1.1eV. typically exhibit good interface property
- HfO_2 is high-k dielectric, and have high dielectric constant compared to SiO_2 which allow grater charge carrier storage capacity and improve gate control.

- Al_2O_3 is also high–k with higher permittivity (Dielectric constant) have higher energy bad gap
- Si_3N_4 less commonly used oxide material and have a different property than the other oxide type

In the figure 4.6 Hfo2 shows a better result, in drain current than the other types of oxide this is because of the high- value dielectric constant or permittivity and reduce effective oxide thickness (EOT). This HfO2 increased capacitance per unit area compared to other oxide types and improved device performance.

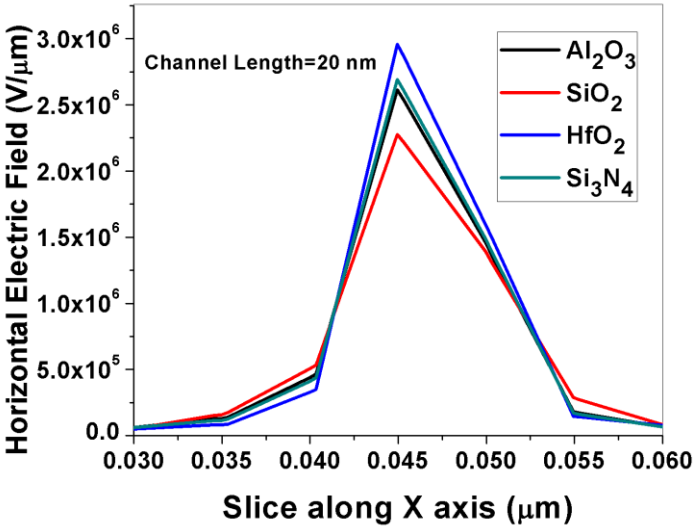


Figure 4.7 Electric field in X-direction for different oxide

Figure 4.7 shows the electric field effect on the X-direction of different oxide type and HfO_2 is showing higher electric field along x-direction.

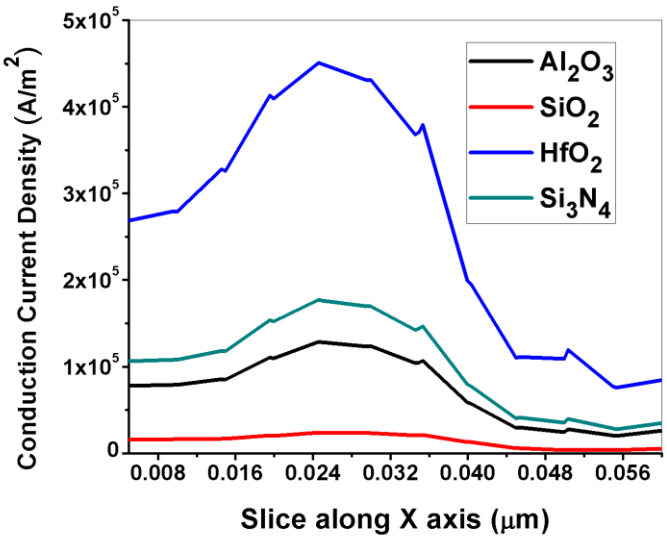


Figure 4.8 Conduction current in X-direction

In figure 4.8, the conduction current of several types of oxide is analyzed.

The conduction current in HfO_2 is shown high. This is because it has high Dielectric constant, which increases the storage per unit area resulting in higher capacitance and a higher capacitance lead to higher conduction current. A device with HfO_2 has a capability of scalability as the technology advanced with scaled-down dimensions. So as a device size is reduce achieving high conduction current is crucial to maintain the device performance.

Table 4.1: Comparison of structure

parameter	Conventional	GAA-JLNTFET	Proposed GAA-H-JLNTFE
SS	27.5 mV/Dec	19mV/Dec	10.2mV/Dec
I_{ON}	$1.39x10^{-7}$ A/μm	$3.37x10^{-6}$ A/μm	$6.66x10^{-5}$ A/μm
I_{OFF}	$9.92x10^{-19}$ A/μm	$2.97x10^{-20}$ A/μm	$1.27x10^{-18}$ A/μm
I_{ON}/I_{OFF}	$1.41x10^{+11}$	$3.35x10^{+13}$	$5.22x10^{+13}$

B) Application of GAA-H-JLNTFET as low power Biosensor

This section discusses the biosensor application implemented on the proposed GAA-H-JLNTFET after a cavity is inserted to mobilize the biomolecules. Generally, there are two types of bio sensing techniques which are used by most of the researcher i.e., one is gating technique and the other is dielectric modulated technique. In this work, we have utilized the dielectric modulated based techniques to implement the simulated biosensor using the junction less Tunneling device. The biomolecules that are used are neutral biomolecules (without any charge).

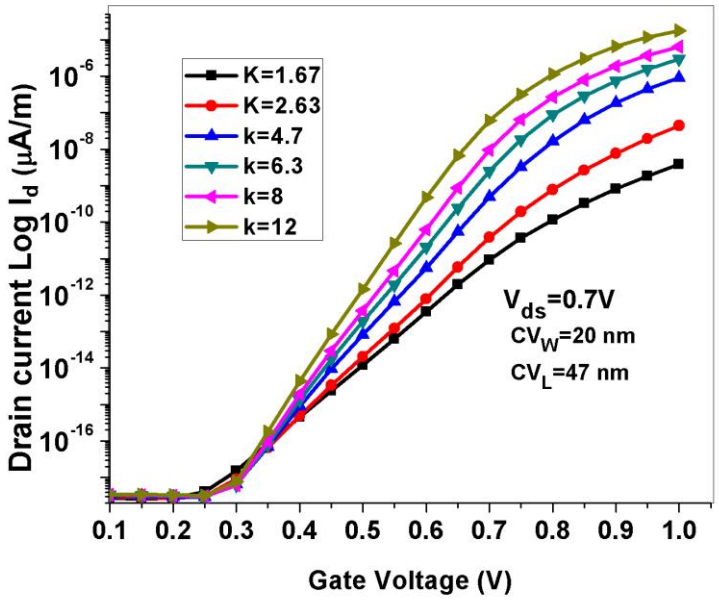


Figure 4.9: Variation of drain current with immobilization of different biomolecules

Figure 4.9 shows the drain current variation when the permittivity is varied from different types of biomolecules and as the permittivity of the cavity is increasing; the sensitivity of the device is increasing. In biosensor the permittivity of the cavity or the sensing region or active region affect the sensitivity of the device since permittivity determines the sensing of capacitance structure, which is typically

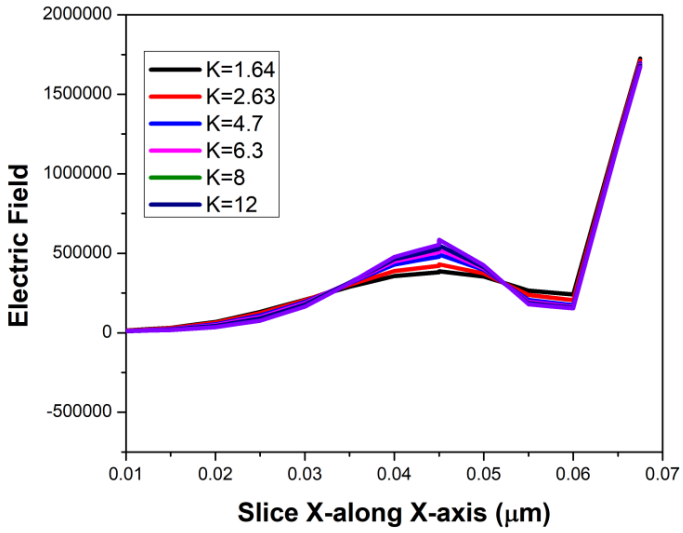


Figure 4.10: Electric field in X-direction

Influenced by the presence of biomolecules. The capacitance varies as the permittivity of the cavity is increasing due to interaction with the biomolecules. This variation of the capacitance noticed in the variation of drain current. In figure 4.9 at k=12 shows high ON current.

The effect of electric field and permittivity of the cavity are directly proportional when the permittivity is increasing the electric filed is also keep on increasing the relation can be given by

$$E \propto V/(\epsilon * d) \tag{4.2}$$

With the same voltage being applied due to the variation in permittivity, the electric fields are affected. This relation is help full that it increases the capacitance, the higher the field the higher capacitance will be in tea cavity region, which influences the charge storage capacity of the device and affect the overall electrical performance of the device. In figure 4.10, it illustrates those points.

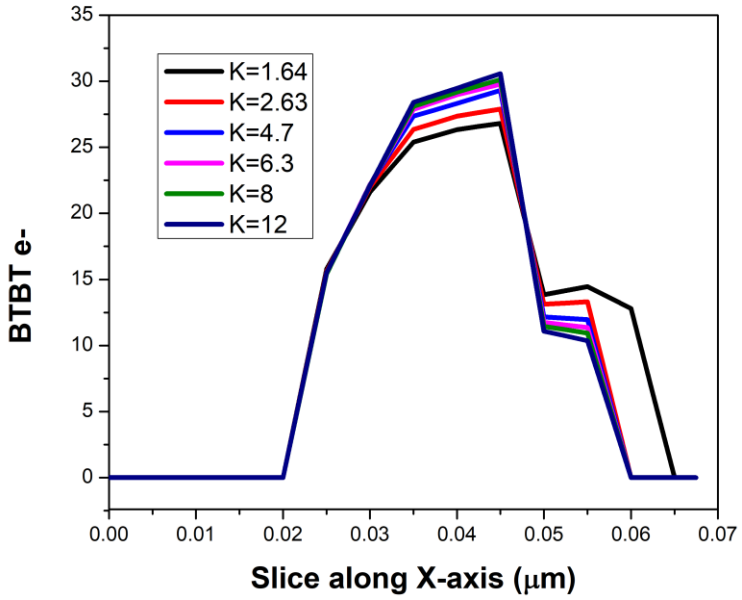


Figure 4.11: Electron tunneling in X-direction

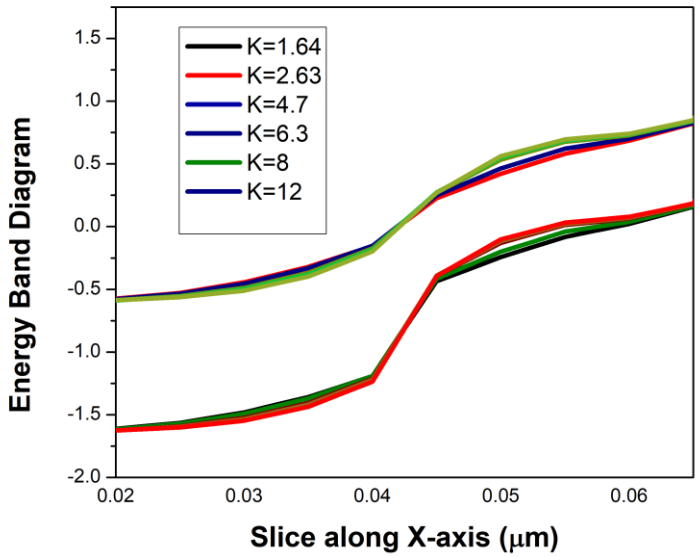


Figure 4.12: Energy Band Diagram

In the biosensor the energy band diagram is illustrates the distribution of energy level within that material stricture, including the CB and VB the variation of the permittivity of the biosensor impacts the energy band diagram and subsequently affect the device performance, in figure 4.12

it shows the energy band diagram for the natural biomolecules. When the permittivity is increasing, it alters the electric field distribution and potential profiles in the device. This in return affects the energy band diagram and modifies the shape as the conduction band (CB) Experian an upward shift and valance band (VB) downward shifts.

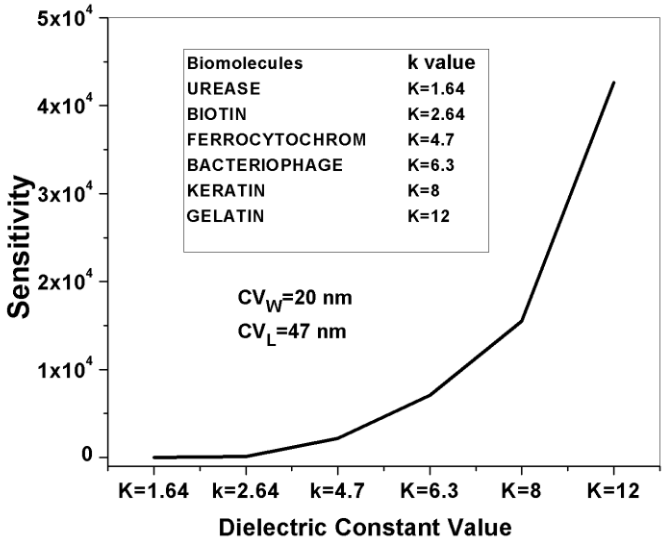


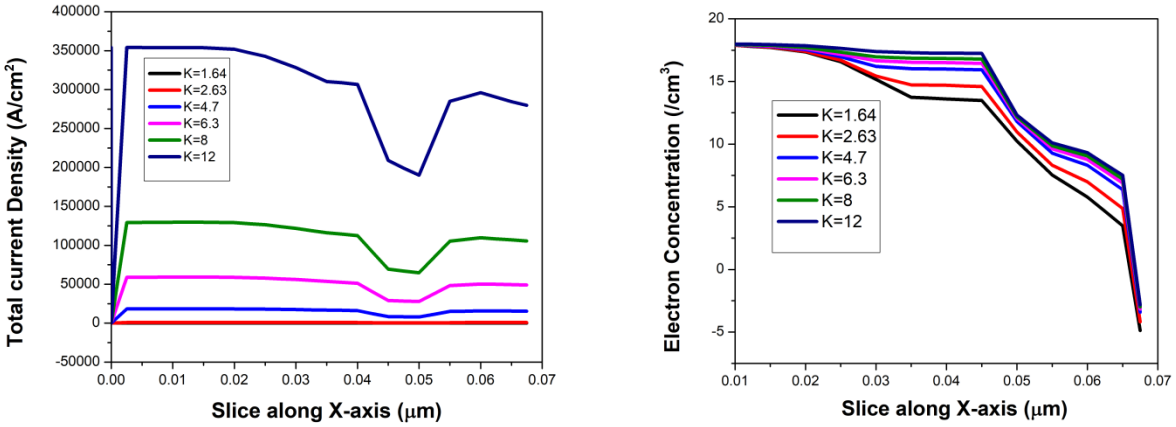
Figure 4.13: Sensitivity of Biomolecules

Biosensor sensitivity plays a crucial role in the accurate and precise detection of target molecules or analytes. As the permittivity of the cavity in a biosensor increased, it significantly affects the device's sensitivity. The permittivity, which represents the material's ability to store electrical energy, influences the electric field distribution within the cavity. The sensitivity of the biomolecules is calculated with the help of below expression:

$$S_I = \frac{I_D(bio) - I_D(air)}{I_D(air)} \tag{4.3}$$

In figure 4.13, the sensitivity of the neutral biomolecules increasing when the k value is increasing, the increment of k value also results in high electric field concentration in the cavity leading to enhance interactions between the sensing surface and target analyte. Furthermore, the surface-to-volume ratio of the cavity also plays a critical role in biosensor sensitivity. The increased surface area allows for mole binding sites and greater availability of active sites for analyte interactions. Consequently, it enhances the chance of successful analyte binding, leading to improved sensitivity of biosensor.

The combination of increased permittivity and higher surface to volume ratio in the cavity result in a synergistic effort on biosensor sensitivity. The presence of high electric field due to increased permittivity, along with the larger sensing area produced by the higher surface to volume ratio, enable enhanced analyte binding and more effective signal transduction.



a) b)

Figure 4.14: a) Total current density and b) Electron Concentration

In biosensor applications, the permittivity of neutral biomolecules plays a crucial role in determining the total current density and the electron concentration of a device. As the neutral biomolecules interact with the biosensor's sensing surface, they induce charges in the local electric field and charge distribution. The total current density in a biosensor relies on the movement of charge carriers, such as electron, in the sensing region or cavity. The permittivity of neutral biomolecules influences the electric field strength and potential near the surface. A higher permittivity result in strong electric field, which affect the movement of electrons and overall current flow figure 4.14 a) shows the direct relationship with permittivity. Similarly, the electron concentration in the biosensor is influenced by presence of neutral biomolecules with specific permittivity values. Figure 4.14 b) shows the effect these biomolecules impact the charge carrier density near the surface by influencing charge distribution and processes like carrier trapping and release. The permittivity also has an effect the capacitance of the sensing region, which is related to charge densities and movement. Changes in permittivity can modulate the capacitance, leading to variations in electron concentration and current density.

5. CONCLUSION AND RECOMMENDATION

5.1 Conclusion

In this thesis study, the Gate engineering and channel engineering on GAA-H-JLNTFET has been investigated. This work aims to determine and improve ON current (ION) reduce OFF Current (IOFF) and reduce the subthreshold slope (SS) and making it suitable for low power analog applications. The presence of Hetero-structure in the device improves mobility and the narrow band gap interface between the source and channel interfaces enhances the band-to band tunneling effect at channel-source interface. Here we used hafnium oxide as the gate oxide material. The high-k dielectric also enhances the capacitive Effect of the gate and reduces the effective oxide thickness (EOT). In this study, junction less FET and Tunnel FET both are combined together in a single structure which provided the competitive advantage of JLFET and TFET. The TCAD simulation has analyzed the performance parameter of ION, IOFF ION/IOFF and subthreshold slope compared to the conventional TFET. The simulated result has shown an improvement in Ion, IOFF and subthreshold slope(SS) compared to the similar published work that has been done and the ION/IOFF ratio remain the same for the voltage values VG=1 and VD=1. The effect of high-k dielectric (HfO2) in the structure has shown a better result in terms of performance by increasing the capacitive coupling between the gate and channel. In the proposed structure, the effect of electric filed BTBT and electron concentration and energy band diagram has been observed and noted.

As an application, the proposed structure (GAA-H-JLNTFET) had been implemented for the biosensing application. The performance of dielectric modulated biosensor is analyzed by investigating the sensitivity by varying the k value of various biomolecules. To check the insight performance of the FET based biosensor, the impact of different type of biomolecules on the electric fields, recombination rate and conduction current density is observed. It is concluded that the proposed device has better performance than the conventional device, particularly for the low power biosensing application. Simulated dielectric modulated biosensor possessing the better sensitivity for high-k value biomolecules.

5.2 Recommendation

This thesis studies the Gate and channel engineering of H-JLNTFET in gate all around for low power applications. The following tasks can be done for the future thesis work

- The analytical modelling of threshold voltage, subthreshold slope, ON current
- Detailed RF analysis for analog applications of the optimized proposed device GAA-H-JLNTFET
- Optimize the biosensor performance for the subthreshold regime and check the suitability for the charge biomolecules.
- Possible fabrication of the junction less Tunnel FET device structure

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6. REFERENCES

Abdi, D. B., & Kumar, M. J. (2015). PNPN tunnel FET with controllable drain side tunnel barrier width: Proposal and analysis. *Superlattices and Microstructures, 86*, 121-125.

Ansari, F., Chaudhary, T., Sunkaria, R. K., Singh, M., & Raj, B. (2022). Comparative Analysis of Nanowire Tunnel Field Effect Transistor for Low Power Application. *Silicon*. doi:10.1007/s12633-022-01967-2

Asthana, P. K., Ghosh, B., Rahi, S. B. M., & Goswami, Y. (2014). Optimal design for a high performance H-JLTFET using HfO 2 as a gate dielectric for ultra low power applications. *RSC advances, 4*(43), 22803-22807.

Baruah, R. K. (2015). *Modelling and simulation of short channel junctionless transistor from an analog design perspective.*

Bergveld, P., Hendrikse, J., & Olthuis, W. (1998). Theory and application of the material work function for chemical sensors based on the field effect principle. *Measurement science and technology, 9*(11), 1801.

Chaudhry, A., & Kumar, M. J. (2004). Controlling short-channel effects in deep-submicron SOI MOSFETs for improved reliability: a review. *IEEE Transactions on Device and Materials Reliability, 4*(1), 99-109.

Colinge, J.-P., Lee, C.-W., Afzalian, A., Akhavan, N. D., Yan, R., Ferain, I., . . . White, M. (2010). Nanowire transistors without junctions. *Nature nanotechnology, 5*(3), 225-229.

Colinge, J. P., Kranti, A., Yan, R., Lee, C. W., Ferain, I., Yu, R., . . . Razavi, P. (2011). Junctionless Nanowire Transistor (JNT): Properties and design guidelines. *Solid-State Electronics, 65-66*, 33-37. doi:https://doi.org/10.1016/j.sse.2011.06.004

Damrongplasit, N., Kim, S. H., & Liu, T.-J. K. (2013). Study of random dopant fluctuation induced variability in the raised-Ge-source TFET. *IEEE Electron Device Letters, 34*(2), 184-186.

Datta, E., Chattopadhyay, A., Mallik, A., & Omura, Y. (2020). Temperature dependence of analog performance, linearity, and harmonic distortion for a ge-source tunnel FET. *IEEE transactions on electron devices, 67*(3), 810-815.

Dharmender, Nigam, K., & Kumar, S. (2022). Performance assessment of cavity on source dual material split gate GaAs/InAs/Ge junctionless TFET for label-free detection of biomolecules. *Applied Physics A, 128*(10), 943.

Edgar, L. J. (1930). Method and apparatus for controlling electric currents: Google Patents.

Ghosh, B., & Akram, M. W. (2013). Junctionless Tunnel Field Effect Transistor. *IEEE Electron Device Letters, 34*(5), 584-586. doi:10.1109/LED.2013.2253752

Goswami, Y., Ghosh, B., & Asthana, P. K. (2014). Analog performance of Si junctionless tunnel field effect transistor and its improvisation using III–V semiconductor. *RSC advances, 4*(21), 10761-10765.

Ionescu, A. M., & Riel, H. (2011). Tunnel field-effect transistors as energy-efficient electronic switches. *nature, 479*(7373), 329-337.

Jossy, A. M., & Vigneswaran, T. (2014). A perspective review of tunnel field effect transistor with steeper switching behavior and low off current (IOFF) for ultra low power applications. *International Journal of Engineering and Technology (IJET), 6*(5), 2092-2104.

Kumar, K., Kumar, A., & Sharma, S. C. (2023). Electrical performance improvement of charge plasma-based junctionless TFET using novel coalescence of SiGe/GaAs and heterogeneous gate dielectric. *Applied Physics A, 129*(1), 23.

Kumar, P., & Raj, B. (2022). Parametric Investigation and Design of Junctionless Nanowire Tunnel Field Effect Transistor. *Silicon, 14*(11), 6031-6037.

Li, W., Liu, H., Wang, S., Chen, S., & Yang, Z. (2017). Design of high performance Si/SiGe heterojunction tunneling FETs with a T-shaped gate. *Nanoscale Research Letters, 12*, 1-8.

Medhi, S. (2014). *Atlas based simulation study of junctionless double gate (DG) tunnel FET*.

Narang, R., Reddy, K. S., Saxena, M., Gupta, R., & Gupta, M. (2012). A dielectric-modulated tunnel-FET-based biosensor for label-free detection: Analytical modeling study and sensitivity analysis. *IEEE transactions on electron devices, 59*(10), 2809-2817.

Nigam, K., Singh, S. V., & Kwatra, P. (2021). Investigation and design of stacked oxide polarity gate JLTFET in the presence of interface trap charges for analog/RF applications. *Silicon*, 1-18.

Nowbahari, A., Roy, A., & Marchetti, L. (2020). Junctionless Transistors: State-of-the-Art. *Electronics, 9*(7), 1174.

Ragavendran, U., & Ramachandran, M. (2018). Low Power and Low Area Junction-less Tunnel FET Design. *International Journal of Engineering & Technology, 7*(3.1), 155. doi:10.14419/ijet.v7i3.1.17076

Rahimian, M., & Fathipour, M. (2016). Asymmetric junctionless nanowire TFET with built-in $${n}^{+}$$source pocket emphasizing on energy band modification. *Journal of Computational Electronics, 15*(4), 1297-1307. doi:10.1007/s10825-016-0895-1

Rahimian, M., & Fathipour, M. (2017). Improvement of electrical performance in junctionless nanowire TFET using hetero-gate-dielectric. *Materials Science in Semiconductor Processing, 63*, 142-152.

Santa Clara, C. (2014). ATLAS device simulation software. *Santa Clara, CA, USA*.

Singh, B., Gola, D., Goel, E., Kumar, S., Singh, K., & Jit, S. (2016). Dielectric pocket double gate junctionless FET: a new MOS structure with improved subthreshold characteristics for low power VLSI applications. *Journal of Computational Electronics, 15*(2), 502-507.

Singh, D., Pandey, S., Nigam, K., Sharma, D., Yadav, D. S., & Kondekar, P. (2016). A charge-plasma-based dielectric-modulated junctionless TFET for biosensor label-free detection. *IEEE transactions on electron devices, 64*(1), 271-278.

Troutman, R. R. (1979). VLSI limitations from drain-induced barrier lowering. *IEEE Journal of Solid-State Circuits, 14*(2), 383-391.

Turkane, S. M., & Kureshi, A. (2016). Review of tunnel field effect transistor (TFET). *International Journal of Applied Engineering Research, 11*(7), 4922-4929.

Verma, M., Sharma, D., Pandey, S., Nigam, K., & Kondekar, P. (2017). Performance comparison of single and dual metal dielectrically modulated TFETs for the application of label free biosensor. *Superlattices and Microstructures, 101*, 219-227.