Investigation and Mitigation of Harmonics and Voltage Dip as A Power Quality Problems in Distribution Networks (Case Study: Adama Spinning Factory)

Chala Baru Mengistu

A Thesis Submitted to

The Department of Electrical Power and Control Engineering

School of Electrical Engineering and Computing

Presented in Partial Fulfillment of the Requirement for the Degree of Master's in Electrical Power and Control Engineering (Power Engineering)

Office of Graduate Studies

Adama Science and Technology University

June, 2022

Adama, Ethiopia

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DECLARATION OF STUDENT

I hereby declare that this Master Thesis entitled "**Investigation and Mitigation of Harmonics and Voltage Dip as A Power Quality Problems in Distribution Networks (Case Study: Adama Spinning Factory)**" is my original work. That is, it has not been submitted for the award of any academic degree, diploma, or certificate in any other university. All sources of materials that are used for this thesis have been duly acknowledged through citation.

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Name of the Student	Signature	Date

RECOMMENDATION OF ADVISOR

I, the advisor of this thesis, hereby certify that I have read the revised version of the thesis entitled "**Investigation and Mitigation of Harmonics and Voltage Dip as A Power Quality Problems in Distribution Networks (Case Study: Adama Spinning Factory)**" prepared under my guidance by **Chala Baru Mengistu** submitted in partial fulfillment of the requirements for the degree of Mater's of Science in Electrical Power and Control Engineering (Power Engineering). Therefore, I recommend the submission of a revised version of the thesis to the department following the applicable procedures.

Dr. C S Reddy _____ _____ _____

Advisor Signature Date

APPROVAL PAGE

I, the advisor of the thesis entitled "**Investigation and Mitigation of Harmonics and Voltage Dip as A Power Quality Problems in Distribution Networks (Case Study: Adama Spinning Factory)**" and developed by **Chala Baru Mengistu**, hereby certify that the recommendation and suggestions made by the board of examiners are appropriately incorporated into the final version of the thesis.

Dr. C S Reddy	_____	_____
Advisor	Signature	Date

We, the undersigned, members of the Board of Examiners of the thesis by **Chala Baru Mengistu** have read and evaluated the thesis entitled "**Investigation and Mitigation of Harmonics and Voltage Dip as A Power Quality Problems in Distribution Networks (Case Study: Adama Spinning Factory)**" and examined the candidate during the open defense. This is, therefore, to certify that the thesis is accepted for partial fulfillment of the requirement of the degree of Master of Science in Electrical Power and Control Engineering (Power Engineering).

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ACKNOWLEDGEMENT

First and foremost, I would like to use this opportunity to praise God Almighty. Following that, I'd want to express my gratitude to Dr. C S Reddy, my advisor, for his kindness, motivation, and support throughout my research. Mr. Getahun Shimeles, the Adama spinning factory's electrical engineering manager, and other industry electricians deserve my gratitude. They were quite helpful in assisting me with data collection for my research. In addition, I'd want to thank my beloved friends for their thoughtful words and ongoing support.

Finally, I would like to thank Adama Science and Technology University for providing me with this invaluable opportunity to finish my master's degree.

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LIST OF ACRONYMS AND ABBREVIATIONS

AC	Alternating Current
ANSI	American National Standards Institutes
ASD	Adjustable Speed Drive
ASF	Adama Spinning Factory
CCM	Current Controlled Mode
CMDB	Central Main Distribution Board
CPD	Custom Power Device
CPU	Central Processing Unit
CSD	Current Synchronous Detection
CT	Current Transformer
DC	Direct Current
DSTATCOM	Distribution Static Synchronous Compensator
DVR	Dynamic Voltage Restorer
HV	High Voltage
HVDC	High Voltage Direct Current
IEC	Electro-Technical Commission
IEEE	Institute of Electrical and Electronics Engineers
KVA	Kilo Volt Ampere
LPF	Low Pass Filter
NEMA	National Electrical Manufacturer Association
PBT	Power Balance Theory
PCC	Point of Common Coupling
PFC	Power Factor Controller

PLC	Programmable Logic Circuit
PLL	Phase Locked Loop
PQ	Power Quality
PR	Proportional Resonant
PWM	Pulse Width Modulation
RMS	Root Mean Square
SMES	Superconducting Magnetic Energy Storage
SRF	Synchronous Reference Frame
SVM	Space Vector Modulation
TCR	Thyristor Controlled Reactor
TDD	Total Demand Distortion
THD	Total Harmonic Distortion
TSC	Thyristor Switched Capacitor
UPQC	Unified Power Quality Conditioner
VSC	Voltage Source Converter

ABSTRACT

In this study, harmonic distortion and voltage sag were investigated and proper mitigation techniques for the Adama spinning factory were provided. The DELAB NV8s PFC equipment is used to measure the voltage and current harmonic distortion levels on the four distribution boards. Although this equipment is primarily designed for automatic power factor regulation with 3-phase capacitor banks, it can also measure total and individual harmonic distortions for voltage and current up to 11^{th} order. The measured voltage and current harmonic distortion levels were compared with IEEE power quality standards, and current harmonic distortion was found on the CMDB-1 and CMDB-3 distribution boards. The investigation also revealed that all of the CMDBs have voltage harmonic distortion that is considerably below the IEEE standard limit. Voltage sag was detected as another power quality concern during the CMDB-2 and CMDB-4 measurements. A DSTATCOM with synchronous reference frame theory has been suggested and modeled on MATLAB/SIMULINK to tackle the current harmonics occurring in the specified distribution boards. The simulation results without this compensating device demonstrate that the THD_I of source current is 17.37% for CMDB-1 and 16.56% for CMDB-3. The THD_I of source current for CMDB-1 and CMDB-3 was then reduced to 3.64% and 2.73%, respectively after the mitigation device has been connected. With the DSTATCOM connected to CMDB-1 and CMDB-3, the THD_I of source current has been reduced by 79.04% and 83.51%, respectively. Another custom power device proposed and designed to eliminate voltage sag in the CMDB-2 and CMDB-4 of distribution networks is the Dynamic Voltage Restorer (DVR). The DVR has compensated for voltage sag caused by various symmetrical and unsymmetrical faults, as shown by simulation results. The simulation results, with and without the mitigating devices illustrate that the current harmonics and voltage sag have been compensated with the devices integrated to the network and these power quality issues have been reduced to below the IEEE standard limit.

Key Words: *DSTATCOM, DVR, Harmonics, MATLAB/SIMULINK, Power quality Standards, Synchronous Reference Frame, Voltage Sag.*

CHAPTER ONE

INTRODUCTION

1.1 Background of the Study

In recent years many researches have been done concerning power quality problems in distribution networks. These problems are very common in manufacturing industries since there are a lot of sophisticated devices that leads to them. Hence, the power quality is becoming increasingly crucial to utilities and electricity customers at all levels, particularly industrial customers. Because of the rising concern for power quality, several consumer groups have had their power quality changes and characteristic disturbances measured. Power quality problems are commonly caused by load switching, system faults, motor starting, load variations, nonlinear loads, intermittent loads, and arc furnaces (Gautam et al., 2017). Power quality problems include harmonics, transients, short-duration voltage changes, long-duration voltage variations, voltage unbalance, voltage fluctuations, and power frequency variations. Voltage sag and harmonics are the most common and dangerous power quality issues in the industry and throughout entire distribution systems. Voltage sag is the most common power quality event, causing repeated mal-operation of sensitive electrical loads such as motors and Adjustable Speed Drives (ASD) (Khergade et al., 2018). In an ideal system, the load should get a balanced and pure sinusoidal three-phase voltage with constant amplitude, as well as a perfect sinusoidal current from the mains with unity power factor, balanced phases, and zero harmonic distortion. However, because of the non-linear nature of the load, harmonics in the supply system traveled to other parts of the distribution system via a point of common coupling before returning to the mains. The harmonic current can cause voltage harmonics and a variety of other power quality issues, all of which are harmful to the equipment and loads connected to the power distribution system. A severe power quality problem may lead to the shutdown of processes and services, causing economic losses to utility consumers (Asha Kiranmai & Jaya Laxmi, 2018).

The manufacturing industry in our country has been substantially expanding in recent years. However, different power quality problems are still happening on a regular basis. As a result of these issues, industries are unable to operate correctly and consistently. When power quality is a concern, the utility must produce sine wave voltage, while end-use customers must control the

harmonic currents their electric loads introduce into the utility system. As a result, the utility must provide a specified minimum quality of electric power to its consumers, while end users must restrict the power quality disruptions they introduce into the system. The majority of electric power quality issues occur in industries.

In this study, the power quality issues, particularly harmonics and voltage sag, are investigated and their proper mitigation technique for the case of Adama spinning factory has been presented. These power quality issues have a major negative influence on the industry's distribution system and equipment.

1.2 Statement of the Problem

The Adama spinning factory is facing numerous challenges as a result of power quality problems occurring from the load side as well as from the utility side. The harmonics and voltage sag investigation performed at this factory, demonstrates that due to these power quality problems the manufacturing process are disturbed many times throughout the year. Many adjustable speed drives (ASD) are utilized in this industry to control motor speed, and their extensive use generates current harmonic distortions in the system, which distorts the given voltage. In the Central Main Distribution Boards CMDB-1 and CMDB-3 there are a large number of ASDs than the other boards. As a result, the Total Harmonic Distortion (THD) under these boards is above the IEEE recommended limit. Another power quality issue that occurs regularly in the factory is voltage sag, which is caused by short circuits, the starting of large motors, and other faults in the distribution network. Also, the voltage provided from the utility side can occasionally fall below the allowable limit, causing the breaker to trip or the motors and other devices to be damaged. The voltage sag problem was occurred in CMDB-2 and CMDB-4 because of faults and short circuits. In the factory, compressor motor, Air Conditioner fan motors and water pump motors are damaged many times due to voltage sag that is caused by the short circuits occurred in the system. Generally, due to these power quality disturbances, the factory is experiencing a number of issues, including the failure of expensive electronic PCB and ASD, repeated burnouts of electric motors and fluorescent lamps, software corruption, and a series of fire accidents in the capacitor banks.

Therefore, voltage sag and harmonics analysis must be performed at the factory to precisely detect and identify which distribution boards are facing these problems, as well as to select and deploy an appropriate solution to mitigate problems exceeding the IEEE standard limit.

1.3 Objectives

1.3.1 General Objective

The general objective of this study is to analyze power quality problems with the Adama spinning factory power distribution network, such as harmonics and voltage sag, and to propose appropriate mitigation techniques using custom power devices.

1.3.2 Specific Objectives

The specific objectives of this study are listed below:

- To measure individual harmonic and total harmonic distortions using a DELAB NV 8s PFC, analyze the voltage sag by recording relevant data and comparing the disturbance levels to IEEE standards.
- To propose a mitigation technique for the harmonics and voltage sag that exceed the disturbance level limit.
- To design and simulate the proposed mitigation technique on MATLAB/SIMULINK and compare the performance of the system with and without a mitigating device.
- To analyze the cost-effectiveness of the proposed custom power devices.
- To conclude, and make further recommendations based on the results of the investigation.

1.4 Scope of the Study

This thesis discusses power quality issues like harmonics and voltage sag, two of the most prominent power quality issues in current distribution systems, as well as mitigation approaches for the Adama spinning factory distribution network. Data has been collected by measuring harmonics with a DELAB NV8s PFC, by interviewing the electrical technician and by reviewing different electrical documents of the factory. The data collected are then analyzed by comparing the level of existing power quality with the IEEE standard limit. Finally, the operation of distribution network has been analyzed before and after integration of mitigating devices.

1.5 Significance of the Study

The goal of this study is to help Adama Spinning Factory reduce the costs associated with power quality issues in its manufacturing process. The findings of this study are most useful to the factory in terms of becoming aware of the quality of the electric power used by its production machinery

and equipment; and, more importantly, the factory can reduce production loss by limiting the effects of power quality problems by implementing the study's proposed solution.

1.6 Organization of the Thesis

In this study, power quality problems in Adama Spinning Factory, particularly harmonics and voltage dip, have been investigated and their proper mitigation technique is proposed. The thesis is organized into five chapters. The study's background, a statement of the problem, objectives, and significance are all included in the first chapter.

The second chapter examines various power quality issues, including their causes and impacts on the distribution system and electrical equipment. In addition, this chapter discusses a number of related papers on power quality issues. There are also discussions on various international power quality standards.

The third chapter discusses data collection methods, electrical distribution network parameters and modeling, and data analysis. This chapter also describes the design of mitigating devices with their respective controlling methods.

In chapter four, the MATLAB/SIMULINK model has been simulated with and without the proposed mitigating device to identify the level of the existing power quality problem. The distribution network's performance before and after the integration of these devices was then discussed.

Chapter 5 outlines the conclusion developed based on the investigation results, as well as the recommendations provided to the industry and the electric utility; and the further future work to be done.

CHAPTER TWO

LITERATURE REVIEW

2.1 Theoretical Background

Power quality has recently been a major concern for companies, businesses, and residential buildings. It has a huge impact on all current energy-related contexts. Harmonics, interruptions, sags, swells, and transients are examples of power quality issues. Various researchers have already recognized voltage sags as one of the most serious power quality challenges. Industrial activities are regularly disrupted, and electronic equipment malfunctions as a result of these events. Apart from voltage sags, the increasing number of nonlinear loads, such as adjustable speed drives (ASDs), fluorescent lamps, and other power electronic devices, causes harmonics in industrial distribution networks (Liao & Milanović, 2017). High harmonic distortion can have a severe impact on a facility's electric distribution system and cause motors and other equipment to overheat, resulting in premature failure. Harmonics produced by nonlinear loads can also have an impact on devices on control boards and other sensitive analog circuits (Sivakumar et al., 2019).

2.2 Power Quality (PQ) Problems

Power quality problems are defined as any voltage, current, or frequency variations causing customer equipment failure or malfunctioning. Power quality issues have persisted, and they have become a serious concern in recent decades. Equipment failure, higher electricity costs, wasted energy, communications system interference, and even the shutdown of entire operations can all be caused by power quality issues (Gao & Awodele, 2015).To solve power quality issues, the problem must first be identified. Some of the most common power quality issues are listed below:

2.2.1 Voltage Variation within a Short-Duration

I) A voltage sag (dip): occurs when the root-mean-square (rms) voltage at the power frequency decreases across time intervals ranging from a half cycle to a minute. Voltage drops from fault currents or the start of large motors are the main causes. Process controls may shut down or computer systems may crash as a result of sags. Due to the sensitivity of modern electronic equipment, voltage dips have resulted in a substantial number of industrial and consumer

shutdowns. Even with advancements in electronic device susceptibility, industrial equipment may still be vulnerable to a variety of voltage dips of varying magnitudes and durations.

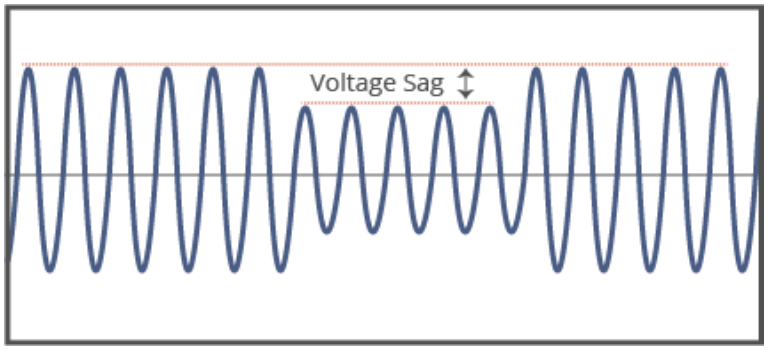


Figure 2.1: Schematic diagram of Voltage sag

II) Voltage Swell: a voltage spike ranging from 1.1 to 1.8 p.u. that lasts longer than half a mains cycle but less than one minute. System faults, energizing a big capacitor bank, turning off a huge load, and poor VAR compensation are all factors that contribute to this. Swells, like voltage sags, are often associated with system faults, such as a temporary voltage spike on the unfaulty phases during a Single Line to Ground (SLG) fault, but they are not as common. Voltage regulators, motor generator sets, uninterruptible power supply (UPS), and automatic transfer switches can all be used to solve voltage swell concerns (Pal & Gupta, 2020).

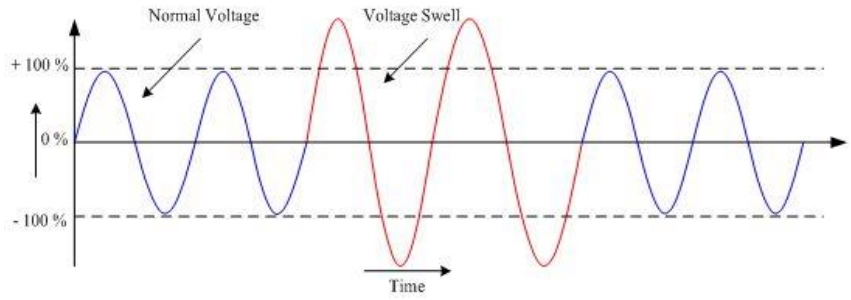


Figure 2.2: Schematic diagram of Voltage Swell

III) An interruption: is a power quality issue that occurs when voltage drops below 0.1 pu for less than one minute. It largely affects the manufacturing sector, particularly the continuous process industry. The main causes of these events are faults, control failures, and equipment failures. IEEE 1159 divides interruptions into two categories: short-duration and long-duration.

However, the term "interruption" is frequently used to refer to a short-duration disruption, whereas "sustained" is used to describe a long-duration interruption.

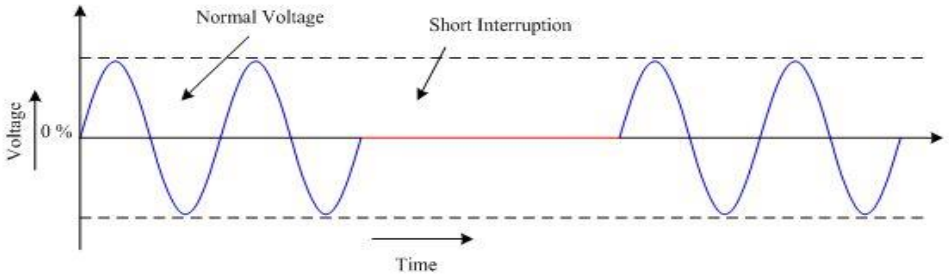


Figure 2.3: Schematic diagram of Interruption

2.2.2 Voltage Variations within a Long-Duration

Long-duration variations are defined as root-mean-square (rms) deviations at power frequencies for more than one minute. It can be classified as overvoltage, undervoltage, or sustained interruptions.

i) An undervoltage: At the power frequency, the rms AC voltage falls below 90% for longer than one-minute intervals. When a load is turned on or a capacitor bank is turned off, an undervoltage can occur until the system's voltage control device restores the voltage to within tolerance limits. Overloaded circuits might also experience undervoltage (Ferdi, 2015).

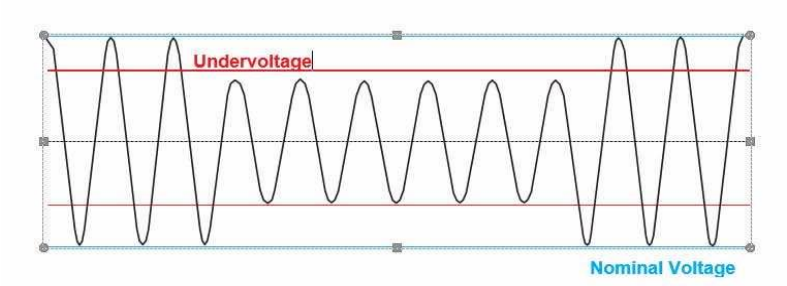


Figure 2.4: Schematic diagram for under-voltage

ii) An over-voltage is defined as an increase in rms AC voltage of more than 110 percent lasting more than one minute at a power frequency. It occurs when a heavy load is turned off or a capacitor bank is energized. Overvoltage occurs when the system is either too weak to accomplish effective voltage regulation or when the voltage controls are insufficient. Overvoltage can also be caused by incorrect tap settings on transformers.

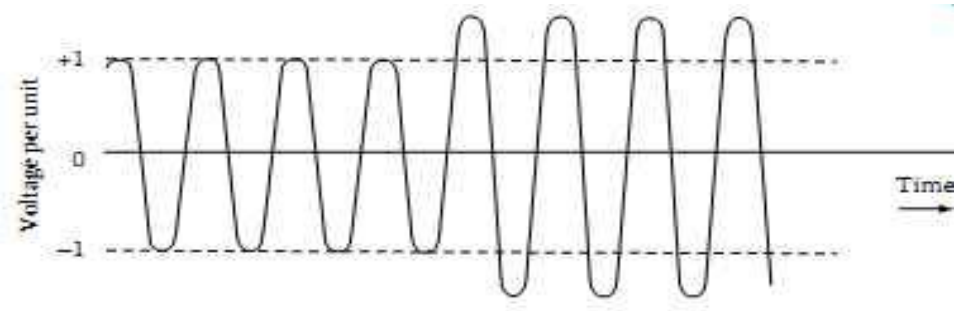


Figure 2.5: Schematic diagram of Over-voltage

iii) A sustained interruption is defined as a long-duration voltage variation that lasts more than one minute.

2.2.3 Transients

A transient refers to an undesirable but short-lived event that occurs during switching from one steady-state operating condition to another. They are divided into two categories: impulsive and oscillatory. An impulsive transient (positive or negative) is a non-power frequency shift in the steady-state situation of unidirectional polarity voltage or current. The most common source of impulsive transients is lightning.

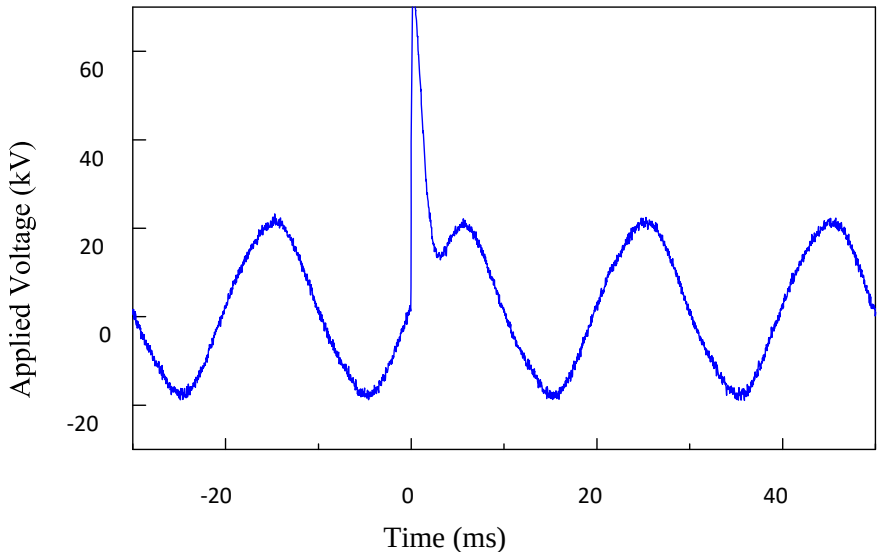


Figure 2.6: Schematic diagram of impulsive transient

An oscillatory transient is defined as a non-power frequency shift in the steady-state condition of voltage, current, or both that has both positive and negative polarity values. A voltage or current whose polarity varies rapidly at its immediate value is also referred to as a polarized voltage or current. It is defined by ns in the measured quantity at very high frequencies and is specified by its spectrum content, duration, and magnitude (Brown, 2012).

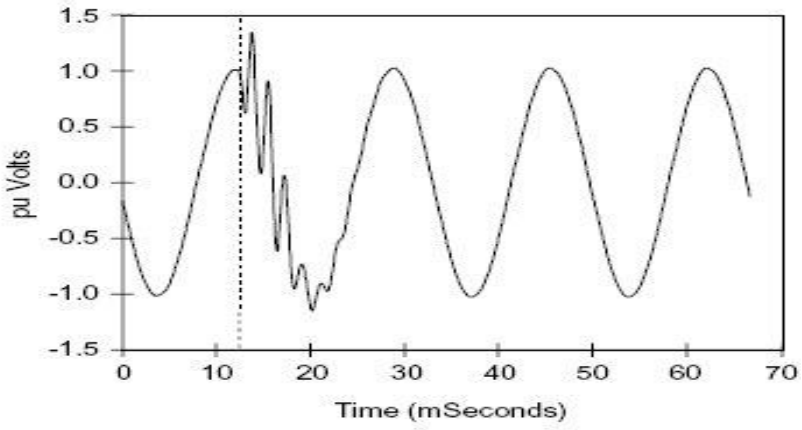


Figure 2.7: Schematic diagram of oscillatory transient

Transients lead to equipment failure, nuisance tripping of adjustable-speed drives, system lock-up, data corruption, and data loss.

2.2.4 Voltage Fluctuation (Flicker)

Voltage fluctuations are a sequence of random voltage shifts with magnitudes ranging from 0.9 to 1.1 p.u. Flicker describes voltage variations caused by loads that exhibit continuous, fast changes in load current magnitude. The term "flicker" comes from the way voltage changes affect lamps, causing them to flicker to the human eye. The most common sources of voltage fluctuations in utility transmission and distribution networks are arc furnaces and welders (Habte, 2018).

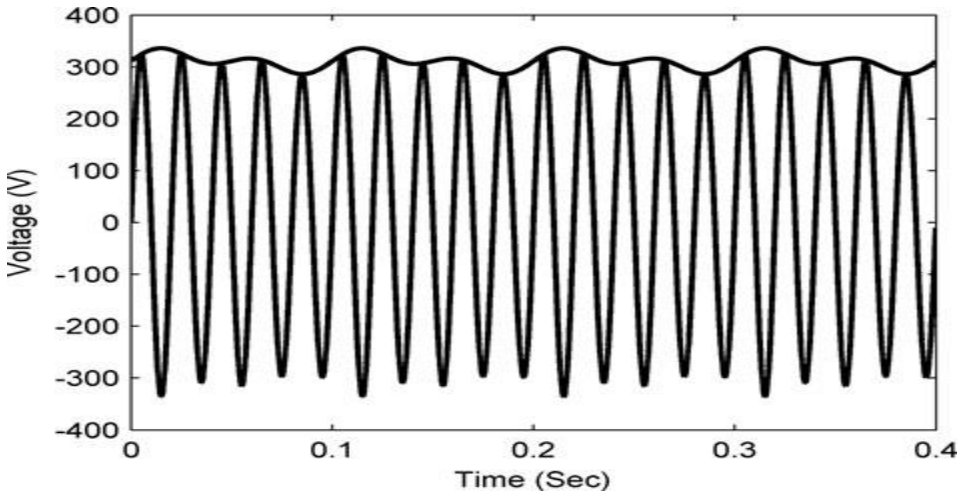


Figure 2.8: Voltage flicker schematic diagram

2.2.5 Voltage Unbalance

A voltage imbalance is defined as the largest variation from the three-phase voltage average. It can be expressed in percent when divided by the average of the three-phase voltages.

$$\%\ \text{Voltage Unbalance} = \frac{\text{Maximum Voltage deviation}}{\text{Average Voltage}} * 100 \qquad (2.1)$$

Unbalanced voltages can cause serious problems in a wide range of electrical devices, especially electric motors. On the motor shafts, the presence of negative and zero-sequence components on the supply voltages causes pulsing torques and speed changes. Imbalances can also disrupt industries and companies (Duarte et al., 2020).

2.2.6 Waveform Distortion

A steady-state variation from an ideal sine wave of power frequency described by the deviation spectral content is known as waveform distortion. The five basic types of waveform distortion are harmonics, inter-harmonics, DC offset, notching, and noise.

2.2.6.1 Harmonics

Harmonics are sine-wave voltages or currents that are integer multiples of the supply system's intended frequency of operation (called the fundamental frequency; usually 50 or 60 Hz). As demonstrated in figure 2.9, the voltage harmonic distortion representation can be used to

decompose regularly deformed waveforms into a sum of the fundamental frequency and harmonics. The equation for such a waveform is as follows.

$$V(t) = a_0 + \sum_{1}^{\infty} V_h * \sin(h * 2\pi f * t + \theta_h) \qquad (2.2)$$

Where θ_h is Phase angle, V_h is peak voltage level, f is fundamental frequency and a_0 is a DC component.

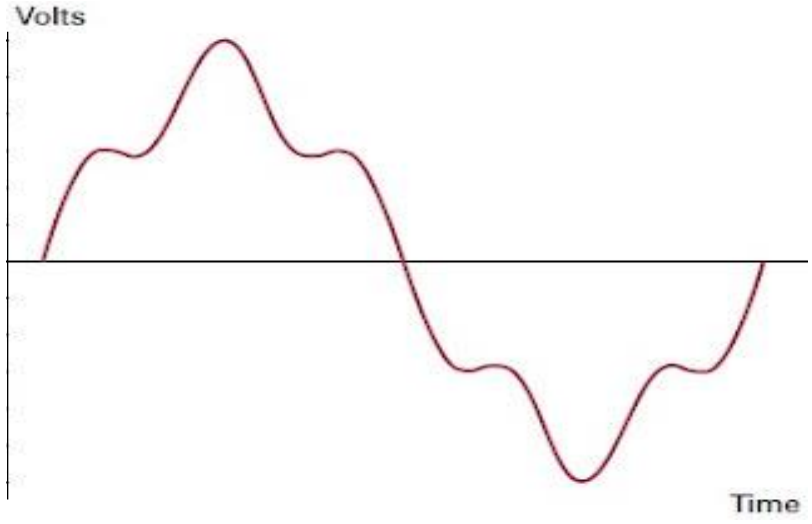


Figure 2.9: A Voltage Harmonic Distortion Waveform

Harmonics are generated by nonlinear loads, causing distortion in voltage and current waveforms. In industry, high-value harmonics with a high chance of having disturbing effects are found, but in the utility network, low-value harmonics with a low probability of causing disturbing effects are found (Kalair et al., 2017). Because of the increased use of power electronics equipment, harmonic distortion is becoming a major concern for many customers and utilities. Total harmonic distortion (THD) is the most widely used measure of harmonic content. It is calculated by the following formula:

$$THD_V = \frac{\sqrt{\sum_{h=2}^{\infty} V^2{}_h}}{V_1} \qquad (2.3)$$

$$THD_I = \frac{\sqrt{\sum_{h=2}^{\infty} I^2{}_h}}{I_1} \qquad (2.4)$$

Where V_1 and I_1 represent the fundamental RMS voltage and current, respectively and V_h and I_h represent the RMS voltage and current values at harmonic orders of h, respectively.

Total Harmonic Distortion is a useful measure of waveform distortion, but it can be deceiving because small currents can have extremely high levels of THD without causing substantial voltage distortions, therefore it's not a power quality issue. Since it is computed in terms of maximum demand load current rather than the fundamental of the current sample, the Total Demand Distortion (TDD) factor can better identify current distortion levels. This is because a small current can have a high THD but not be a significant threat to the system (Kelly, 2020).

$$TDD = \frac{\sqrt{\sum_{h=2}^{\infty} I^2{}_h}}{I_L} \tag{2.5}$$

Where I_L represent at the fundamental frequency component, the maximum demand load current.

2.2.6.2 Notching

The regular operation of power electronics devices causes notching, which is a periodic voltage disturbance. Commutation from one phase to another is the main cause of it. During commutation, a transient short circuit occurs between two phases. The notch depth is the average depth of line voltage from a sinusoidal wave of voltage, with the width of the notch depth determined by the commutation angle. There are consequences to notching, such as frequency and timing errors (Leite & Decker, 2020).

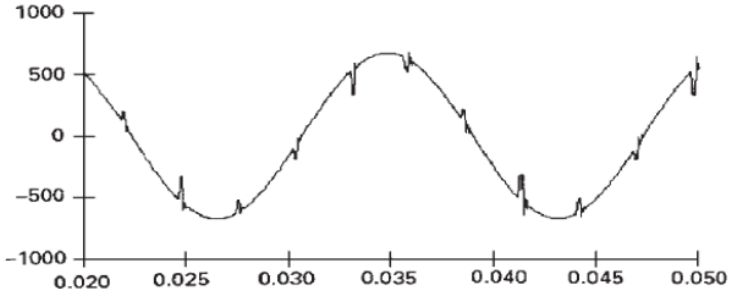


Figure 2.10: Notching waveform

2.2.6.3 Noise

Noise is an undesired signal added to the fundamental frequency of voltage or current in the phase or neutral conductor. It does not include transients and harmonic distortion. This issue is frequently exacerbated by a lack of improper or poor grounding in the system. The magnitude and frequency range of noise generally depend on the source and system characteristics. Typically, the spectral content is less than 200 kHz and its magnitude is less than 1% of the voltage magnitude (Abas et al., 2020).

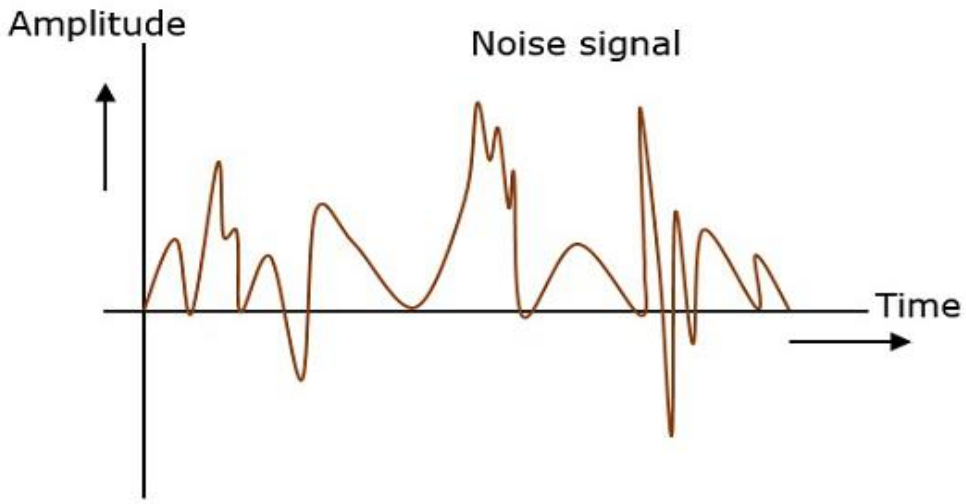


Figure 2.11: Noise in the phase current wave shape

2.2.6.4 Inter-harmonics

Interharmonics are voltages or currents that have frequency components that are not integer multiples of the supply system's operating frequency (e.g., 50 or 60 Hz). It can be caused by static frequency converters, cycloconverters, induction furnaces, and arcing devices. Interharmonics have a significant impact on transformer saturation and insulation stress (Cao et al., 2019).

2.2.6.5 DC Offset

A DC offset is the presence of DC current or voltage in an AC power system. It is caused by half-wave rectification. Grid-connected static power converters (caused by delay mismatch in gating circuits and power switch defects), HVDC transmission, and railway signaling equipment are the main sources of DC injection into the low- and medium-voltage AC grids. In normal operation, direct current in AC networks can destroy transformer cores by biasing them to saturate. As a

result, the transformer heats up more, and the life of the transformer shortens. Direct current can also cause grounding electrodes and other connectors to corrode electrolytically (Habte, 2018).

2.2.7 Power Frequency Variation

The electric power network is designed to operate at a specified value of frequency (i.e.,50 Hz or 60 Hz). Frequency fluctuation arises when there is an imbalance between supply and demand. The loss of a generator or the sudden change of loads can produce large variations in frequency. Faults in the bulk power transmission system, the disconnection of a significant block of load, or the shutdown of a large source of generation can all create frequency changes. Frequency variation has a direct impact on the operation of power consumers. For instance, the operation of an electric motor is harmed by frequency deviations, which result in changes in rotation frequency and active and reactive power consumption. Power plant equipment is the most vulnerable to frequency variation. Furthermore, because of an increase in the magnetization current and increased heating of steel elements, the lower frequency in the power network decreases the service life of steel-containing equipment (e.g., electric motors and transformers). Frequency variation, on the other hand, has a negligible impact on the operation of furnaces and lighting loads (Diahovchenko et al., 2019).

In this study, among the power quality problems that are mentioned in the above section, voltage sag and harmonics are investigated, and their proper mitigation technique is proposed

2.3 Power Quality Standards

A lot of power quality assessments and case research studies have been conducted by various utilities and consumers all over the world as a result of the growing awareness about power quality concerns. The increased demand for power quality monitoring has prompted the creation of standards that define measuring methods as well as how different power quality parameters are computed and interpreted. As a result, a number of international standards relating to power quality have been produced and implemented by a number of standard bodies. Examples of such organizations are the Institute of Electrical and Electronics Engineers (IEEE), the International Electro-Technical Commission (IEC), the American National Standard Institute (ANSI), and the National Electrical Manufactures Association (NEMA). When the voltage, current, or frequency deviates from normal levels, power quality standards protect utility and end-user equipment

against failure or malfunction. These standards provide protection by setting measurable limits as to how far the voltage, current, or frequency can deviate from normal values. Furthermore, power quality standards assist utilities and customers in determining what levels of service are acceptable and undesirable.

The IEEE standards and definitions will be used extensively in this study due to their widespread use in academic and research areas and also due to their high level of completeness in describing all of the major electrical phenomena that make up power quality.

The following are some of the IEEE standards related to power quality issues:

- IEEE Standard 1159-2009: Recommended Practice for Monitoring Electric Power Quality.
- IEEE Standard 1159.3-2003: Recommendations for transmitting data on power quality.
- IEEE Standard 519-2014: Recommendation and Requirements for Electrical Power Systems' Harmonic Control.

In this study, IEEE standard 519-2014 is used to analyze the harmonic distortion level of the Adama spinning factory distribution network.

Table 2.1: The current distortion limits for systems rated from 120 V to 69 KV

Maximum harmonics current distortion in percent of I_L						
Individual harmonic order (odd harmonics) [a,b]						
I_{SC}/I_L	$3 \le h \le 11$	$11 \le h \le 17$	$17 \le h \le 23$	$23 \le h \le 35$	$35 \le h \le 50$	TDD
< 20[c]	4.0	2.0	1.5	0.6	0.3	5.0
20 < 50	7.0	3.5	2.5	1.0	0.5	8.0
50 < 100	10.0	4.5	4.0	1.5	0.7	12.0
100 < 1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

[a]Even harmonics are limited to 25% of the odd harmonic limits above.

[b]Current distortions that result in a dc offset, e.g., half-wave converters, are not allowed.

[c]All power generation equipment is limited to these values of current distortion, regardless of actual ISC/IL

Where I_L is the maximum demand load current (fundamental frequency component) at the PCC under normal load operating conditions and I_{SC} is the maximum short-circuit current at the PCC

Table 2.2: Voltage distortion limits

Bus voltage V at PCC	Individual harmonics (%)	Total harmonic distortion THD (%)
$V \leq 1.0$ KV	5.0	8.0
1 KV $< V \leq$ 69 KV	3.0	5.0
69 KV $< V \leq$ 161 KV	1.5	2.5
161 KV $< V$	1.0	1.5[a]

[a]High - voltage systems can have up to 2.0% THD where the cause is an HVDC terminal whose effect will have attenuated at points in the network where future users may be connected.

2.4 Power Quality Problem Effects on Textile Factory

In the textile industry, which uses high-tech devices like electronic control cards and driver-controlled motors, poor power quality can damage the system and cause production failure. On the other hand, those adjustable speed drives are also another problem for the machinery since they are nonlinear loads.

2.4.1 Effects of Power Quality Problems on Weaving-Knitting

Textile weaving is used to create a diverse range of products. Weaved or knitted textiles make up the majority of our clothing, as well as the surface coverings of our seating sets in our rooms; tulle and curtains; carpets; bathroom towels; and even the airbags in our cars. Weaving and knitting machines are today's high-tech machines. The components include Ethernet cards; tens of sensors; encoders; driver-controlled AC and DC electrical machines; communications cards; touchscreens; Ethernet cards and CPU units. And these components operate at different voltage values. The occurrence of voltage sag or any voltage variation may cause the shutting down of these machines. This happens because of the sensitivity of these machines to sinusoidal electrical power.

Harmonics is another factor which causes a reduction in the life expectancy of all electrical and electronic components in these machines. In addition to this, they may cause breakdowns, which result in additional repair expenses and production losses. They also reduce machine depreciation times, resulting in higher expenditures and losses (Koçyiit et al., 2009).

2.4.2 Effects of Power Quality Problems on Dyeing Processes

The three most common types of dyeing techniques used in the textile industry are fiber, yarn, and fabric dyeing. Despite the fact that the physical structures of these machines differ, they all operate on the same principles since the materials they dye are the same. Driver-controlled pumps, level gauges, calorimeters, liquid meters, PLC devices or CPUs, control cards, touchscreen panels, actuator valves, proportional valves, and a variety of other electrical, electromechanical, and electronic sensors are included in these machines. Poor power quality is the main cause of the disruption of these machines, and the amount of money lost is determined by the length of the interruption period. In the event of a voltage drop or fluctuation, the machinery may activate the automated protection and shut down on its own (Koçyiit et al., 2009).

2.4.3 Effects of Power Quality Problems on Finishing Processes

The finishing process refers to the final steps in the production of textile products and includes a variety of machinery. Any malfunction with any component of this sophisticated system results in the line being shut down. On this machine, the shortening of the depreciation time owing to low power quality is even more important. Meanwhile, direct losses are accounted for when equipment fails due to harmonics or other issues with power quality. When the equipment breaks down, the machine stops and the time required for detection of the break-down and repair is a significant amount of time. In such circumstances, manufacturing losses will reach higher values.

2.5 Mitigation Techniques for Power Quality Problems

Electric utilities' major goal is to provide their consumers with sinusoidal balanced currents at the AC mains and an uninterrupted sinusoidal voltage of constant amplitude and frequency. Today's AC distribution systems, on the other hand, are affected by significant power quality (PQ) issues such as high reactive power, unbalanced loads, voltage sag, harmonics, and excessive neutral current. Furthermore, these utilities are unable to prevent voltage sags, swells, surges, notches, spikes, flickers, imbalances, and harmonics in supply voltages across the load ends of their customers. However, many essential and sensitive loads require constant magnitude and frequency sinusoidal balanced voltages, otherwise their protective systems will operate due to power quality disturbances. These power quality problems can be either from the utility side or the load side. These PQ issues might arise from either the utility or the load.

For instance, harmonics are power quality problems from the load side that are injected into the system because of nonlinear loads. These are the most common and dangerous problems that occur in textile industries since there are many nonlinear loads. Voltage sag is an additional power quality problem that can be sourced from both sides (i.e., load and utility). For example, due to a variety of factors, the voltage supplied by the utility may occasionally fall below the allowable limit. Short circuits in the distribution network can also cause this to happen.

As a result, for the industry to operate properly, these power quality problems must be mitigated. For that purpose, a number of solutions have been suggested, among which power electronics-based Custom Power Devices (CPDs) are the best and most cost-effective alternative for correcting and managing power quality problems. The employment of power electronic controllers for distribution systems to improve the quality and dependability of power delivered to clients is known as "custom power". They perform well at medium-distribution levels, and the majority of them are commercially available. The two types of CPDs are network reconfiguring and compensating CPDs (Prafull A. Desale, 2014).

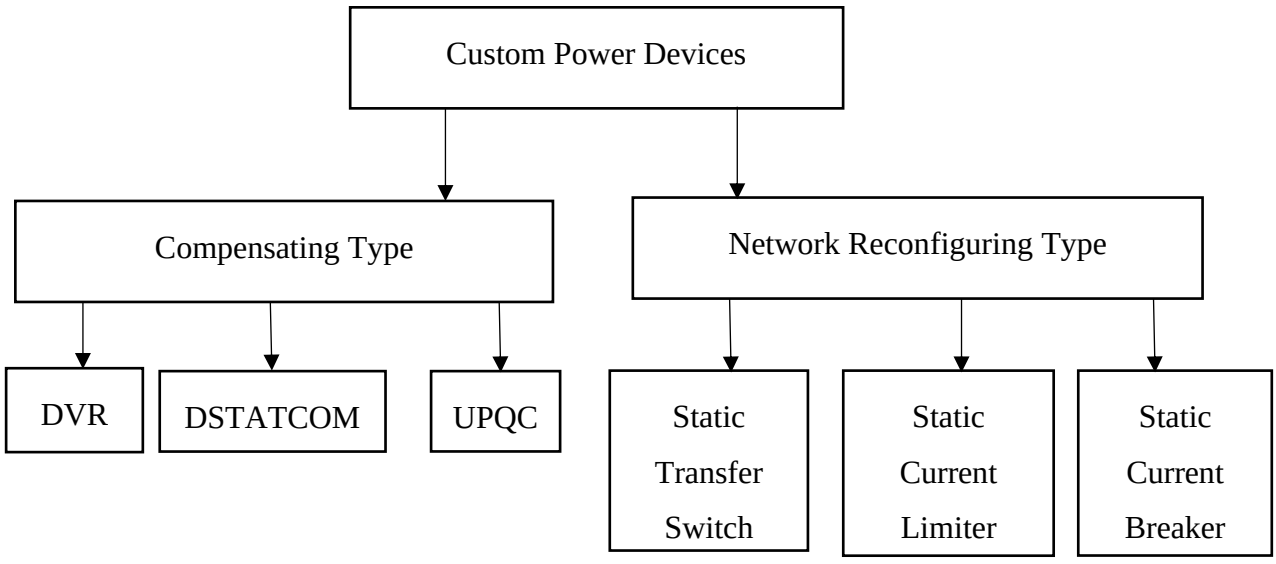


Figure 2.12: CPD's general classification

2.5.1 Network Reconfiguring Type CPDs

A conventional thyristor or a gate turn-off thyristor base can be used to reconfigure the network. Static Current Limiters and Static Circuit Breakers are commonly used for quick current limiting

and current breaking during faults. In the event of voltage sag/swell or a fault in the providing feeder, however, Static Move Switches (STS) are used to transfer a load to a separate feeder. The UPS is also classified as a network reconfigurable type CPD, which is used to mitigate voltage dips and short-term interruptions (Devaraju, 2010).

2.5.2 Compensating Type CPDs

Active filtering, load balancing, harmonics compensation, power factor enhancement, and voltage regulation (sag/swell) are all possible with compensating CPDs. Distribution static synchronous compensators, dynamic voltage restorers, and unified power quality conditioners are the three types of these devices (Devaraju, 2010).

2.5.2.1 Dynamic Voltage Restorer

The DVR is a device that connects in series between the source voltage and the load and protects the load from grid voltage distortions (DaneshvarDehnavi et al., 2021). It is the most cost-effective way to alleviate voltage sags, which are the most serious and common power quality problems in today's power system. When there is a voltage disturbance on the supply side, it injects the desired voltage to the load-side as a power electronic-based device. Furthermore, the DVR helps safeguard sensitive and crucial loads from supply-side interruptions. As a result, the DVR is important for voltage sag mitigation and sensitive load protection (Ali Moghassemi, 2020). The components of DVR include injection transformers, VSC, energy storage units, low pass filters, by-pass switches, etc.

a) Injection Transformer

The major role of the injection transformer is to connect the DVR to the distribution network through HV-windings, as well as to convert and relate injected compensating voltages created by voltage source converters to the incoming supply voltage (Muluk et al., 2017). The usage of a delta-star transformer prevents the transformer from passing zero-sequence voltages. As a result, positive and negative sequence voltages must be changed. As a result, positive and negative sequence voltage correction is necessary. In this circumstance, an open-delta injection transformer that can maximize the usage of DC-link voltage is highly suggested. In an earthed star–star transformer, zero-sequence voltages must be corrected for. An open-star injection transformer is used to accomplish this (Ali Moghassemi, 2020).

b) Voltage Source Converter

In the DVR, the VSC is utilized to convert DC voltage (energy storage or DC-link) to an AC desired voltage of any magnitude, frequency, and phase angle. The load voltage is thus maintained in a balanced state. The voltage generated by the VSC must be managed and injected through the transformers.

c) Energy Storage Unit

Energy is stored using a variety of devices, including flywheels, lead-acid batteries, superconducting magnetic energy storage (SMES), and super-capacitors. The storage unit's principal role is to provide the required actual power when there are voltage sags. The active power produced by the energy storage device determines DVR's compensating capability. Rather than using additional storage devices, the devices with the fastest charging and discharging response times are used. These are lead-acid batteries. The rate of discharge controls the amount of internal space available for energy storage, and it is determined by a chemical reaction (Abas et al., 2020).

d) Low Pass Filters

Low-pass filters are used to convert the PWM inverted pulse waveform into a sinusoidal waveform in this technique. The removal of high-value harmonic components during the DC-AC transformation is required for this conversion, and this will modify the corrected output voltage. A low-pass filter is a necessary component of a voltage source converter. As a result, it can be found on either the low voltage side of an injection transformer, such as the inverter side, or the high voltage side, such as the load side. If we put the filters on the inverter side, they can overcome the maximum value harmonics from passing through the voltage transformer. So, the stress on the injection transformer is also decreased by it. That is the filter's disadvantage. However, this problem can be solved by putting the filter on the load side. The secondary side of the transformer permits the high-valued harmonic currents because the transformer with high values is necessary (Eltamaly et al., 2018).

e) By-Pass Switch

Because the DVR is a series-connected device, if a problem in the downstream creates a fault current, the current travels via the inverter. The by-pass switch is intended to safeguard the inverter from damage (Eltamaly et al., 2018).

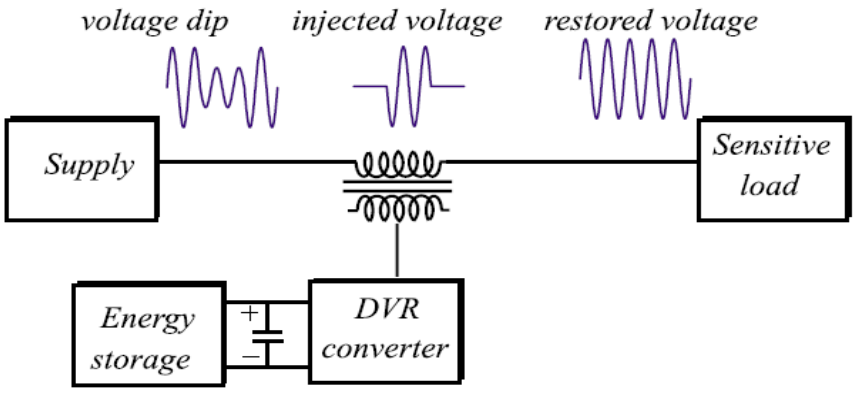


Figure 2.13: Schematic Diagram of DVR

2.5.2.2 Distribution Static Synchronous Compensator

A DSTATCOM is a device used to cancel load harmonics delivered to the supply. It is connected in parallel to the network and load and injects current into the PCC to compensate for undesirable load current components. This current cancels out the harmonic current created by the non-linear load, resulting in pure current flowing through the system. With a suitable control strategy, power factors and unbalanced loads can also be adjusted. This method can be used with any load that is categorized as a harmonic source. It benefits from simply carrying the compensation current and a small amount of active fundamental current to compensate for system losses. In general, load current balancing, flicker effect compensation, current harmonic distortion compensation, and power factor enhancement may all be done using it in distribution networks. DSTATCOM is a shunt-connected device with six IGBTs, three inductors, and DC energy storage in a three-leg voltage source converter (VSC) (Gidd et al., 2019).

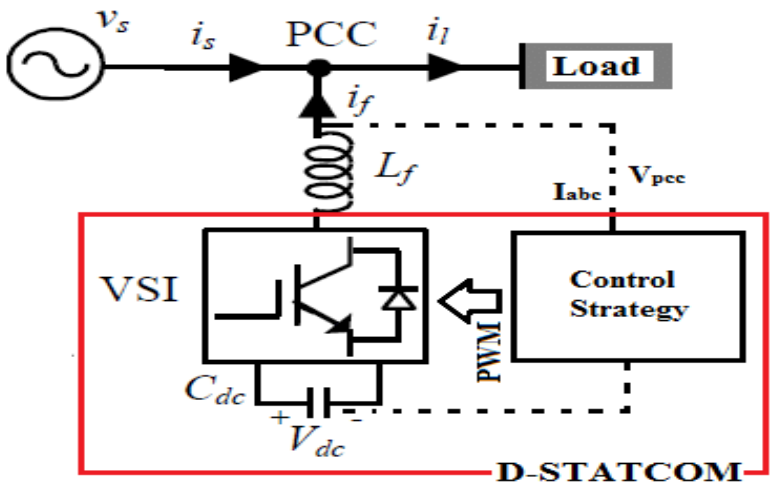


Figure 2.14: Schematic Diagram of DSTATCOM

2.5.2.3 Unified Power Quality Conditioner (UPQC)

UPQC compensate for load reactive power while mitigating voltage and current disturbances that could harm sensitive electrical loads. They're active power filters that combine series and shunt active filters to correct for voltage, current, and reactive power fluctuations simultaneously (Gunjan Varshney, D. S. Chauhan, 2016). A UPQC's power circuit consists of two VSCs connected back-to-back by a DC link. The DSTATCOM is a shunt device that is connected to the consumer load in parallel. Reactive power compensation, load balancing, and harmonic reduction are all done with it. A DVR, on the other hand, is a series device that protects the load end voltage against sag/swell, surges, spikes, notches, or imbalance. It injects a compensating voltage between the supply and the consumer load in order to restore the load voltage to its nominal value. A UPQC's principal function is to adjust for supply voltage flicker, imbalance, reactive power, negative-sequence current, and harmonics. In other words, the UPQC can improve power quality at the point of common coupling on power distribution systems or in industrial power systems (Ferdi, 2015).

The following are some of the advantages of employing a unified power quality conditioner (UPQC) for non-linear and voltage-sensitive loads:

- It lowers supply current harmonics, resulting in higher utility current quality for nonlinear loads.
- UPQC keeps the load end voltage at the rated value even when the supply voltage sags.

- The series compensator does not require any additional dc link voltage support since the voltage injected by UPQC to keep the load end voltage at the required value comes from the same dc link.

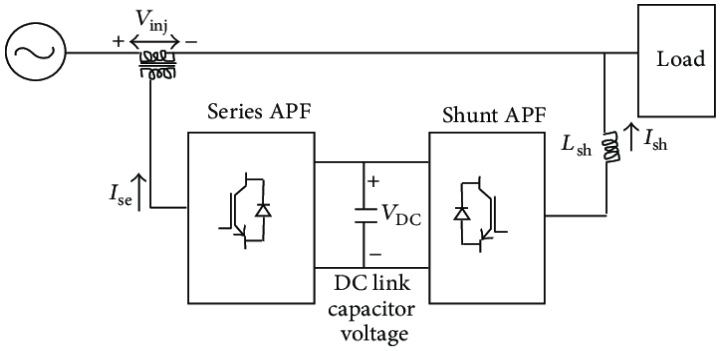


Figure 2.15: Schematic Diagram of UPQC

2.6 Review of Related Works

Electric power quality has become a major concern in recent years, especially with the development of sophisticated devices with greater performance in the electrical utility for automated distribution systems. Several studies on power quality issues have been conducted by a number of researchers. Brief summaries of literature reviews related to power quality are presented as follows:

In (Simarjeet Kaur, Thapar University, 2015), a four-wire three-phase system with a hybrid system of shunt passive and series active filters was built and simulated with MATLAB/SIMULINK. This system is employed to mitigate and compensate for the source current harmonics and unbalanced voltages respectively. It is also used to overcome problems caused by the utilization of the shunt passive filter alone. However, due to their high cost, large size, and resonance effect, passive filters are not widely used. Furthermore, Shunt passive filters are also not a good solution because the reactive power adjustment is fixed.

In (Leite et al., 2020) the Harmonic Compensation Strategy for Current-Controlled Converters based on Voltage Feedback is investigated. For Current Controlled Mode (CCM) converters, it proposes a voltage detection-based harmonic compensator. This work also proposes a voltage feedback-based harmonic compensator that directly operates on the modulation signals to incorporate CCM converters with both fundamental power management and advanced voltage harmonic compensation capabilities. The employment of CCM converters in grid-interactive

systems to achieve voltage harmonic correction makes this study unique. However, less reliability and dependence of the performance of the system on passive components are the major drawbacks of this method.

(Wang et al., 2018) investigated a novel three-level hybrid modular shunt active power filter. The traditional modular SAPF mathematical models are improved in this article to investigate tradeoffs between dynamic responsiveness and stability control. A novel hybrid modular three-level SAPF structure is proposed based on the analysis results derived from the model. Each module in the proposed system has its own current carrying capacity, LCL filter parameters, and switching frequency. In this study, wider and faster reference current tracking has been achieved, but it has unrealistic simulation modeling.

(Biricik, 2018) demonstrates the use of a passive shunt filter, TCR, and TSC for the improvement of power quality. The primary goal of this study was to develop several power quality enhancement approaches for increasing various power quality indices at AC mains and on the DC bus in an AC-DC converter with R-L load. It also aims to measure the level of improvement in various power quality indices in various application strategies. However, the drawback of using this method is mainly due to the poor performance of passive filters in comparison to other power electronic devices, such as custom power devices. Therefore, it is preferable to employ those current devices for better mitigation.

(Zhang et al., 2017) investigates the space vector modulation-based proportional resonant current controller for matrix converter systems with selective harmonics compensation. For the three-phase direct matrix converter and its application systems, this work also provides a Proportional Resonant (PR) controller based on the Space Vector Modulation (SVM) technique. The PR controller has a fast dynamic response, and the harmonic compensator can efficiently compensate for the desired harmonics. But this Proportional Resonant technique requires being designed and tuned to compensate for the fundamental component and specific harmonics, previous to the operation. In this circumstance, the controller's ability to safeguard the load from additional disruptions is limited. Covering additional frequencies complicates the control mechanism.

CHAPTER THREE

METHODOLOGY

3.1 Methods of Data Collection

The data are collected while all of the factory machines are running in order to determine the general characteristics of the industrial loads. The data for this study was gathered from both primary and secondary sources. The primary data obtained is the current and voltage harmonics fed into the system by nonlinear loads. The data was measured with a DELAB NV8s Power Factor Controller (PFC). Secondary data is acquired through factory records, personal interviews, and other sources. The collected data is then analyzed and compared to IEEE standards in order to recommend a power quality mitigation device for the factory.

Figure 3.1: DELAB NV-8s

3.2 Adama Spinning Factory Electric Distribution Network

The Adama Spinning Factory receives power from the Adama substation, which is approximately 4 kilometers away. The power from the substation enters the powerhouse directly, and there are four transformers in the powerhouse that are connected to feed various loads.

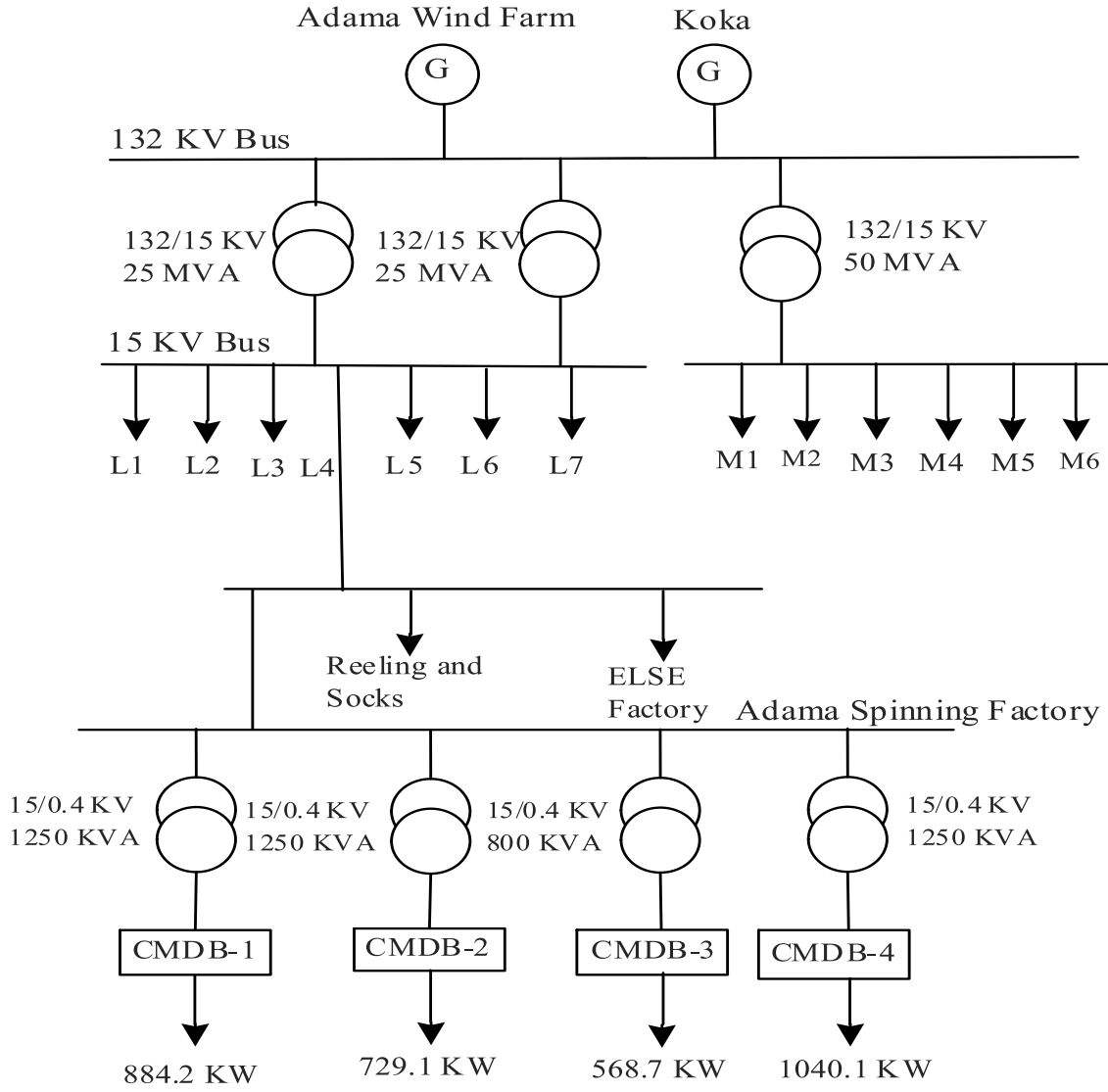


Figure 3.2: Single line diagram from Adama Substation to Adama Spinning Factory distribution network

In the above figure 3.2, the letters L and M represent the outgoing feeders from the old substation and mobile substation respectively.

Electrical power is delivered through four Central Main Distribution Boards (CMDBs). These four CMDBs feed a variety of loads via Sub Distribution Boards (SDBs) located throughout the plant near the loads they feed. Appendix A of this document contains the electrical installation layout for the Adama Spinning Factory.

3.3 Design of Factory's Distribution Network

Distribution is the final stage of electric power supply, in which electricity is transmitted from the transmission network to individual customers. The distribution network components, such as distribution transformers and installed loads under each transformer, must be modeled in order to conduct the analysis for this factory. Furthermore, under each CMDB, the capacitor banks utilized for power factor correction must be listed, as well as their ratings. The equivalent impedance diagram of the distribution network is used to model it. The calculations and assumptions used to model various components of the distribution network are discussed. The factory's distribution network is modeled, simulated, and analyzed using MATLAB/SIMULINK software.

3.3.1 Distribution Transformers

A distribution transformer reduces the voltage in distribution lines to the level required by the consumer in an electric power distribution system. The output voltage, kVA rating, percent impedance (% Z), and X/R ratio of transformers are all used to characterize them. The transformers' series resistances and leakage reactance are used to model them. Similar to the most power system analysis, the magnetizing current, shunt admittances, and core losses are ignored. Using equation 3.1, the transformer's impedance, Ztr, may be computed from the percentage impedance.

$$Z_{tr} = \frac{\%Z * (KV)^2 * 10}{KVA} \tag{3.1}$$

$$\%\ \text{Z at new KVA} = \frac{\text{base KVA new}}{\text{KVA given}} * \%\text{Z at given KVA} \tag{3.2}$$

The Adama spinning factory has one 15/0.4 KV, 800 KVA, %Z = 5.03, Delta-Wye, and three 15/0.4 KV, 1250 kVA, %Z = 5.05, Delta-Wye, step-down distribution transformers. For all of the transformers in this study, the base KVA has been set to 1250 KVA. The transformers' X/R ratio is usually not indicated on the nameplate. It can be acquired from the manufacturer or calculated

using the transformer's full load and no-load loss data. In this study, the X/R ratio has been calculated from the transformer's full load and no-load losses. For all transformers, the resistance and reactance values are computed as follows:

a) Three transformers (T1, T2, and T4) of rating 1250 KVA, 50Hz, 15/0.4 KV, %Z=5.01, I_{pri}=48.11A, I_{sec}=1804.22A, No load loss=2500 W; load loss=10500 W, Vector group: Dyn 5

By using the above equation (3.1)

$$Z_{tr} = \frac{5.01*(0.4)^2*10}{1250} = 6.413 m\Omega$$

To find the values of resistances and inductances, the X/R ratio should be calculated first.

$$R\% = \frac{Full\ load\ loss(W) - No\ load\ loss(W)}{Transformer\ rated\ power(KVA)*1000} * 100 \qquad (3.3)$$

$$R\% = \frac{10500(W) - 2500(W)}{1250KVA*1000} * 100 = 0.64\%$$

Then, X% can be calculated using the impedance relation $Z^2 = R^2 + X^2$:

$$X\% = \sqrt{(Z^2\% - R^2\%)}$$

$$X\% = \sqrt{(5.01^2 - 0.64^2)} = 4.97\%$$

Hence, X/R=X%/R%=4.97/0.64 =7.76

Then, the R_{tr} and X_{tr} can be calculated from Z_{tr} and X/R ratio.

R = 0.82 mΩ and X = 6.36 mΩ

b) Transformer (T3) of the rating 800KVA, 15/0.4KV, 50Hz, %Z=5.03, Ipri = 30.8A, Isec=1154.7A, Vector group =Dyn 5, No load loss= 1700W, Load loss=7700W.

Because the nameplate Z% value is specified as a base KVA on the transformer's rating, it must be converted to the selected base KVA, 1250 KVA. The %Z on the base KVA of 1250 KVA is:

$$Z\%\ at\ new\ KVA = \frac{1250\ \text{KVA}}{800\ KVA} * 5.03 = 7.86$$

$$Z_{tr} = \frac{7.86*(0.4)^2*10}{1250} = 10.06\ \text{m}\Omega$$

Similarly, the X/R ratio can be calculated using equation (3.3) and Z_{tr}.

$$R\% = \frac{7700(W) - 1700(W)}{800KVA * 1000} * 100 = 0.75\%$$

Then, $X\% = \sqrt{(Z^2\% - R^2\%)}$

$$X\% = \sqrt{(10.06^2 - 0.75^2)} = 10.032\%$$

As a result, X/R=X%/R%=10.032/0.75 =13.38

Then, Ztr and X/R ratio can be used to calculate transformer resistance and reactance.

R = 0.75 mΩ and X = 10.035 mΩ.

3.3.2 Installed Loads on Each Transformer

An electrical load is a power-consuming component or portion of a circuit. The electrical loads connected to the distribution boards are characterized as linear loads, with active and reactive powers computed on each distribution board using the actual power factor and installed load data. The factory's document is used to collect active power data for loads under each CMDB. Then, the reactive power consumed can be determined using the following formula:

$$S^2 = P^2 + Q^2 \tag{3.4}$$

To compute the reactive power, the apparent power must be calculated. Power factor can be expressed in terms of apparent power and real power as:

$$pf = \frac{P}{S} \tag{3.5}$$

Where pf, P, and S represent power factor, active power and apparent power respectively.

The actual power factor is calculated by taking the average of the power factors recorded at various points during the measurement. The average of the power factor recorded at various times is given in table 3.1 below. Each load under all the central main distribution boards (CMDBs) with their power consumption is written on Appendix A.

Table 3.1: Power Factor Recorded on different days

Date	CMDB-1	CMDB-2	CMDB-3	CMDB-4
3/1/2022	0.76	0.89	0.72	0.88
7/1/2022	0.74	0.84	0.71	0.93
10/1/2022	0.81	0.88	0.73	0.91
14/1/2022	0.83	0.9	0.76	0.9
17/1/2022	0.72	0.8	0.81	0.95
22/1/2022	0.79	0.79	0.78	0.92
25/1/2022	0.8	0.85	0.7	0.86
28/1/2022	0.83	0.86	0.75	0.89
1/2/2022	0.75	0.83	0.77	0.84
Average	0.78	0.85	0.75	0.9

- For the loads connected to CMDB-1, the active power is 884.2 KW. Hence, apparent power can be calculated as:

$$S = \frac{884.2}{0.78} = 1133.6KVA$$

So, reactive power becomes,

$$Q = \sqrt{S^2 - P^2} = \sqrt{1133.6^2 - 884.2^2} = 709.4KVar$$

- For the loads connected to CMDB-2, the active power is 729.1 KW. So, apparent power can be calculated as:

$$S = \frac{729.1}{0.85} = 857.8KVA$$

Similarly, the reactive power,

$$Q = \sqrt{S^2 - P^2} = \sqrt{857.8^2 - 729.1^2} = 451.92KVar$$

By adopting the same procedure, the active and reactive power of all the loads under each transformer can be summarized in table 3.2.

Table 3.2: Active and Reactive Power of loads under each CMDB

CMDB	Active Power (KW)	Power factor	Reactive Power (KVAr)
CMDB-1	884.2	0.78	709.4
CMDB-2	729.1	0.85	451.92
CMDB-3	568.8	0.75	501.63
CMDB-4	1040.1	0.9	503.74

3.3.2.1 Loads Causing Harmonics in Adama Spinning Factory

The Adama spinning factory employs technologically sophisticated and energy-efficient machinery that are sensitive to slight variations in the given power quality while also having a tendency to distort the supplied pure sine wave. AC and DC motors, microprocessor-based controllers, fluorescent and gas discharge lamps, resistive heaters, adjustable speed drives (ASDs), computers, and other loads are found in the factory. The nonlinear loads that cause harmonics in this industry are as described in the following:

- Adjustable Speed Drives
- Fluorescent lamps
- Computers
- Printers
- Rectifiers and etc.

In the factory Adjustable Speed Drives are the common cause for power current harmonic distortion. The number of ASDs under all Central Main Distribution Boards are listed in the table 3.3 below.

Table 3.3: Number of Adjustable Speed Drives under each CMDBs

CMDB	Quantity
CMDB-1	58
CMDB-2	24
CMDB-3	56
CMDB-4	5

3.3.3 Power Factor Controlling Unit of Each Distribution Board

In the Adama spinning factory, when the power factor goes below 0.95, a capacitor bank is employed as a power factor improvement device by connecting different sized capacitors step by step. A DELAB NV8s Automatic Power Factor Controller (PFC) is installed on all CMDB boards. Each CMDB's capacitor step is pre-designed based on the types and patterns of the loads connected to it. Anti-resonance harmonic filters are connected in series to each power factor compensating capacitor to detune the system and avoid resonance events. KVAr values are used to specify the three-phase shunt capacitors connected to the distribution network on each CMDB board. In addition to the KVAr values, the nameplate data includes the capacitance values of each step capacitor for 50 and 60 Hz systems. Table 3.4 lists the KVAR values of all step capacitors and the anti-resonant reactors' series-connected inductance values for each CMDB board.

Table 3.4: Capacitors and Reactors installed under each CMDB

CMDB	Capacitor			Anti-resonant reactor
	Step	Detail	KVAr	Inductance
CMDB-1	3	1x20KVAr 2x10KVAr	40	1.922mH 3.876 mH
CMDB-2	5	2x50KVAr 2x25KVAr 1x12.5KVAr	162.5	0.768mH 1.533mH 3.07mH
CMDB-3	5	2x50KVAr 1X25KVAr 2x12.5KVAr	150	0.768mH 1.533mH 3.07mH
CMDB-4	7	4x50KVAr 2x25KVAr 1x12.5KVAr	262.5	0.768mH 1.533mH 3.07mH

3.4 Data Analysis and Comparison with IEEE Standard

The data gathered from measurements and recorded sources are examined. After performing the necessary analysis, the data is computed and compared to the IEEE suggested practice for power quality monitoring.

3.4.1 Voltage Sag Analysis

Voltage sags are frequent phenomena in industries that cause numerous losses. Variable speed drives and other industrial control systems are particularly vulnerable to these faults. If these faults are not addressed within a short period of time, the equipment may malfunction. As a result, in

order to avoid these problems, it is critical to analyze, identify, and describe them (Camarillo-Penaranda & Ramos, 2019). A voltage sag analysis is required to predict the impact of these problems on sensitive loads and industrial activities. Voltage sag can be caused by many conditions such as (Holm-nielsen, 2021):

- Electrical short circuit
- Switching on large loads at the same time
- Arcing fault in the system
- DOL starting of large motors.

From the personal interview and maintenance report of the factory, it has been known that voltage sag is a common problem in distribution boards CMDB-2 and CMDB-4 that is caused by the short circuits and arcing fault. When the short circuit happens, the motors stop suddenly because of reduced voltage magnitude and this leads to burnout of motors and other PCB circuits. Many motors under CMDB-2 and CMDB-4 are damaged by this voltage sag problem. Even though they can be maintained, a lot of them are damaged after rewinding four or five times. The main source of this problem is the occurrence of different short circuits in the industry's electrical system. It is primarily due to winding insulation failure, mechanical damage to wires, and improper wiring. The voltage sag data recorded manually are attached in appendix D of this document. Therefore, in order to avoid this problem, appropriate mitigating techniques must be utilized.

The most cost-effective technique to reduce voltage sag in the distribution system is to use a Dynamic Voltage Restorer (DVR). It recovers the load voltage to its reference value by injecting a compensating voltage between the supply and the consumer load. It's a vital and modern custom power device that compensates for voltage sags caused by faults or delivered directly from the utility. It is a quick, versatile, and effective voltage sag remedy (Mohammed et al., 2013).

In this study, DVR is used for voltage sag mitigation, and it is connected to CMDB-2 and CMDB-4 since the voltage sag is detected on these boards from the gathered data.

3.4.2 Harmonics Analysis

IEEE Std 519-2014 is the most widely used industry standard for harmonics in power systems(Ali Moghassemi, 2020). The I_{SC}/I_L ratio is the ratio of short circuit current available at PCC to the maximum fundamental load current. The number of harmonics a facility can inject into the utility's

distribution system is influenced by the amount of current it draws, according to the standard. The short circuit ratio (I_{SC}/I_L) is calculated in this section to select the maximum TDD limit for each transformer. The following are steps followed.

The three-phase short-circuit I_{SC} is expressed in amperes, but if it is given in MVA, the following formula is used to convert it to an amperage value:

$$I_{SC} = \frac{MVA*1000}{\sqrt{3}*KV} \tag{3.6}$$

The MVA and kV indicate a three-phase short-circuit capacity in mega-volt-amperes and the line-to-line voltage at the PCC in kV, respectively. The current in a short circuit can alternatively be described as:

$$I_{SC} = \frac{V_{ph}}{Z_{sc}} \tag{3.7}$$

Percentage reactance, %Xtr, can be expressed as:

$$\%X_{tr} = \frac{I_{FL}X_{tr}}{V_{ph}}*100 \tag{3.8}$$

Then, from equation (3.8), X_{tr} is given by

$$X_{tr} = \frac{\%X*V_{ph}}{I_{FL}*100} \tag{3.9}$$

Where I_{FL} is the full load current, Vph is phase voltage, and Xtr is reactance in ohms per phase of each transformer.

Hence,

$$I_{SC} = \frac{I_{FL}*100}{\%X_{SC}} = \frac{I_{FL}*100}{\%X_{tr}} \tag{3.10}$$

Then, $\%X_{tr}$ and I_{SC} for all the transformers can be determined by using equations 3.1 and 3.10.

- For transformers (T1, T2, T4)

$$\%X_{tr} = \frac{KVA*X_{tr}}{10(KV)^2} = \frac{1250*0.00636}{10*(0.4)^2} = 4.97$$

Then the short circuit current, I_{SC} can be;

$$I_{SC} = \frac{I_{FL} * 100}{\%X_{tr}}$$

Where I_{FL} represents the secondary side current and is determined as:

$$I_{FL} = \frac{KVA}{\sqrt{3} * KV} \tag{3.11}$$

$$I_{SC} = \frac{I_{FL} * 100}{\%X_{tr}} = \frac{1804.22 * 100}{4.97} = 36302.21A$$

- For transformer (T3)

$$\%X_{tr} = \frac{KVA * X_{tr}}{10(KV)^2} = \frac{800 * 0.010035}{10 * (0.4)^2} = 5.02$$

$$I_{SC} = \frac{I_{FL} * 100}{\%X_{tr}} = \frac{1154.7 * 100}{5.02} = 23002A$$

The load's average active demand power must be known to calculate the average demand current. This power is obtained from the factory's monthly energy consumption, which is presented in Appendix C. This report is prepared using measured values at the PCC for all four transformers, and it is used by utilities for billing purposes. Note that the average active demand power is computed between July 2020 and June 2021.

$$\text{PD} = \frac{\text{Sum of max.demand (July,2020 to June,2021)}}{12} \tag{3.12}$$

$$P_D = \frac{13780.2}{12} = 1148.35KW$$

Then, the average demand current can be calculated as follows.

$$I_L = \frac{P_D}{\sqrt{3} * KV * pf} \tag{3.13}$$

The power factor (pf) is calculated by taking the average of the actual power factor measured for billing purposes from July 2020 to June 2021. The resulting power factor is 0.878.

$$I_L = \frac{1148.35}{\sqrt{3} * 0.4 * 0.878} = 1887.6A$$

Each transformer's average demand current is determined using the average load share of the four transformers. Each transformer's percentage load share is computed by dividing its energy consumption by the total energy consumption of the four transformers. As a result, the load share percentage and demand current can be represented as follows:

- For T1, percentage Load share = 27.44%, then I_L=517.96 A
- For T2, percentage Load share = 22.63%, then I_L=427.16 A
- For T3, percentage Load share = 17.65%, then I_L=333.16 A
- For T4, percentage Load share = 32.28%, then I_L=609.32 A

Therefore, the short circuit ratio (I_{SC}/I_L) for each transformer becomes:

For T1: Isc/I_L= 36302.21/517.96=70.1 For T2: Isc/I_L= 36302.21/427.16=84.99

For T3: Isc/I_L= 230021/333.16=69.04 For T4: Isc/I_L= 36302.21/609.32=59.58

As a result, based on Tables 2.1 and 2.2, the following standard limits for the distribution network under investigation have been defined.

- A maximum permissible voltage THD level of 8% will be used for all CMDB boards, with a maximum percentage of 5% for individual harmonic components.
- Maximum permissible current TDD level of 12%, will be used for all the Central Main Distribution Boards (CMDBs) since $50<I_{SC}/I_L<100$.

The measured harmonic distortion data for all CMDBs are examined in order to give a mitigation approach for the distribution board having this power quality issue. The measured data is attached in Appendix B. As previously stated, the DELAB NV8s PFC device was used for the measurement. This device is installed on each CMDB board for controlling and correcting the power factor on the respective transformers. However, the lack of data storage capability is the main disadvantage of these devices. The harmonic distortion data are measured manually at various time intervals. The accuracy of this method is highly dependent on the precision of the data collector.

3.4.2.1 Harmonic Distortion Analysis for CMDB-1

The voltage as well as current harmonic distortion were measured on the secondary side of transformers. Tables 2.1 and Table 2.2 show the IEEE recommended voltage and current distortion

limitations in percent of the rated power frequency voltage, Vr, and maximum demand current, I_L, respectively. In the preceding section, the average demand current for transformer T1 is determined.

To do the computations with the measured values, this value must be transferred to the primary side of the CT. The average demand current on the secondary side of this distribution board is 517.96A, and with a transformation ratio of 500, it can be referred to the primary side of the CT. On the primary side, the average demand current becomes 1.04A.

For the average demand current of 1.04A, the Total Demand Distortion (TDD) can be calculated using the equation (2.5). It is obtained from the data collected on February 24, 2022, when the THD_I was at its highest.

$$TDD = \frac{\sqrt{I_3^{\,2} + I_5^{\,2} + I_7^{\,2} + I_9^{\,2} + I_{11}^{\,2}}}{I_L} = \frac{\sqrt{0.06^2 + 0.19^2 + 0.09^2 + 0.04^2}}{1.04} = 21.38\%$$

Since the TDD of CMDB-1 is above the maximum permitted value, i.e., 12%, the current harmonic distortion exists on this board. For the 5/2/2022 measurement, the voltage total harmonic distortion (THD_V) reaches its highest value of 2.91%. Therefore, THD_V and all individual voltage harmonic values, are within the IEEE voltage harmonic distortion limit of 8%.

3.4.2.2 Harmonic Distortion Analysis for CMDB-2

The average demand current for this distribution board is 427.16A, and it can be referred to the primary side of the CT with a transformation ratio of 2500/500=500. The average demand current at the primary side becomes 0.85A. The TDD can then be calculated for the data collected on 22/2/2022, which shows the maximum current harmonic distortion.

$$TDD = \frac{\sqrt{I_3^{\,2} + I_5^{\,2} + I_7^{\,2} + I_9^{\,2} + I_{11}^{\,2}}}{I_L} = \frac{\sqrt{0.03^2 + 0.05^2 + 0.04^2 + 0.01^2}}{0.85} = 8.41\%$$

The Total Demand Distortion calculated confirms that CMDB-2 is within the IEEE standard current harmonic limit. On the other hand, the maximum THD_V measured on this distribution board is 2.41%, which was recorded on 12/2/2022. Therefore, this board is free from harmonic distortion since this value is also below the IEEE maximum voltage distortion limit.

3.4.2.3 Harmonic Distortion Analysis for CMDB -3

The average demand current is 333.16 A and it is transferred to the primary side of the CT to determine Total Harmonic Distortion (TDD). The CT installed on CMDB-3 has a transformation ratio of 1250/5=250. Hence, the average demand current at the primary side is 1.33A. TDD is calculated as follows:

$$TDD = \frac{\sqrt{I_3^{\,2} + I_5^{\,2} + I_7^{\,2} + I_9^{\,2} + I_{11}^{\,2}}}{I_L} = \frac{\sqrt{0.03^2 + 0.18^2 + 0.09^2 + 0.03^2}}{1.33} = 15.48\%$$

The current harmonic distortion is also existing on this board since the TDD of CMDB-3 is greater than the maximum allowed value, i.e.12%. On the other hand, the voltage total harmonic distortion (THD_V) for the 9/2/2022 measurement, reaches its highest value of 2.32%. Hence, this board is free of voltage harmonic distortion since this number is within the IEEE voltage harmonic distortion standard.

3.4.2.4 Harmonic Distortion Analysis for CMDB-4

This distribution board's average demand current is 609.32A, and with a transformation ratio of 1600/5=320, it can be referred to the primary side of the CT. The average demand current at the primary side becomes 1.9A. The TDD can then be calculated for the data collected on 7/2/2022, which shows the maximum current harmonic distortion.

$$TDD = \frac{\sqrt{I_3^{\,2} + I_5^{\,2} + I_7^{\,2} + I_9^{\,2} + I_{11}^{\,2}}}{I_L} = \frac{\sqrt{0.01^2 + 0.04^2 + 0.08^2 + 0.01^2}}{1.9} = 4.77\%$$

The Total Demand Distortion (TDD) calculated for CMDB-4 confirms that this board is within the IEEE standard current harmonic limit. On the other hand, the maximum THD_V measured on this distribution board is 1.61%, which was recorded on 14/2/2022. Therefore, this board is free from harmonic distortion since this value is also below the IEEE maximum voltage distortion limit (i.e., 8%).

Table 3.5: Summary of Harmonic Distortion Analysis for all CMDBs

CMDB	THD_V (%)		TDD (%)	
	Actual	IEEE Standard	Actual	IEEE Standard
CMDB-1	2.91	8	21.38	12
CMDB-2	2.41	8	8.41	12
CMDB-3	2.32	8	15.48	12
CMDB-4	1.61	8	4.77	12

The following are a summary of the data collected and analyzed:

- The current distortion levels on distribution boards CMDB-1 and CMDB-3 exceed the IEEE standard limits.
- For all of the Central Main Distribution Boards, the voltage harmonic distortion is below the IEEE standard limits.

3.5 Design of Mitigation Techniques

From the above analysis, it can be concluded that Adama spinning factory has power quality issues such as current harmonics and voltage sag. Therefore, the development of an appropriate mitigating device is necessary in order to address these issues for the improvement of the industry's performance. A DSTATCOM is a power electronics-based device that is connected in parallel with a load bus and is often used to reduce line current harmonics. DVR, on the other hand, is designed to minimize voltage sag (Al-Ammar et al., 2021). As a result, DSTATCOM is used to tackle source current harmonics and DVR is to mitigate sag in load voltage (J.Bangarraju et al., 2017).The secondary side of distribution transformers is chosen as the point of common coupling (PCC) because it is a favorable point for compensating both current harmonics and voltage sag. It is selected because the nonlinear loads producing harmonics are at the secondary side of transformer and hence this distorted current should be compensated before returning back to supply side. Also for the DVR the secondary side of distribution transformer is chosen to protect the loads from the voltage sag created by different fault types at the primary side of transformer. Hence both the

mitigating devices are placed on the secondary side of transformer. The processes used in the design, as well as the assumptions made, are detailed further down.

3.5.1 Design of Distribution Static Synchronous Compensator (DSTATCOM)

DSTATCOM's parameters such as DC bus voltage, DC bus capacitance, and interfacing inductance are designed in this section.

3.5.1.1 DC Bus Voltage

The minimum DC bus voltage of VSC should be more than twice the crest of the AC electrical system's phase voltage. The voltage on the DC bus is calculated using the formula below:

$$V_{DC} = 2\sqrt{2}V_{LL} \Big/ \sqrt{3}m \tag{3.14}$$

Where V_{LL} represents the line-to-line voltage and m is the modulation index. The parameter m is less than 1 under normal working conditions (Alam & Arya, 2020).

By considering m = 1, the DC bus voltage can be

$$V_{DC} = 2\sqrt{2} * 400 \Big/ \sqrt{3} = 653.2V$$

However, the attainable voltage at the DSTATCOM output terminal will be lower than the estimated one in practice due to the switching device's dead-band and transition times. As a result, the DC bus voltage of 800V is selected.

3.5.1.2 DC Bus Capacitance

The amount of transient energy required during load changes determines the DC bus capacitance. Because the energy stored in the capacitor is used to supply the load's energy requirement for a portion of a power cycle, the relationship is expressed as:

$$1/2 (V^2_{DC} - V^2_{DC1}) C_{DC} = 3V_f I_f \Delta t \tag{3.15}$$

Where V_{DC} is the maximum voltage, V_{DC1} is the allowed DC bus voltage reduction during transients, t is the time when the backup is required, and C_{DC} is the DC bus capacitance (Singh,

Bhim, Ambrish Chandra, 2015). The DC bus voltage can't reach exactly at the DSTATCOM output terminal. Hence the voltage selected should be greater than the one that is calculated.

When t = 0.1 ms, V_{DC} = 800 V, and V_{DC1} = 653.2 V are taken into account, equation (3.15) produces:

$$\frac{1}{2}(800^2 - 653.2^2)C_{DC} = 3*214.56*1052.4*0.1*10^{-3}$$

It gives C_{DC} = 4490.7 μF. Hence, a 4500 μF DC bus capacitor is selected.

3.5.1.3 Coupling Inductor

The AC inductance (L_f) of a VSC is determined by the current ripple, Icr, pp, switching frequency, fs, and DC bus voltage (V_{DC}), which is expressed as:

$$L_f = \frac{\sqrt{3}mV_{DC}}{12af_sI_{cr,pp}} \tag{3.16}$$

where m and a represent modulation index and overloading factor respectively.

For output currents greater than 5%–15% of full load, the current in the inductor will be continuous. Therefore, the ripple current of 10% is considered in this design. This ripple current is the percentage of the current supplied through the interfacing inductors. The rate at which a switching device is turned on or off is called the switching frequency (fs). Frequencies typically range from a few KHz to a few MHz (10 KHz-2MHz).

By considering, Icr, pp = 10%, fs = 10 kHz, m = 1, V_{DC} = 800 V, and a = 1.2 in equation (3.16), the AC inductance (L_f) of a VSC becomes:

$$L_f = \frac{\sqrt{3}*800}{12*1.2*10000*0.1} = 96.2mH$$

3.5.2 Design of Dynamic Voltage Restorer

The injection transformers, VSC, coupling inductors, and ripple filter parameters for the dynamic voltage restorer are designed as follows.

3.5.2.1 Design of an Injection Transformer

A VSC of DVR is connected to the supply in series via the injection transformer. The transformer's voltage rating is determined by the voltage to be injected as well as the VSC bus voltage (Singh, Bhim, Ambrish Chandra, 2015). The voltage to be injected to compensate for voltage variation is calculated as follows:

$$V_{DVR} = X * V_S \tag{3.17}$$

Where X represent percentage of voltage sag and V_S is the phase supply voltage. In Adama Spinning factory, the single phase voltage reduces up to about 200V during voltage sag. However, this voltage might be reduced more than this percentage reduction on the other day. As a result, by assuming the voltage variation of 20%, the voltage that DVR must inject to compensate for this voltage variation in the system is:

$$V_{DVR} = 0.2 * 230.95 = 46.19V$$

The following formula can be used to calculate the injection transformer's turn ratio: A PWM controller can be used to generate 400 V across the line at the VSC's output using a DC bus voltage of 800 V (selected for 400 V for the DSTATCOM). In contrast, the DVR requires only 46.19 V per phase. Therefore, the injection transformer's maximum turn ratio is:

$$K_{DVR} = \frac{V_{VSC}}{V_{DVR}} \tag{3.18}$$

$$K_{DVR} = \frac{400}{\sqrt{3} * 46.19} = 4.99 \approx 5$$

The injection transformer's power rating can then be determined as follows:

$$S_{DVR} = 3V_{DVR} * I_{DVR(under-sag)} \tag{3.19}$$

The Load under CMDB-2 is 729.1 KW with a power factor of 0.85. The apparent power rating of the DVR that injects this voltage through the injection transformer can be calculated from the current during sag condition. Hence, the VA rating of DVR becomes

$$S_{DVR} = 3 * 46.19 * \left(\frac{729.1}{\left(3 * \left(230.95 - 0.2 * 230.95\right)\right)} \right) = 182.28KVA$$

For the load of CMDB-4, the active power is 1040.1 KW with a power factor of 0.9.

Then, the DVR VA rating is:

$$S_{DVR} = 3*46.19*\left(\frac{1040.1}{\left(3*\left(230.95-0.2*230.95\right)\right)}\right) = 260.03KVA$$

3.5.2.2 Design of the Interfacing Inductors

The real power of the load determines the current through the secondary side of the injection transformer. The supply current is at its lowest during a voltage swell (Singh, Bhim, Ambrish Chandra, 2015). The transformer's supply current must be at least:

$$I_{DVR(under-swell)} = P_L \big/ 3(1+X)V_S \tag{3.20}$$

For CMDB-2, the load power of 729.1 KW,

$$I_{DVR(under-swell)} = 729100 \big/ 3*(1+0.2)*230.95 = 876.93A$$

Assuming a 10% ripple in supply current, the value of filter inductance of the DVR is given as:

$$L_{DVR} = (\frac{\sqrt{3}}{2})m*V_{DC}*K_{DVR}/6af_s*\Delta I_{DVR} \tag{3.21}$$

By substituting the values,

$$L_{DVR} = \sqrt{3} \big/ 2 *1*800*5/(6*1.2*10000*0.1*876.93) = 0.55mH$$

For CMDB-4,

$$I_{DVR(under-swell)} = 1040000.1 \big/ 3*(1+0.2)*230.95 = 1250.9A$$

Then,

$$L_{DVR} = \sqrt{3} \big/ 2 *1*800*5/(6*1.2*10000*0.1*1250.9) = 0.38mH$$

3.5.2.3 Design of Voltage Rating of Series Voltage Source Converter

The DC bus voltage of a three-phase rectifier load is used to construct the DVR. Because the DVR injects the load voltage's harmonic component, the PCC voltage is the basic component. The switching frequency (fs) in the DVR is set to 10 kHz. The VSC's DC voltage (V_{DC}) is set at 800 V, and it must be kept within a 10% tolerance. The inductor's ripple current is limited to 10% of the current flowing through the series VSC.

The fundamental component of the load AC voltage is:

$$V_{LL} = \sqrt{6}/\pi * V_d \tag{3.22}$$

For a V_{LL} of 400 V, V_d is 513 V.

The difference between the PCC and load voltages for a given line voltage of 400 V and a DC load voltage (Vd) of 513 V is used to calculate the voltage rating of the series VSC. It can be calculated as:

$$V_f = \sqrt{\left[1/\pi \left\{ \int_0^{\pi/3} (V_{ph}\sqrt{2}\sin\theta - V_d/3)^2 d\theta + \int_{\pi/3}^{2\pi/3} (V_{ph}\sqrt{2}\sin\theta - 2V_d/3)^2 d\theta + \int_{2\pi/3}^{\pi} (V_{ph}\sqrt{2}\sin\theta - V_d/3)^2 d\theta \right\} \right]}$$

$$V_f = \sqrt{\left[1/\pi \left\{ \int_0^{\pi/3} (230.95\sqrt{2}\sin\theta - 513/3)^2 d\theta + \int_{\pi/3}^{2\pi/3} (230.95\sqrt{2}\sin\theta - 1026/3)^2 d\theta + \int_{2\pi/3}^{\pi} (230.95\sqrt{2}\sin\theta - 513/3)^2 d\theta \right\} \right]}$$

$$V_f = \sqrt{\left[1/\pi \left\{ \int_0^{\pi/3} (326.62\sin\theta - 171)^2 d\theta + \int_{\pi/3}^{2\pi/3} (326.62\sin\theta - 342)^2 d\theta + \int_{2\pi/3}^{\pi} (326.62\sin\theta - 171)^2 d\theta \right\} \right]}$$

$$V_f = \sqrt{\left[1/\pi \left\{ 29564.58 + 116158.42 + 25514.27 \right] \right.}$$

$$V_f = \sqrt{46036.93} = 214.56V$$

The three-phase diode rectifier load's diodes conduct continuously (each diode conducting for 180°) since sine waves supply current after compensation and a stepped waveform of the phase voltage at the diode bridge's input with:

- The first step of π/3 angle (from 0° to π/3) with a magnitude of Vd/3.

- The second step of π/3 angle (from π/3 to 2π/3) with a magnitude of 2Vd/3, and
- The third step of π/3 angle (from 2π/3 to π) with a magnitude of Vd/3, and it has both half cycles of symmetric segments of such steps.

3.5.2.4 Design of current Rating of Series Voltage Source Converter

The DVR's current rating is determined by the fundamental component of load current, as shown below.

The load power is calculated as:

$$P_{DC} = \frac{V_d^{\,2}}{R} \tag{3.23}$$

Where R denotes the DC load's equivalent resistance at the diode bridge rectifier's output. The rms supply current is calculated as follows, assuming a unity power factor and a lossless series VSC:

$$I_f = \frac{P}{\sqrt{3}V_{LL}} \tag{3.24}$$

$$I_f = \frac{729100}{\sqrt{3}*400} = 1052.4A$$

3.5.2.5 Design of kVA Rating of a VSC

The series VSC's kVA rating is calculated as follows:

$$KVA = \frac{3V_f I_f}{1000} \tag{3.25}$$

Then by substituting the respective values in equation (3.25):

$$KVA = \frac{3*214.56*1052.4}{1000} = 677.41KVA$$

3.6 Control of Mitigating Devices

A control mechanism is required to generate the gate pulse for the voltage source converter so that the chosen mitigation device can execute its function. The DSTATCOM and DVR are controlled using a variety of time domain and frequency domain control techniques. These control methods

are used to create reference currents and voltages in order to regulate the VSC with a pulse. Since frequency domain control algorithms are sluggish, wasteful, and require a lot of computation, they are not as good as time-domain control algorithms for real-time control of these compensators (Singh & Badoni, 2021).

Some of the time-domain control algorithms are: Synchronous reference frame (SRF) theory, Instantaneous symmetrical component theory, Instantaneous reactive power theory (IRPT), Current synchronous detection (CSD) approach, Power balance theory (BPT), and others.

The SRF algorithm has a number of advantages over other time-domain algorithms, including a simple design, increased speed, and fewer calculations, all of which make it more likely to be applied in practice (Hoon et al., 2016). By lowering the number of computations necessary, SRF-based control reduces the overall complexity of the control system (Al-Ammar et al., 2021). As a result, this control theory is used in this study.

3.6.1 Reference Current Generation and Control of DSTATCOM

The DSTATCOM is a common CPD for tackling current-based power quality issues. In this study, synchronized reference frame theory is used to manage the DSTATCOM's VSC.

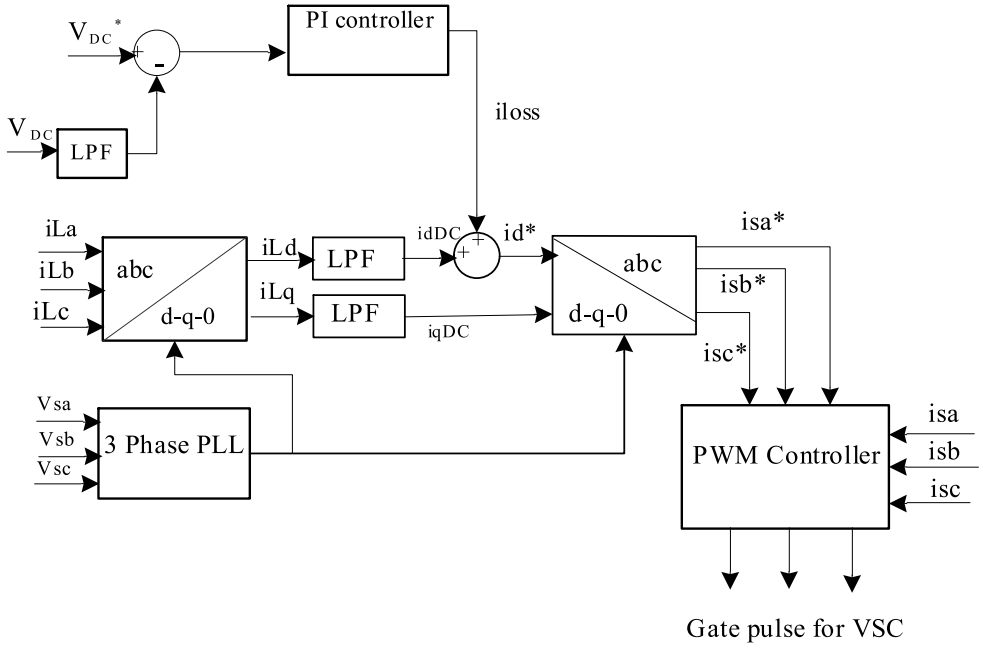


Figure 3.3: Block diagram of SRF theory-based control algorithm for DSTATCOM

PCC voltages (vsa, vsb, vsc), Load currents (iLa, iLb, iLc) and the DC bus voltage (VDC) are all detected as feedback signals. Park's transformation is used to convert the load currents in the three phases to the dq0 frame (Singh, Bhim, Ambrish Chandra, 2015). Then the reference currents generated from the output of inverse Park transformation is compared with the source current in the PWM controller block to generate the gating pulse that triggers the VSC.

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \text{Cos}\,\theta & \text{Cos}(\theta-\frac{2\pi}{3}) & \text{Cos}(\theta+\frac{2\pi}{3}) \\ -\text{Sin}\,\theta & -\text{Sin}(\theta-\frac{2\pi}{3}) & -\text{Sin}(\theta+\frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{3.26}$$

The inverse Park's transformation is defined by the following transformation matrix.

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} \text{Cos}\,\theta & \text{Sin}\,\theta & 1 \\ \text{Cos}(\theta-\frac{2\pi}{3}) & \text{Sin}(\theta-\frac{2\pi}{3}) & 1 \\ \text{Cos}(\theta+\frac{2\pi}{3}) & \text{Sin}(\theta+\frac{2\pi}{3}) & 1 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \tag{3.27}$$

To synchronize these signals with the PCC voltages, a three-phase PLL is required. Low-pass filters (LPFs) are employed to extract the DC components of iLd and iLq from these d–q current components. The following are the fundamental and harmonic components of the d-axis and q-axis currents:

$$i_{Ld} = i_{dDC} + i_{dAC} \tag{3.28}$$

$$i_{Lq} = i_{qDC} + i_{qAC} \tag{3.29}$$

An LPF separates the non-DC qualities from the reference signals by deriving DC quantities from an SRF controller.

3.6.2 Reference Voltage Generation and Control of Dynamic Voltage Restorer

The synchronous reference frame theory and hysteresis voltage control are used to control the system. The source voltage Vsabc is measured and fed into the transformation block (abc/dq0), while the load current (iLabc) is fed into the PLL block. This block generates sin-cos functions,

which are subsequently used as parameters by both the transformation (abc/dq0) and inverse transformation (dq0/abc) blocks. Following that, the voltage of the inverse transformation block is compared to the reference value. The voltage signal created by DVR (V_{DVR}) is then set to the hysteresis voltage controller, which generates inverter switching pulses (Ilamkar & Joshi, 2018). The source voltage is converted to a dq0 frame using Park's transformation as follows:

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \text{Cos}\,\theta & \text{Cos}(\theta - \frac{2\pi}{3}) & \text{Cos}(\theta + \frac{2\pi}{3}) \\ -\text{Sin}\,\theta & -\text{Sin}(\theta - \frac{2\pi}{3}) & -\text{Sin}(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} \tag{3.31}$$

And the dq0 frame is converted again to Vabc using inverse Park's transformation.

$$\begin{bmatrix} V_a^* \\ V_b^* \\ V_c^* \end{bmatrix} = \begin{bmatrix} \text{Cos}\,\theta & \text{Sin}\,\theta & 1 \\ \text{Cos}(\theta - \frac{2\pi}{3}) & \text{Sin}(\theta - \frac{2\pi}{3}) & 1 \\ \text{Cos}(\theta + \frac{2\pi}{3}) & \text{Sin}(\theta + \frac{2\pi}{3}) & 1 \end{bmatrix} \begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} \tag{3.32}$$

The SRF theory detects supply voltage sags and establishes a reference voltage using transformation equations, which is then compared to a DVR's output voltage using a Hysteresis Voltage Controller. The difference derived from the above must be between the upper (VH) and lower (VL) levels of the hysteresis band for switching less operation, and when it surpasses the lower and upper limits, the difference either reduces or increases. Harmonics and oscillatory voltage components are removed using low-pass filters (LPFs) (Gandhi et al., 2015). Voltage components in the d-and q-axes are:

$$V_{Sd} = V_{dDC} + V_{dAC} \tag{3.33}$$

$$V_{Sq} = V_{qDC} + V_{qAC} \tag{3.34}$$

The voltage quality compensation technique assumes a rated magnitude and distortion-free load terminal voltage.

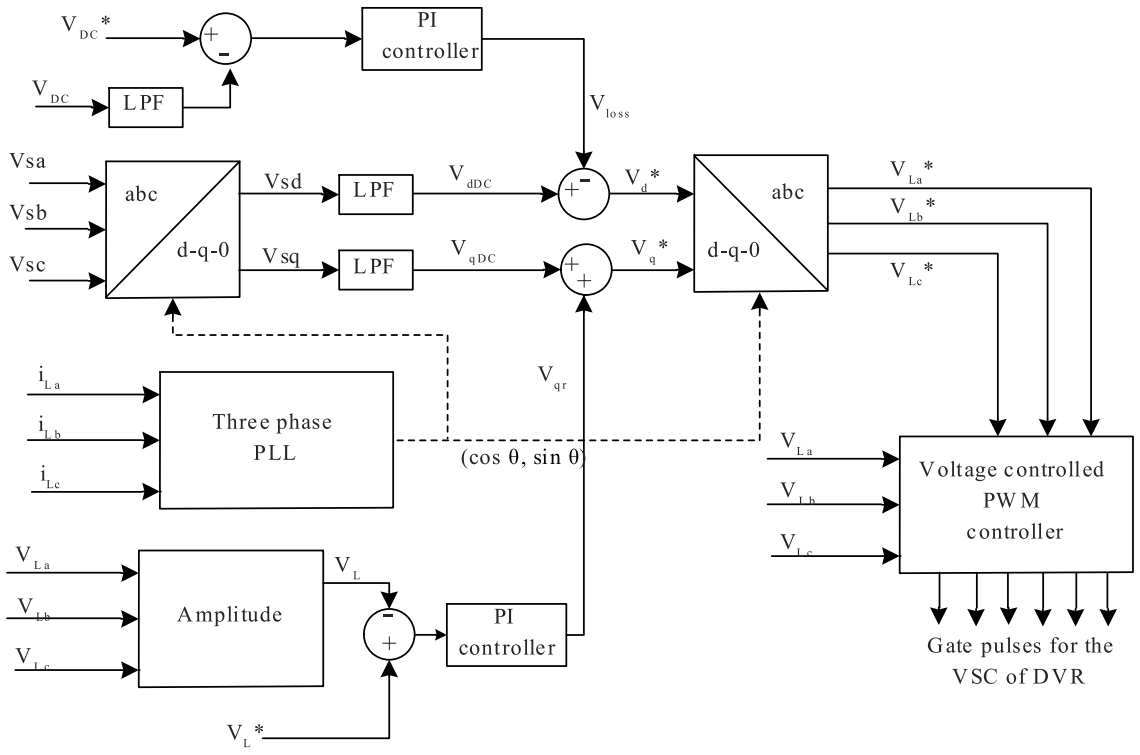


Figure 3.4: Block diagram of SRF theory-based control algorithm for DVR

3.7 Cost Analysis

In modern automated industrial facilities, voltage sags cause annoying process tripping, resulting in significant financial losses for customers. Another power quality issue that leads to production losses is harmonic distortion, which causes sensitive electronics like PCBs and PLCs to malfunction. As a result, both the utility and the customers must be concerned about power quality improvements (Akhtar & Mathew, 2016). The Adama spinning mill contains a variety of delicate equipment, including motors, ASD, and control boards. As a result, assessing the industry's voltage sag and harmonics and attempting to alleviate them in order to improve the production process is critical.

The cost analysis evaluates the proposed CPD's cost effectiveness using standard financial measures such as the payback period. The payback period is the time it takes for a custom power device to pay back its initial cost(El-Gammal et al., 2010). It is necessary to use mitigating devices with a short payback period.

$$Payback\ Period = \frac{\text{Net Investment}}{\text{Net annual Return}} \quad (3.35)$$

The initial cost, which is the total of the cost of mitigation devices plus the cost of installation, is referred to as the net investment. The annual expenses (operation + maintenance) are subtracted from the annual benefit to calculate the net annual return.

The steps for estimating the payback period of the selected mitigation devices are as follows.

1. Estimate the quantity and severity of power quality issues each year.
2. Determine the average cost of a single shutdown.
3. To calculate the annual cost of shutdowns, multiply the result of step (1) by the result of step (2).
4. Obtain the installation, operation, and maintenance costs for the mitigating devices, as well as any technical and economic data that is available.
5. Divide the result of step (4) by the result of step (3) to find the payback period.

In the Adama spinning factory, voltage sag and harmonics cause damage to devices such as motors, inverters, capacitor banks, and so on. Data from the maintenance report and the purchasing department are shown in Table 3.6.

Table 3.6: Maintenance cost of different devices in Adama Spinning Factory

CMDB	Devices	Units	Rating	Maintenance Cost
CMDB-1	Motors	5	1 KW each	12,000
CMDB-2	Motor	1	55 KW	121,000
	Technical Air fan motor	2	18.5 KW each	108,000
	AC Fan Motor	1	4 KW	9,500
		1	5 KW	11,000
CMDB-4	AC Pump Motor	1	11 KW	20,000

	Pump House	2	2.2 KW	9,200
		1	3 KW	7,000
	Fire Fighting Pump Motor	1	55 KW	121,000
	Compressor	2	45 KW	133,000
Total				551,700 ETB

Finance data also shows that after multiple maintenances, different equipment is purchased to replace the destroyed ones.

Air Conditioner fan motors of different rating

- 37 KW Motor……4298 Euro = 232,792.6 ETB
- 30 KW Motors……..2927 Euro = 158,535.1 ETB and 3596 Euro = 194,770.15 ETB.
- 15 KW Motor……...1672 Euro = 90,560.54 ETB

Capacitor Bank

- 20 KVAR…….18,743 ETB
- 10 KVAR…….13,388 ETB

Total cost of maintenance and bought devices = 1,260,489.39 ETB

The factory has lost a significant amount of money as a result of the damaged equipment, such as fluorescent lamps, cables, and other regulating devices, as well as the income paid to employees who are unable to work due to the power quality issue. In the industry, even a short-term power quality problem has a significant impact on the production process.

The amount of money the factory loses as a result of the salary paid to employees without working due to power quality problems, the cost of cables burned and other PCB control boards is assumed to be about 7,600,000 ETB. Therefore, the total loss of the factory in the absence of production becomes 8860489.39 ETB (1,260,489.39 ETB + 7,600,000 ETB).

The mitigating devices used in this study are the DVR and DSTATCOM.

The initial cost for DVR is about 300$/KVA. By assuming maintenance and running cost 5% of initial cost. The power rating of DVR calculated is about 182. 28 KVA and 260.03 KVA for CMDB-2 and CMDB-4 respectively. By taking the standard rating of 200 KVA and 300 KVA:

- For CMDB-2

  Cost of DVR = 300$/KVA*200 KVA + 5% (300$/KVA *200 KVA) = 63,000 $

- For CMDB-4

  Cost of DVR = 300$/KVA*300 KVA + 5% (300$/KVA*300KVA) = 94,500 $.

Then total cost of DVR becomes (63,000 + 94,500) $ = 157500 $ = 8,190,000 ETB.

The initial cost of DSTATCOM of 400V voltage is about 150,000 $. Since two DSTATCOM are proposed in this study, the total cost is 300,000 $.

- For DSTATCOM

  Total cost = 300,000 $ = 15,600,000 ETB.

As a result, the total cost of mitigating devices becomes 23790000 ETB.

Therefore, the payback period of the proposed mitigating devices can be found using equation (3.35).

$$PBP = \frac{23790000}{8860489.39} = 2.68 years$$

CHAPTER FOUR

RESULTS AND DISCUSSIONS

4.1 Overall Model of Adama Spinning Factory Distribution Network

As stated in Chapter 3, the Adama spinning plant is supplied by the Adama substation, and the 15KV line enters a powerhouse. The voltage in this powerhouse is stepped down to 400V by four step-down distribution transformers. The distribution board distributes power to various loads. The system's parameters and loads are determined mathematically, and the overall distribution network of the industry is represented in MATLAB/SIMULINK. Figure 4.1 illustrates the industry's electrical distribution network without the compensating device.

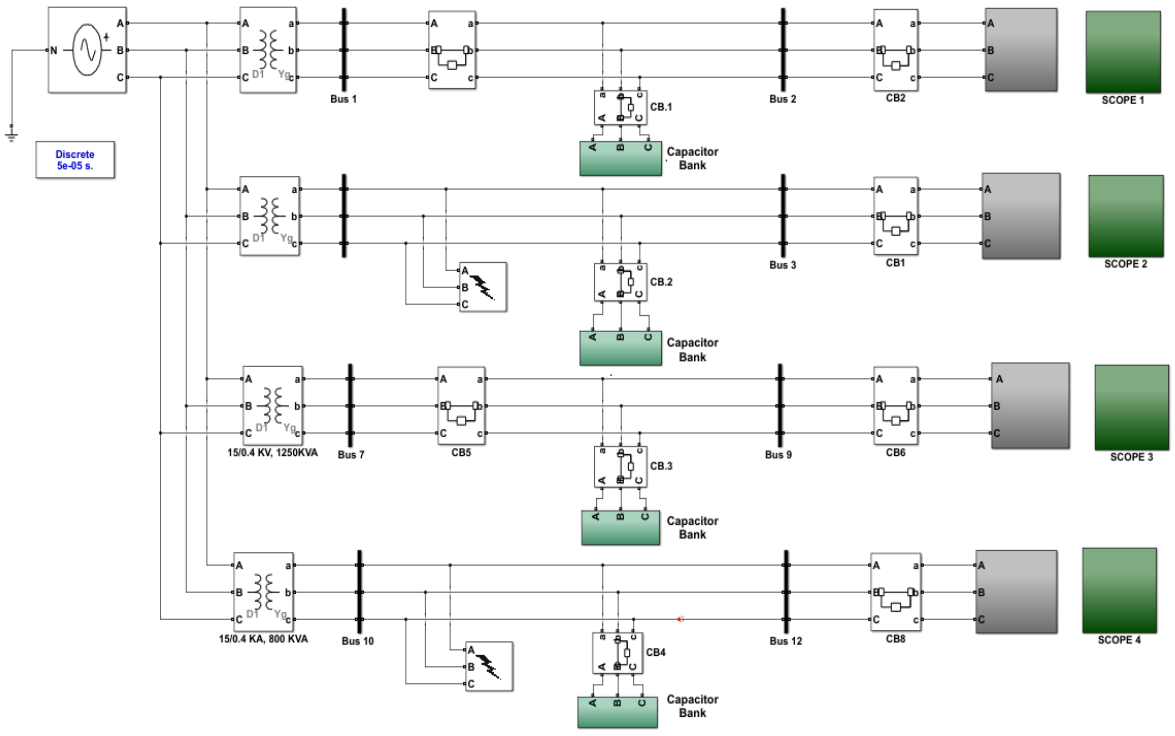


Figure 4.1: SIMULINK Model of Adama Spinning Factory Distribution Network

According to the primary and secondary data acquired, the power quality problem, particularly current harmonics, and voltage sag, exists in the Adama spinning factory electrical distribution network. As a result, the modeled network was simulated to assess the severity of the identified

issue as well as the distribution network's performance with and without the mitigating device was integrated. The next sub-sections go through this in further details.

4.2 Simulation Results Without Mitigating Devices

Power quality issues, notably current harmonics, exist in the CMDB-1 and CMDB-3 due to the numerous nonlinear loads on these boards. These loads are represented as three-phase rectifiers in parallel with linear loads for simulation purposes. On the other hand, there is voltage sag on the network's CMDB-2 and CMDB-4 as a result of several short circuits on this distribution boards. The simulation is performed for different types of faults such as symmetrical and unsymmetrical faults.

4.2.1 For CMDB-1

According to the study, the current harmonics exist under this distribution board since there are several Adjustable Speed Derives (ASDs) for controlling motor speed. Figure 4.2 shows the CMDB-1's simulation result for current without the use of any compensating techniques.

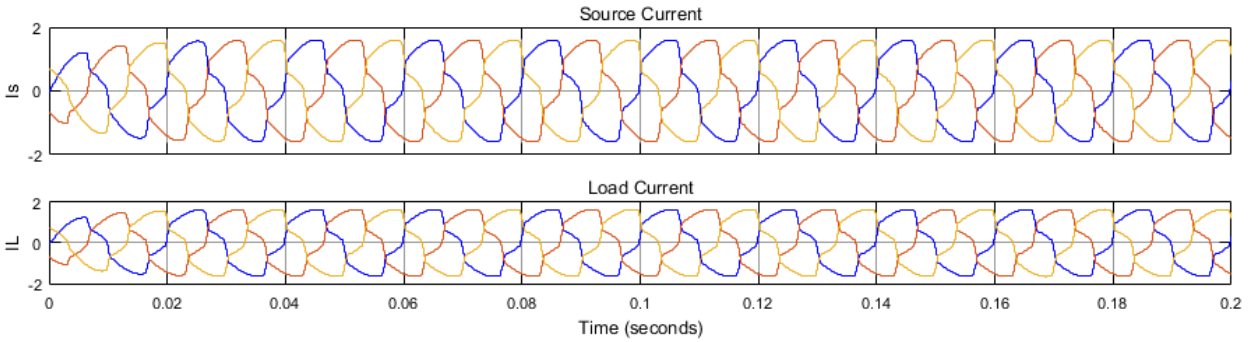
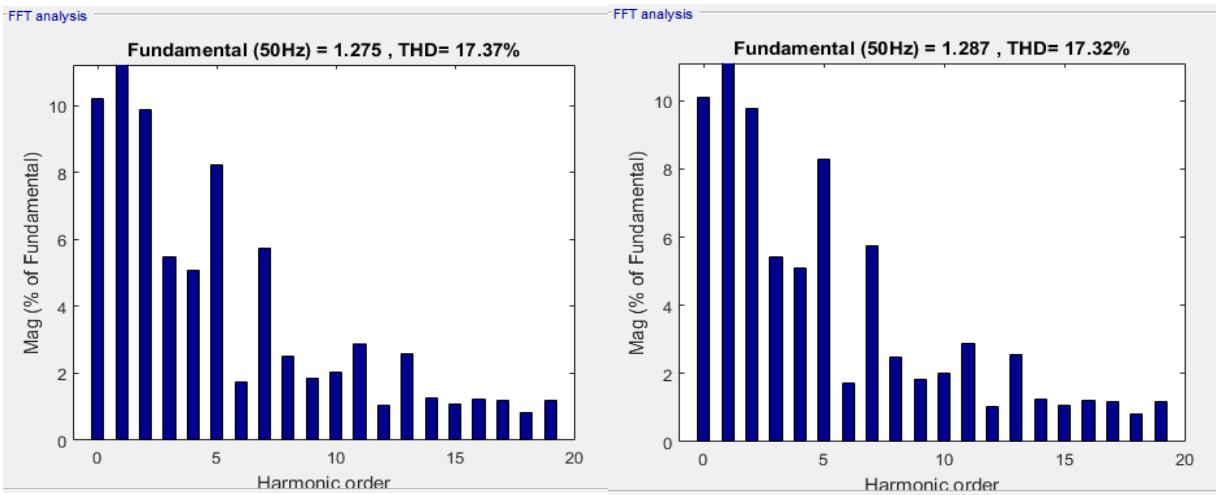


Figure 4.2: Current Waveform of CMDB-1 Without DSTATCOM

Nonlinear loads draw current in short, sharp pulses, as shown in figure 4.2. These pulses distort load current waveforms, causing harmonics that can create power problems for both distribution system equipment and loads connected to it. When there are harmonics in the network, the loads demand more reactive power. This causes a reduction in power factor. Furthermore, as can be seen from the result, the source current has also been interrupted due to the return of the distorted current to the source from the load. In Figure 4.3, the Total Harmonic Distortion of Current (THD_I) is illustrated for both load and source current.



a) b)

Figure 4.3: Harmonic Spectrum for a) Source Current b) Load Current of CMDB-1

The load and source currents are distorted as a result of the nonlinear loads in the system, as demonstrated by the harmonic spectrum. In addition to this, since the THD value exceeds the permitted current harmonics limit, the factory will be penalized for a low power factor.

4.2.2 For CMDB-2

Voltage sag is a power quality problem occurring on CMDB-2 many times throughout the year from the analysis performed. A three-phase fault has been applied to this board to demonstrate it via simulation. As a result, voltage sag under different fault scenarios is modeled and investigated in this study.

Case 1: Symmetrical Fault

A symmetrical fault affects all phases of the voltage in the same proportion, keeping the system balanced. A short-circuit fault is an example of this type of fault, which results in a voltage drop of the same magnitude in all phases. Figure 4.4 shows the system's performance during a symmetrical fault. The voltage sag occurs from 0.2 to 0.38 seconds for 0.18 seconds.

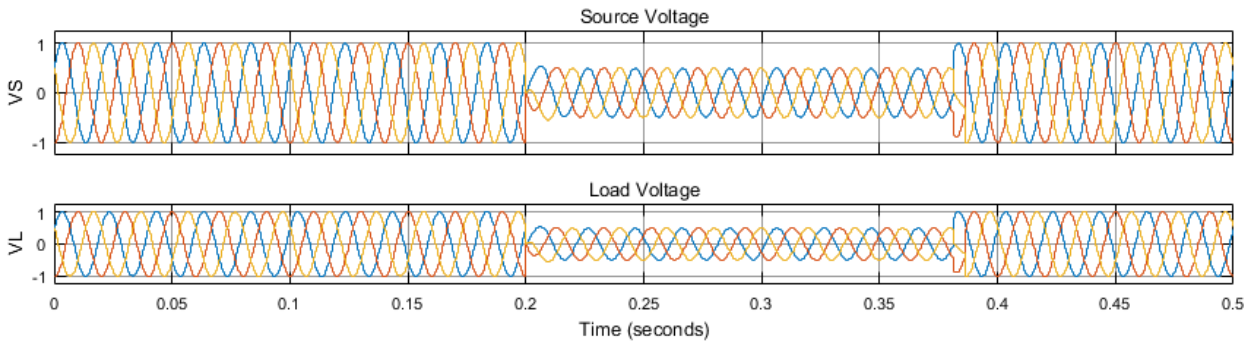
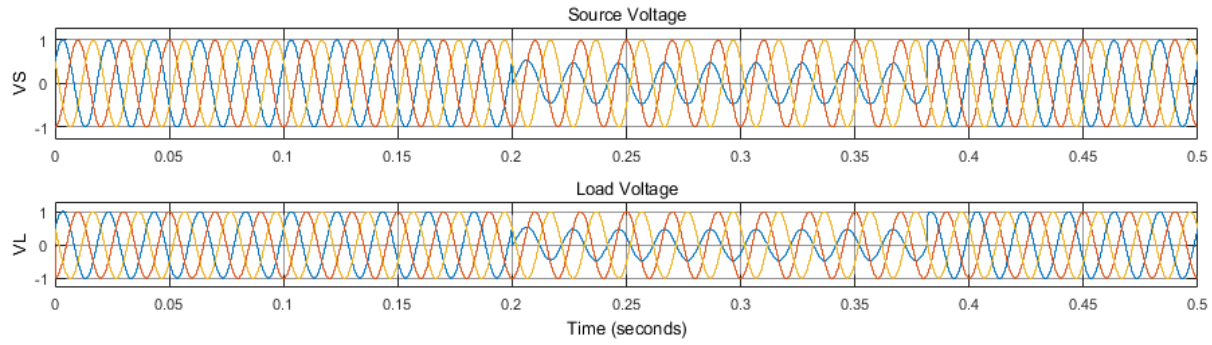


Figure 4.4: Voltage sag when a symmetrical fault occurs on CMDB-2

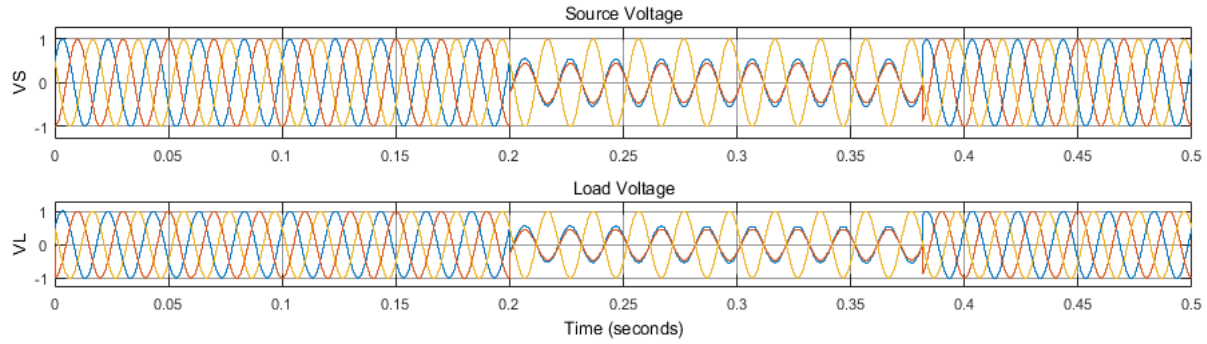
When a three-phase fault occurs in the network, all three phases of the voltage are short-circuited, and the voltage magnitude is reduced. Because motors and other sensitive devices can't operate under the voltage level they require, this situation is dangerous. That is, if the circuit breaker does not trip abruptly, it may result in serious damage to these devices.

Case 2: Unsymmetrical Faults

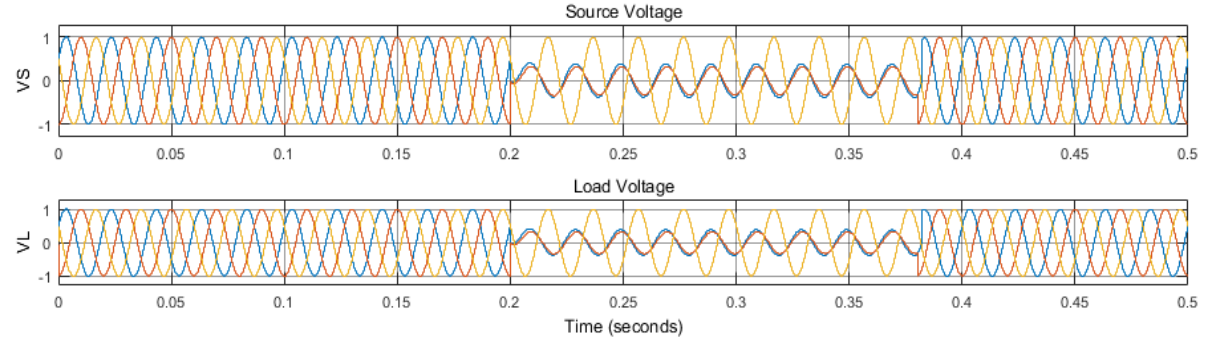
Unsymmetrical faults are those faults that have unbalanced magnitude and unequal phase shifts. Line-to-ground, line-to-line, and double line-to-ground faults are the three types of these faults. The CMDB-2 is simulated in the presence of these unsymmetrical faults in order to assess the system's performance during their occurrence.



a)



b)



c)

Figure 4.5: Voltage Waveform of CMDB-2 for a) Line to ground b) Line to Line c) Double Line to Ground without DVR

The voltage waveform for different types of unsymmetrical faults has been shown in figure 4.5. Different unsymmetrical faults in the electrical distribution network influence the operation of the induction motors and other loads connected to these faulted lines. The electrical torque and motor speed were reduced as a result of the voltage sags caused by the fault. Furthermore, a significant voltage reduction causes the motor to slow down to the point of stopping. As a result, in order for the machines to operate efficiently, the voltage sag caused by various fault types must be compensated.

4.2.3 For CMDB-3

As previously indicated, CMDB-3 is one of the distribution boards that is having power quality issues. According to the collected data, the numerical analysis undertaken shows that this board has a current harmonics problem. The existence of various Adjustable Speed Drives, similar to

CMDB-1, is the main cause of these harmonics. The current distortion waveform generated by nonlinear loads is shown in Figure 4.6.

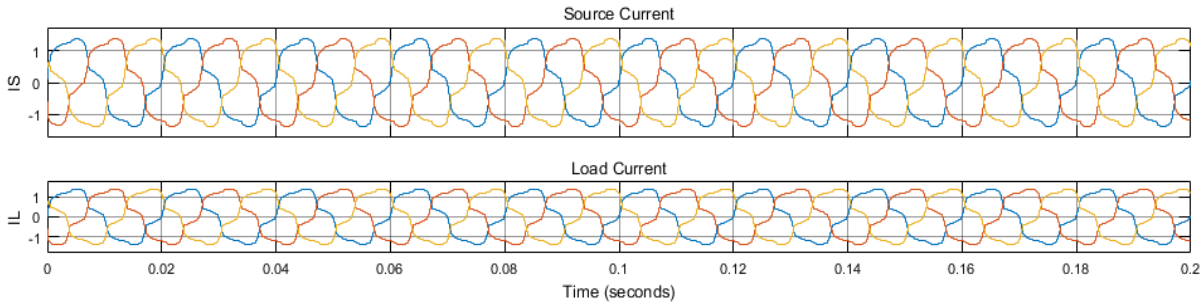
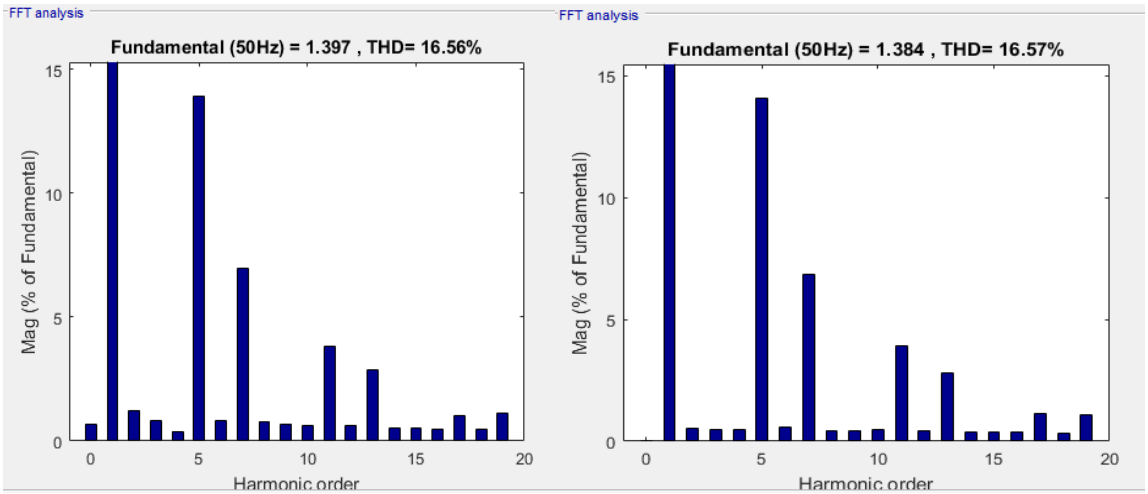


Figure 4.6: Current Waveform of CMDB-3 without DSTATCOM

As seen in figure 4.6, the load current is distorted due to the presence of these nonlinear loads, resulting in source current distortion. The THD_I is shown in figure 4.7 to analyze their distortion level.



a) b)

Figure 4.7: Harmonic Spectrum for a) Source Current b) Load Current

The harmonic spectrum in the above figure 4.7 shows that the current harmonics is existing on this board since the THD_I is above the IEEE standard limit. So, the mitigating device is needed for this distribution board like that of CMDB-1.

4.2.4 For CMDB-4

The investigation performed shows that voltage sag is existing on CMDB-4 and due to this problem, a lot of devices have been damaged. In this study, a three-phase fault is applied to this board for different fault conditions. The fault is applied from 0.15 sec to 0.32 sec i.e., for 0.17 sec.

Case 1: Symmetrical Fault

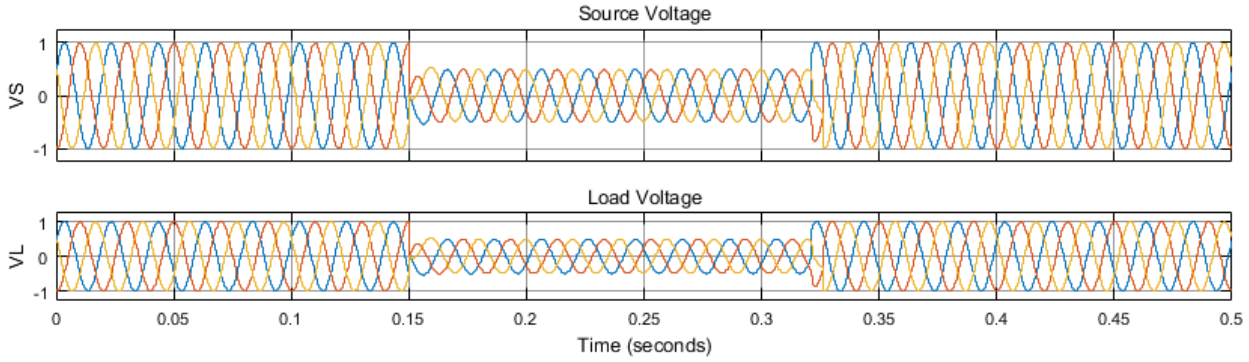
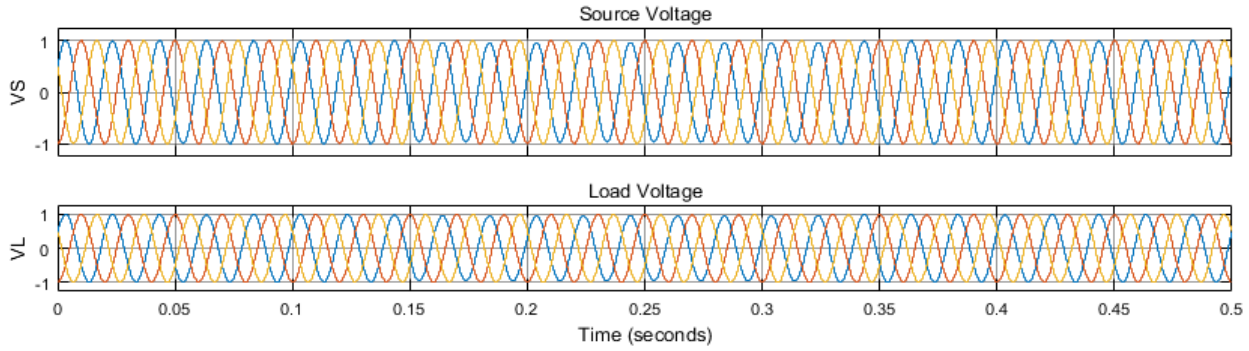
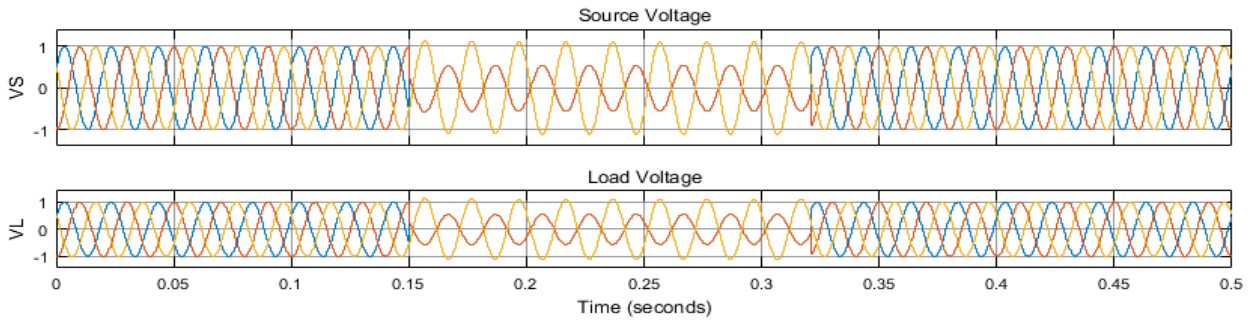


Figure 4.8: Voltage Waveform of CMDB-4 under Symmetrical fault without DVR

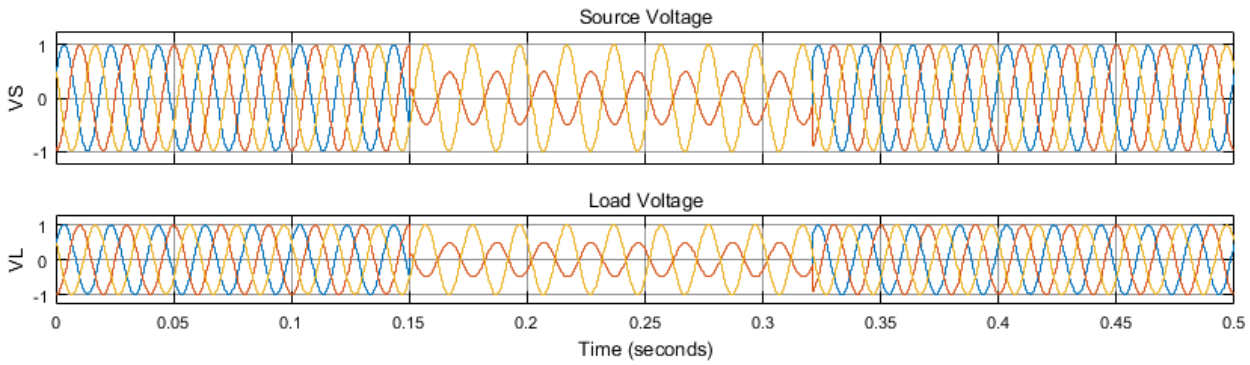
Case 2: Unsymmetrical Faults



a)



b)



c)

Figure 4.9: Voltage Waveform of CMDB-4 under a) Line to ground fault b) Line to Line fault c) Double Line to Ground fault without DVR.

4.3 Simulation Results with the Proposed Mitigating Devices

As shown in the above simulation results, without compensating devices, current harmonics and voltage sag exist in the Adama spinning factory. Current harmonics and voltage sag are compensated using DSTATCOM and DVR, respectively. In other words, the DSTATCOM is used to tackle current-related power quality problems, whereas the DVR is used to fix voltage-related ones. The distribution networks are simulated together with the proposed mitigating devices. Figure 4.10 shows the MATLAB/SIMULINK model of the distribution network with the mitigating device.

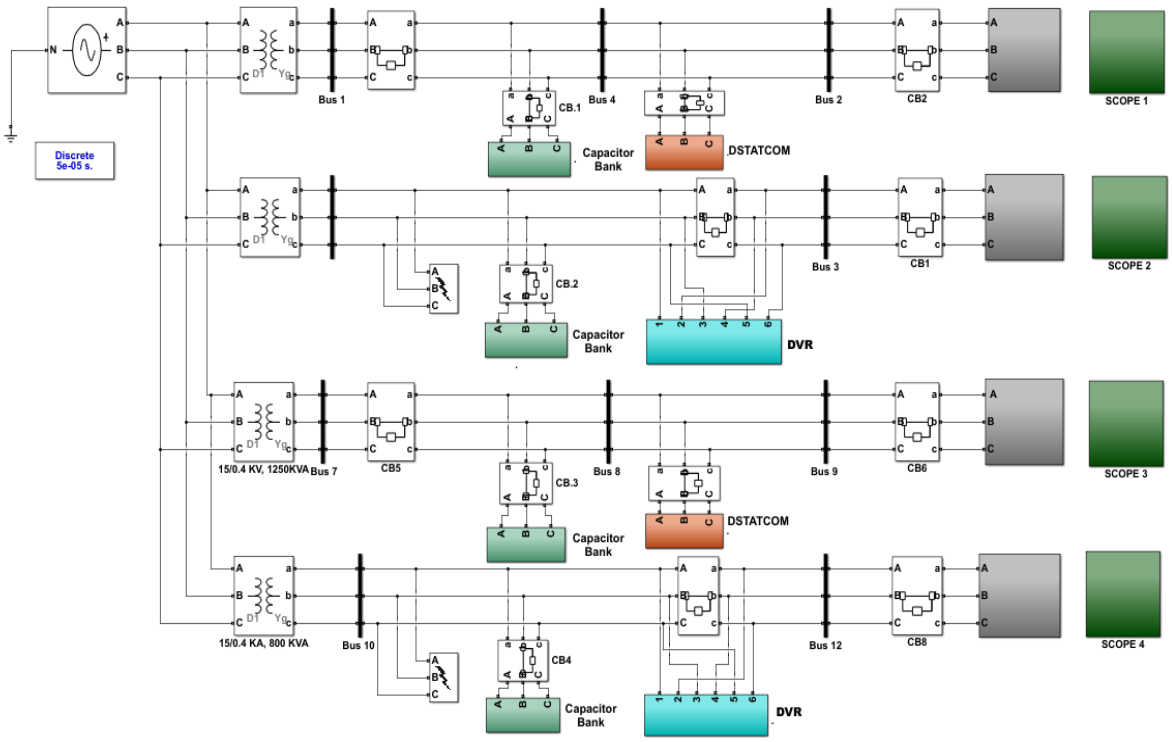


Figure 4.10: SIMULINK Model of Adama Spinning Factory with Mitigating Devices

The control algorithm used for gate pulse generation is synchronous reference frame theory for both mitigating devices. The modeled control theory is shown for DSTATCOM as in figure 4.11 below.

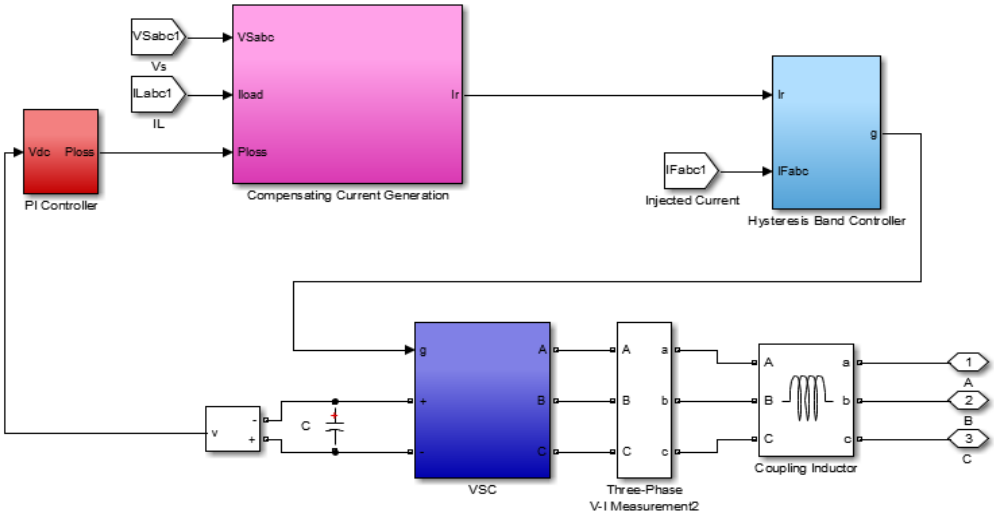


Figure 4.11: MATLAB/SIMULINK Model for DSTATCOM

In the above model, the PI controller is utilized to control the DC bus voltage using the reference voltage V_{DC}* and the measured voltage V_{DC}. The Discrete PI controller from SIMULINK's Simscape power system toolbox, with proportional gain KP=1000 and integral gain KI=50, is used to regulate this DC voltage across the capacitor, as shown in the DSTATCOM block diagram in figure 4.11. The manual tuning approach is used to select the gains. Figure 4.12 illustrates the SRF which is used to control DSTATCOM.

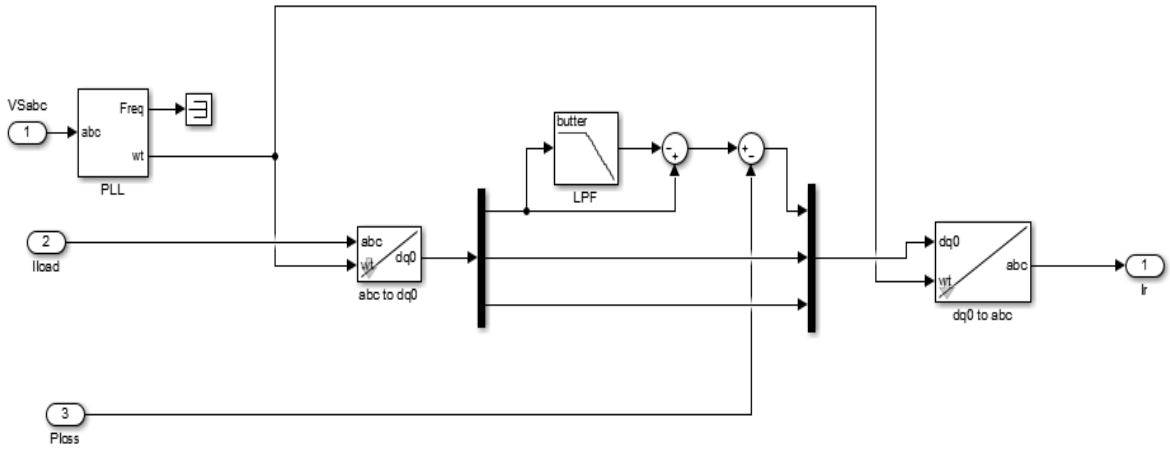


Figure 4.12: MATLAB/SIMULINK Model for SRF theory

In this control technique, the source voltage (Vs), load current (IL), and DC voltage (VDC) are detected as feedback. The measured load currents are then compared to the references using hysteresis comparators, as shown in figure 4.13. Each comparator determines the switching state of the corresponding inverter leg (Sa, Sb, and Sc) in order to keep the load currents within the hysteresis band (Nachiappan et al., 2012).

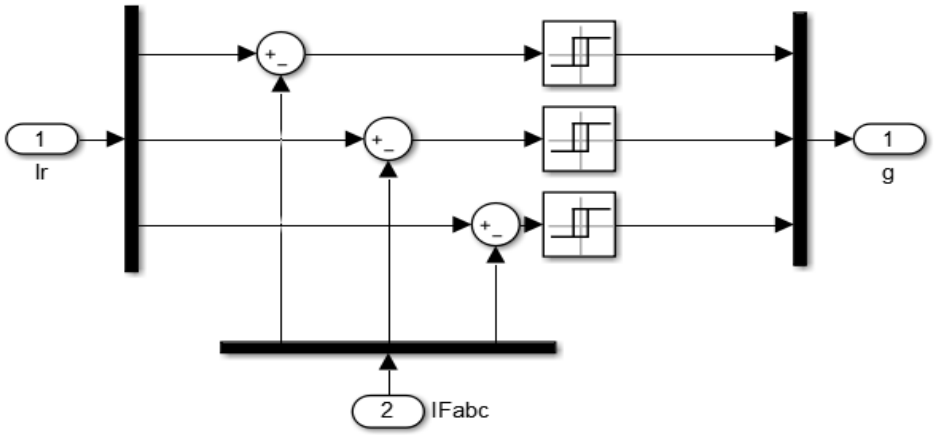


Figure 4.13: MATLAB/SIMULINK of Hysteresis Current Controller

Dynamic Voltage Restorer (DVR) is modeled in this study for voltage sag mitigation on the specified Central Main Distribution Boards i.e. CMDB-2 and CMDB-4. Its Simulink model is shown as in figure 4.14 below.

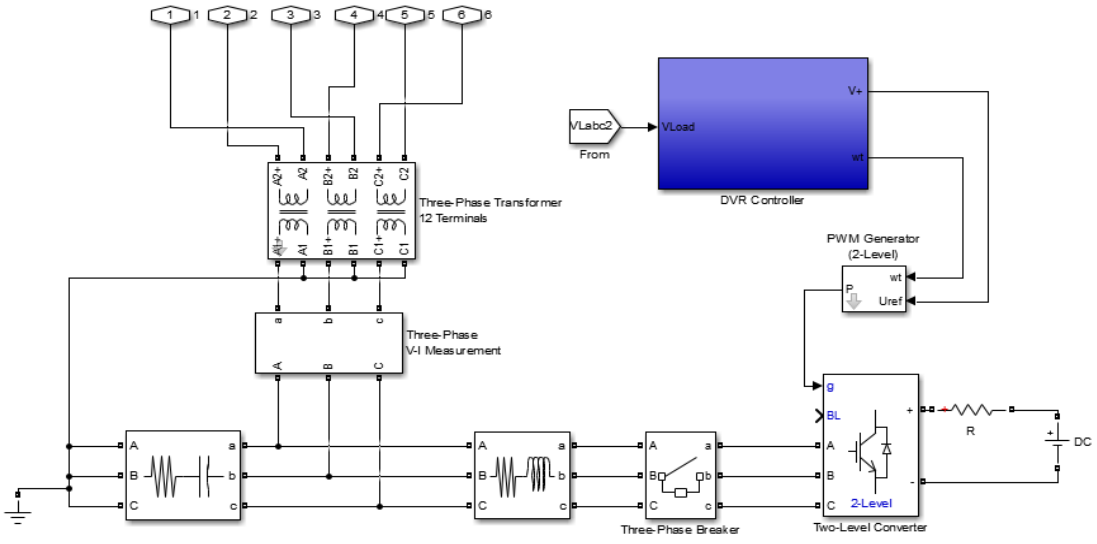


Figure 4.14: MATLAB/SIMULINK Model for DVR

In this study, the DSTATCOM is connected to CMDB-1 and CMDB-3 since current harmonics are detected on these boards from the analysis undertaken. Also, the investigation demonstrates that the voltage sag is occurring frequently on CMDB-2 and CMDB-4. As a result, DVR is integrated into these distribution boards to mitigate it.

4.3.1 For CMDB-1

On this distribution board, DSTATCOM is employed to minimize current harmonics caused by nonlinear loads. The current waveform and its harmonic spectrum with this compensating device are shown in figures 4.15 and 4.16, respectively.

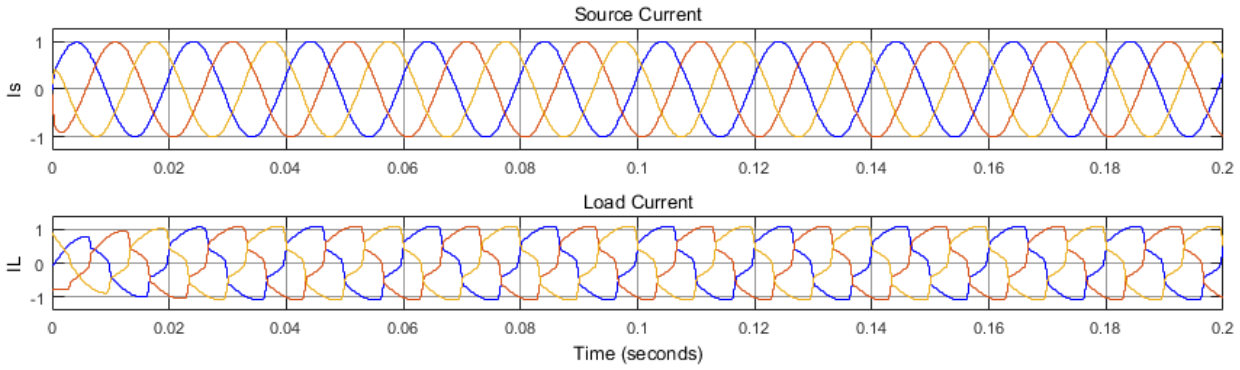
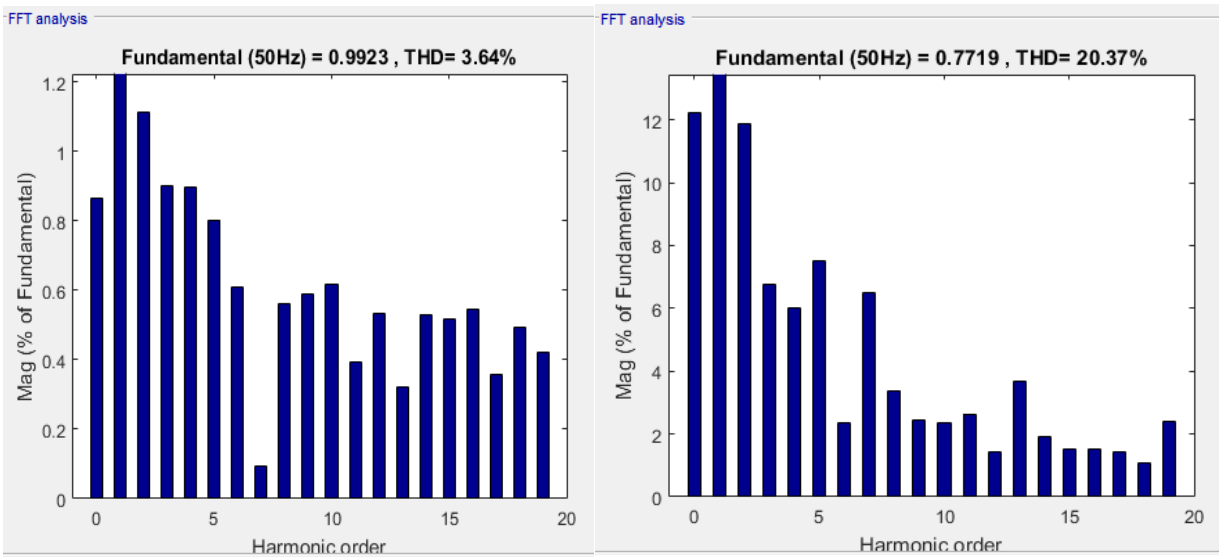


Figure 4.15: Current Waveform of CMDB-1 with DSTATCOM



a) b)

Figure 4.16: Harmonic Spectrum of a) Source current b) Load Current of CMDB-1 with DSTATCOM

The source current waveform becomes pure sinusoidal after the DSTATCOM is integrated into the system, according to simulation results shown in figure 4.15. The THD_I level also drops to 3.64%, which is substantially within the IEEE-recommended limits.

4.3.2 For CMDB-2

A DVR is utilized to ensure the voltage delivered to the loads is free from voltage sag. In this section, this distribution board is simulated with DVR to observe the performance of the selected custom power device during different fault conditions.

Case 1: Symmetrical Fault

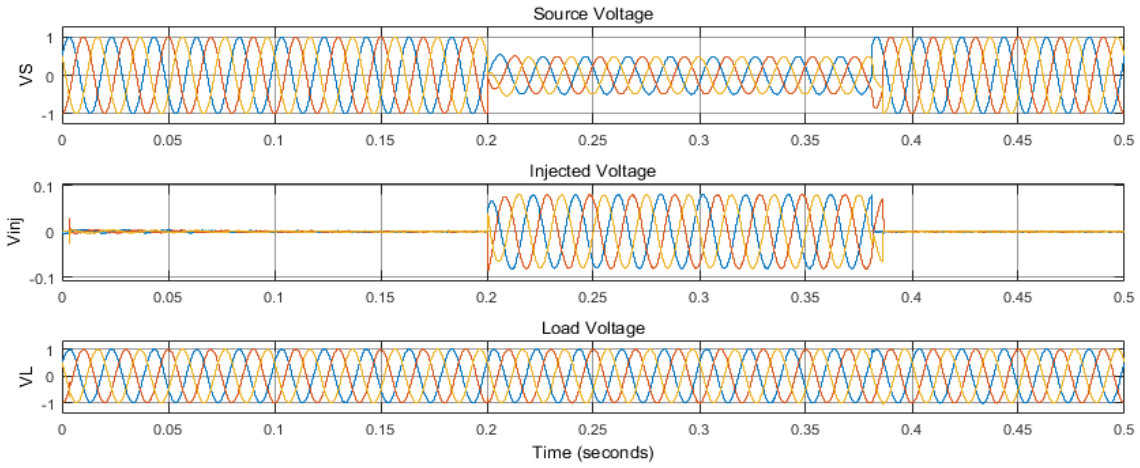
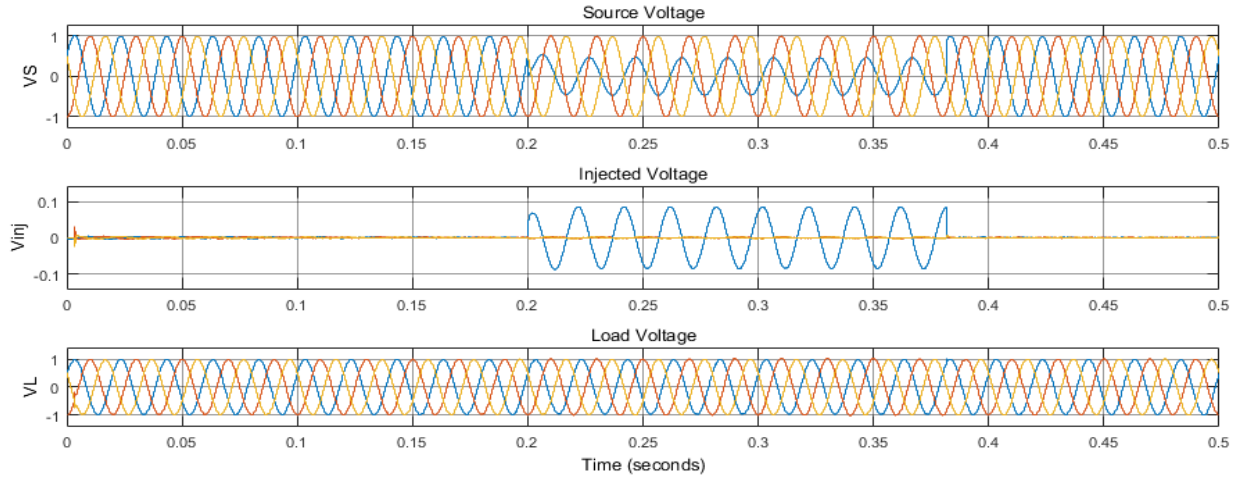


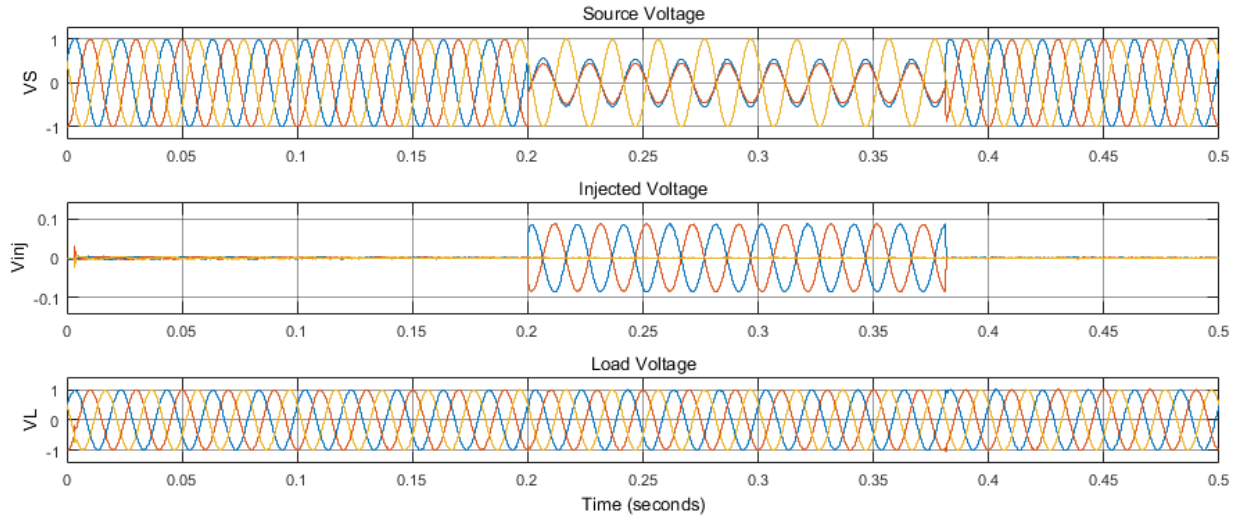
Figure 4.17: Voltage Waveform of CMDB-2 under symmetrical fault with DVR

Case 2: Unsymmetrical Faults

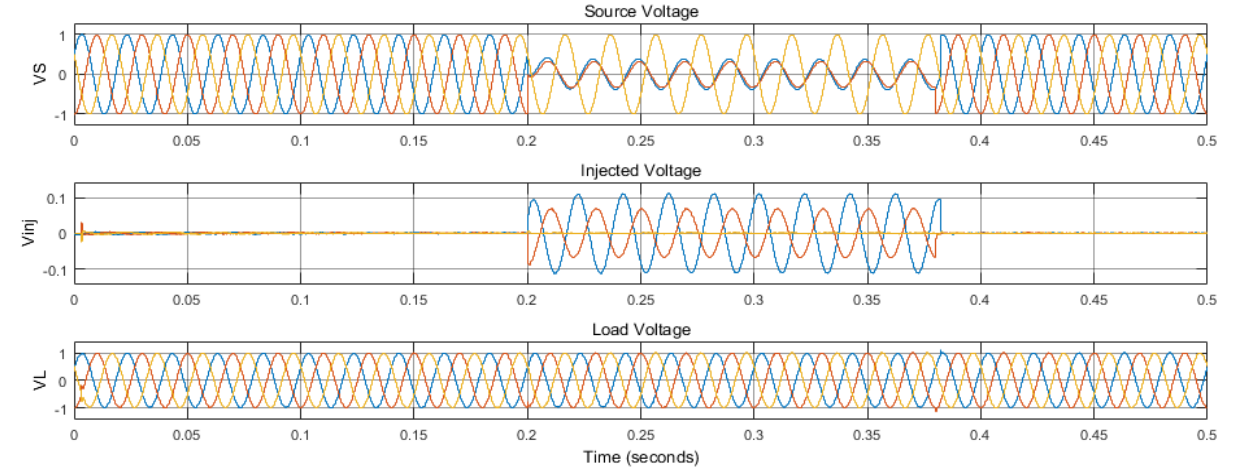
With the DVR connected to the network, the distribution network is simulated for CMDB-2 with unsymmetrical faults such as line to ground, line to line, and double line to ground. Below are the voltage waveforms obtained after compensation.



a)



b)



c)

Figure 4.18: Voltage Waveform with DVR for a) Line to Ground Fault b) Line to Line Fault c) Double Line to Ground Fault

As seen in the above simulation results, voltage sag exists in the CMDB-2 of Adama spinning factory distribution network due to various faults. However, this problem will no longer be an issue when the DVR is connected to the network. This means that even if a fault occurs, the proposed custom power device compensates for the load voltage to protect heavy loads such as motors and printed electrical boards.

4.3.3 For CMDB-3

The DSTATCOM is connected to this board to compensate for the existing harmonics issue. The current waveform and harmonic spectrum after DSTATCOM integration are shown in Figures 4.19 and 4.20, respectively.

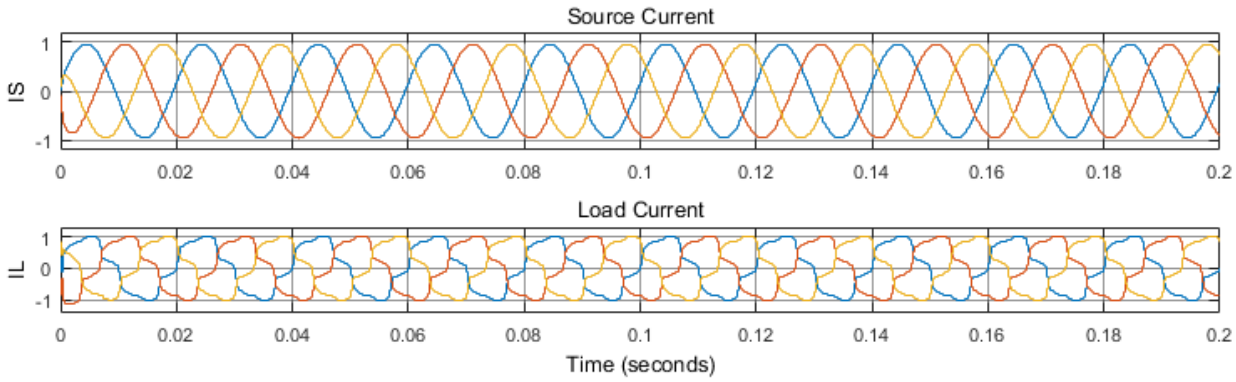


Figure 4.19: Current Waveform of CMDB-3 with DSTATCOM

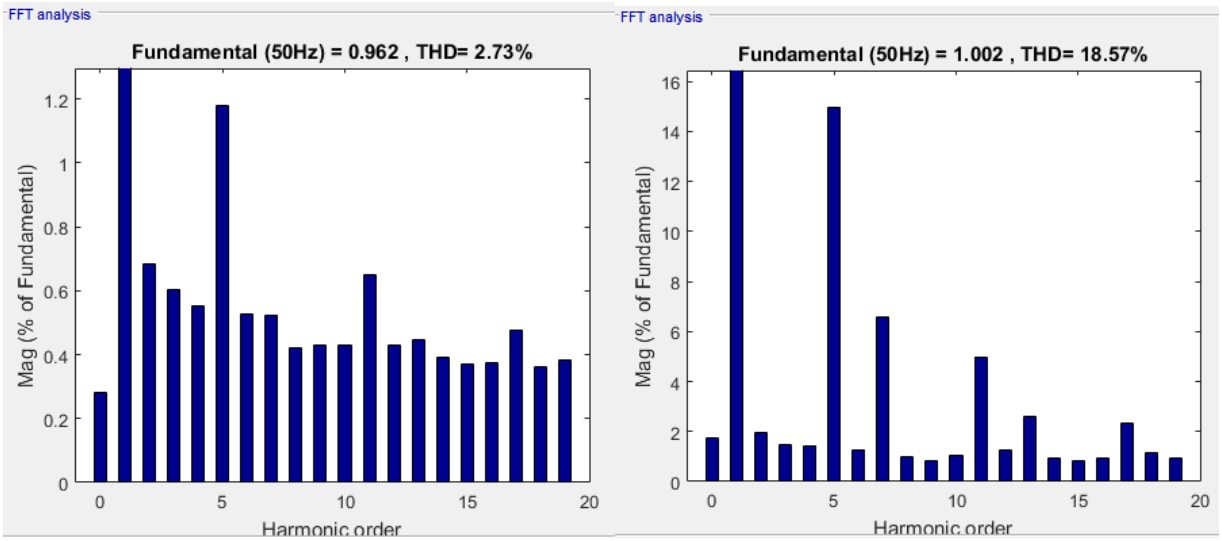


Figure 4.20: Harmonic Spectrum of Current for CMDB-3 with DSTATCOM

The DSTATCOM compensates for harmonic current created by nonlinear loads, as shown in the above simulation for CMDB-3. Even though the load current is distorted due to these loads, the source current becomes pure sinusoidal, and THD_I is 2.73, which is below the IEEE standard limit.

4.3.4 For CMDB-4

To compensate for the voltage sag problem, the DVR is integrated with this CMDB. Because several motors used for various purposes, particularly for water pumping, are regularly burned under this board, the plant has lost money as a result of this power quality issue.

Case 1: Symmetrical Fault

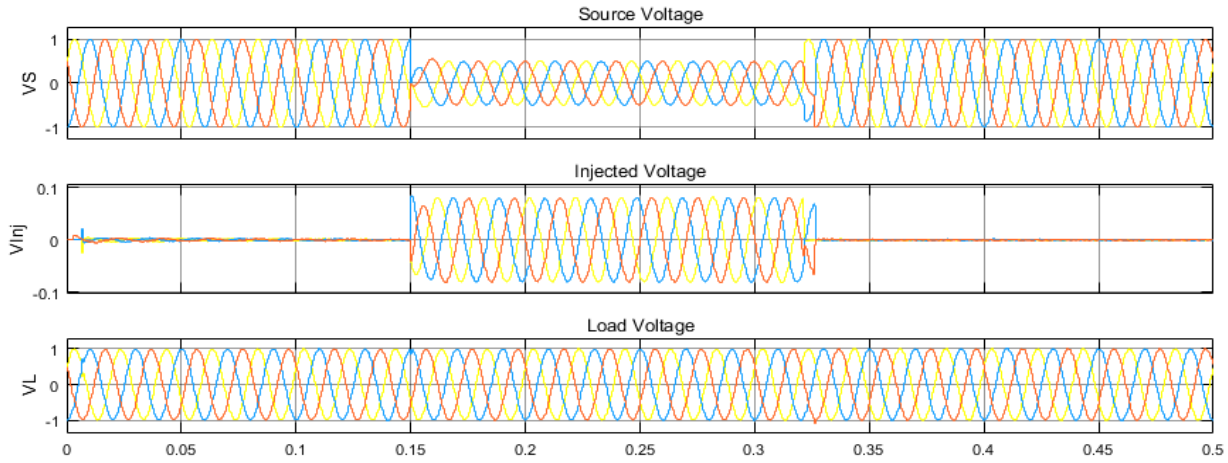
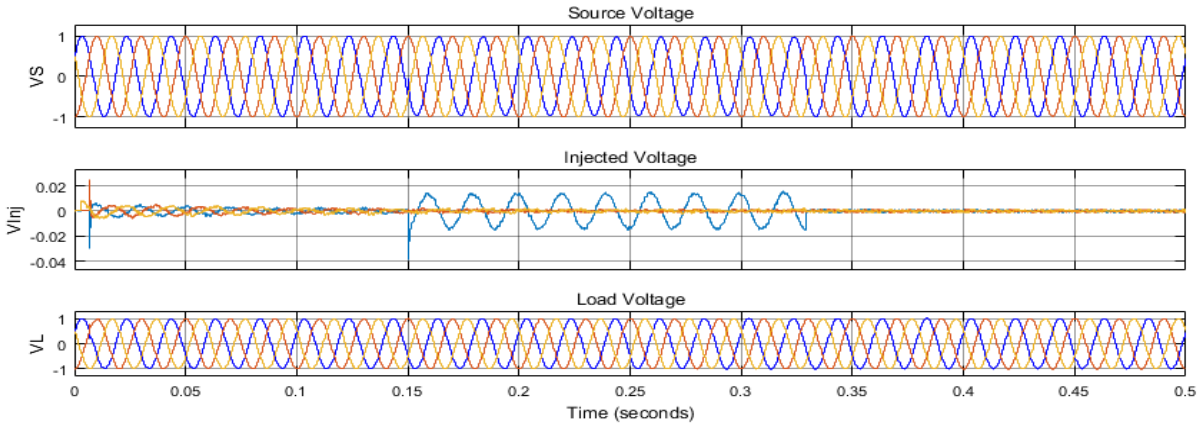
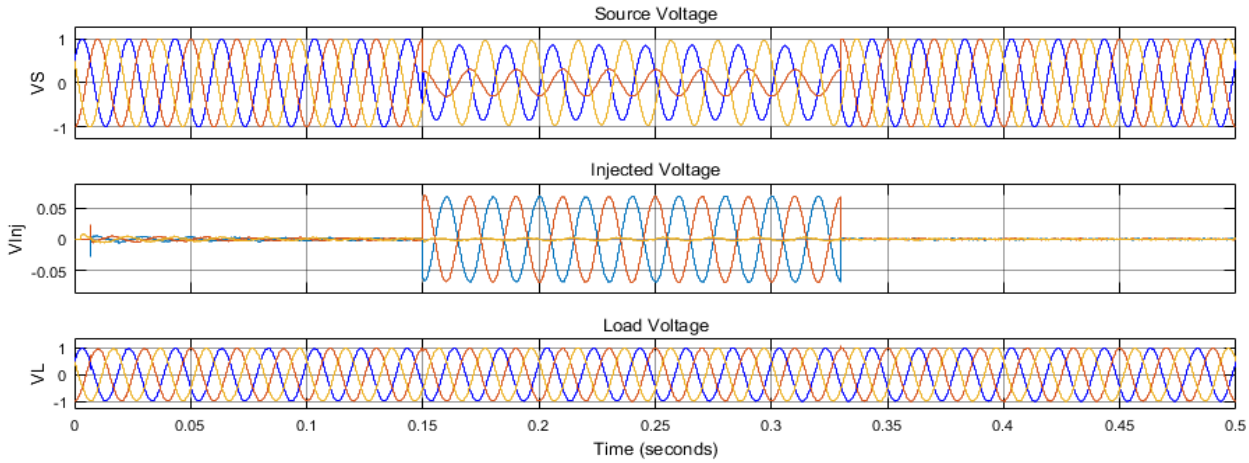


Figure 4.21: Voltage Waveform of CMDB-4 with DVR

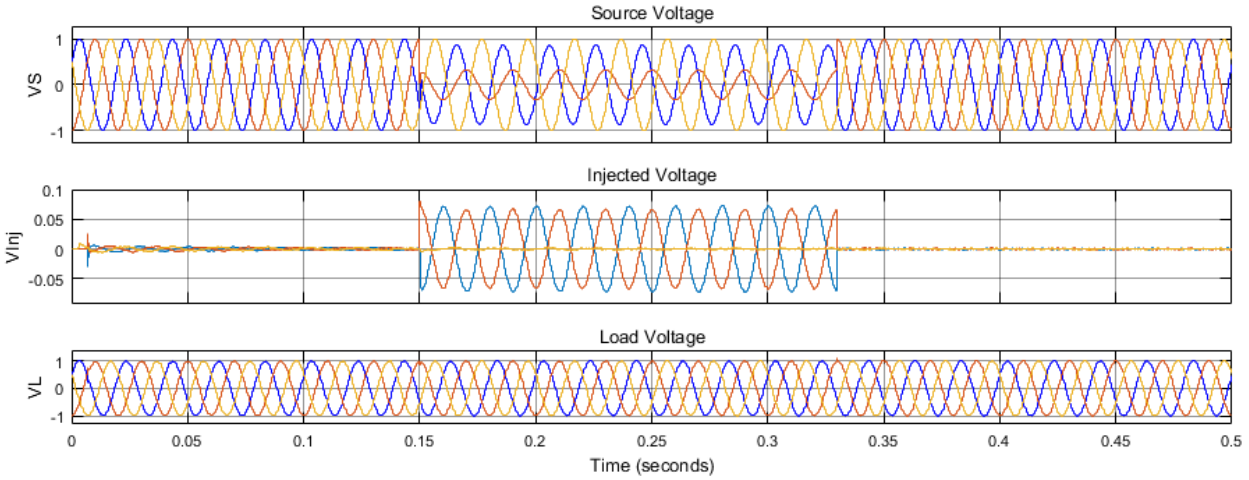
Case 2: Unsymmetrical Faults



a)



b)



c)

Figure 4.22: Voltage Waveform of CMDB-4 for a) Line to Ground Fault b) Line to Line Fault c) Double Line to Ground Fault with DVR

It has been shown that the voltage sag occurs on the source voltage based on the CMDB-4 simulation results. The load voltage is compensated when the DVR injects voltage during the sag duration.

4.4 Discussions

The Adama Spinning Factory distribution network is modelled and simulated with MATLAB/SIMULINK. The factory's distribution system is modeled as a balanced three-phase pure sinusoidal voltage supply with linear and non-linear loads. The linear loads are defined by active and reactive power of a series RL load when the real power factor of the loads is taken into account. Three-phase rectifier with RL loads is used to simulate nonlinear loads. Finally, the modeled distribution network is simulated both with and without mitigating devices integrated.

According to the simulation results obtained from CMDB-1 and CMDB-3, the waveform of source current become pure sinusoidal once the DSTATCOM is integrated to the system. The THD_I level also falls below the IEEE standard limit, as shown by the harmonic spectrum. As a result, the proposed DSTATCOM is capable of compensating for existing harmonic distortion in the system.

On the other hand, the CMDB-2 and CMDB-4 simulation results indicate that the suggested DVR can mitigate voltage sag on this distribution boards. Table 4.1 compares source current total harmonic distortion with and without a compensating device.

Table 4.1: Comparison of THD_I with and without DSTATCOM

CMDB	THD_I Without DSTATCOM	THD_I with DSTATCOM
CMDB-1	17.37%	3.64%
CMDB-2	0.1%	0.1%
CMDB-3	16.56%	2.73%
CMDB-4	0.48%	0.48%

The power factor of CMDB-1 and CMDB-3 is reduced due to the current harmonics existing on these boards. But after DSTATCOM is integrated into them, the power factor is improved. The following table 4.2 illustrates this.

Table 4.2: Power factor Comparison without and with DSTATCOM

CMDB	pf without DSTATCOM	pf with DSTATCOM
CMDB-1	0.78	0.91
CMDB-2	0.85	0.85
CMDB-3	0.75	0.88
CMDB-4	0.9	0.9

The voltage harmonic distortion is within the IEEE standard limit for all Central Main Distribution Boards (CMDBs), according to the numerical analysis and simulation results. The following table 4.3 shows the Total Voltage Harmonic Distortion with and without a mitigating device.

Table 4.3: Voltage Harmonic Distortion with and without DSTATCOM.

CMDB	THD_V without DSTATCOM	THD_V with DSTATCOM
CMDB-1	1.92%	1.92%
CMDB-2	0.05%	0.05%
CMDB-3	5.7%	5.7%
CMDB-4	7.27%	7.27%

Voltage sag is observed in CMDB-2 and CMDB-4 based on the information gathered and data manually recorded. Three phase fault is connected to these boards in order to investigate this power quality issue and propose a solution. The voltage sag has been mitigated after integrating DVR with the prescribed CMDBs, and the load voltage magnitude during sag has been 1pu even when the source voltage is reduced. The load voltage with and without the mitigating device is illustrated in the following table 4.4.

Table 4.4: Comparison of Load Voltage During Voltage Sag with and without DVR

CMDB	Voltage Magnitude without DVR	Voltage Magnitude With DVR
CMDB-1	1 pu	1 pu
CMDB-2	0.5 pu	1 pu
CMDB-3	1 pu	1pu
CMDB-4	0.5 pu	1 pu

CHAPTER FIVE

CONCLUSIONS, RECOMMENDATIONS, AND FUTURE WORKS

5.1 Conclusions

In this study, harmonic distortion and voltage sag problems are investigated and their proper mitigation techniques have been proposed for Adama Spinning Factory distribution networks. The data were obtained through direct measurement and a review of the factory's documents. Current harmonics occur on distribution networks CMDB-1 and CMDB-3, according to the numerical analysis and simulation of the distribution network. This is due to the fact that under those distribution boards there are a lot of ASD than others. According to the investigation's results, all of the distribution boards are free of voltage harmonics since their voltage harmonic distortion is substantially below the IEEE standard limit. Voltage sag is another power quality issue discovered on distribution boards CMDB-2 and CMDB-4.

Then DSTATCOM and DVR are proposed and modeled in the MATLAB/SIMULINK environment to mitigate current harmonics and voltage sag, respectively. The synchronous reference frame (SRF) control technique is used to generate the gating pulse of the voltage source converter (VSC). The distribution system's performance was then compared without and with the mitigating devices.

The simulation results show that the suggested DSTATCOM compensated for the current harmonics on CMDB-1 and CMDB-3. As a result, with DSTATCOM integrated into the distribution network, the source current becomes pure sinusoidal. As a result, the proposed DSTATCOM can be concluded to be capable of compensating current harmonics. On the other hand, the simulation results for CMDB-2 and CMDB-4 with the DVR, show that the load voltage remains constant at 1 pu even when the source voltage is lowered due to various fault conditions.

5.2 Recommendations

Power quality problems especially harmonic distortion and voltage sag have been investigated and their proper mitigation technique has been proposed in this thesis work. The DELAB NV8s PFC was used to collect the harmonic distortion data. This device can only measure harmonic distortions and it is not capable of storing data and showing waveforms. Therefore, it is highly

recommended for the factory to use a power quality analyzer such as FLUKE 435 to measure the harmonic distortion and other power quality problems. Also, the workers must record the voltage sag occurrence of all the distribution boards manually to demonstrate the frequency level of this problem. Even though the factory is using a capacitor bank for power factor correction, the power factor is below the allowable value on some of the distribution boards. Therefore, this capacitor bank should be replaced by DSTATCOM for avoiding this current harmonic problem and for better improvement of power factor. Voltage sag is also a concern at this factory. This is because the voltage provided by the substation can occasionally go below the permitted voltage limit, as well as because faults can occur. If not addressed in a timely manner, manufacturing devices such as motors will malfunction, potentially resulting in severe damage. As a result, it is strongly recommended that the factory use DVR to compensate for the voltage sag so that it can operate efficiently.

5.3 Future Works

This study focuses on the investigation of power quality problems particularly harmonics and voltage sag and with their mitigation technique. Even if these problems are the dominating, there might be also other power quality problems in this factory.

The problems that need to be studied further are listed below.

- The investigation of various power quality issues, such as transient, and the techniques used to mitigate them.
- Reliability analysis for the factory's power distribution networks.
- Effects of the power quality problems on each and every electrical device in the factory's distribution network.

Research Fund Acknowledgment

This research thesis was funded by Adama Science and Technology University under the grant number of ASTU/SM-R/575/22, Adama, Ethiopia.

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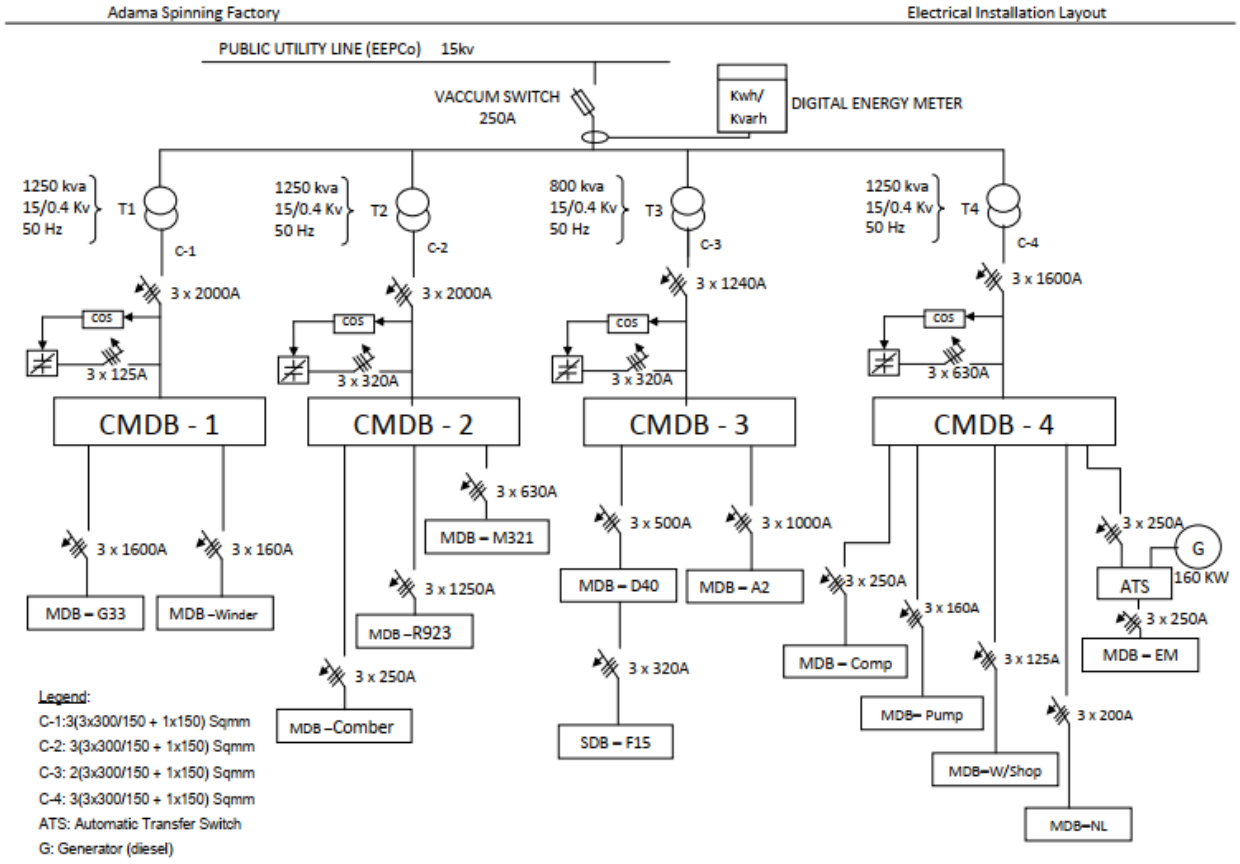
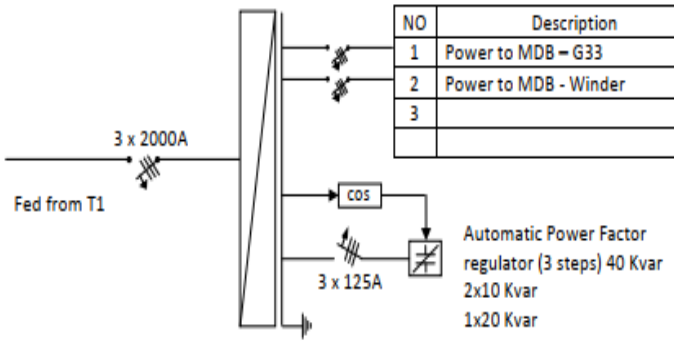
APPENDICES

Appendix A: Adama Spinning Factory Electrical Installation Layout



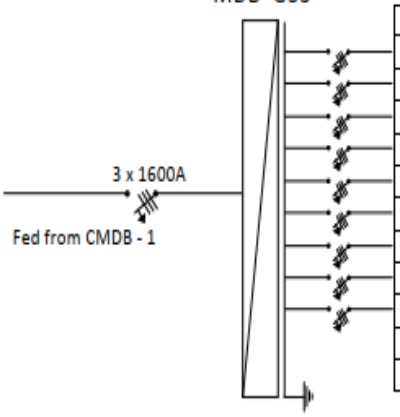
CMDB–1



NO	Description	A(mm²)	I (A)	Load (KW)
1	Power to MDB – G33	5(3x150/70 + 1x70)	3 x 1600	652.80
2	Power to MDB - Winder	2(3x120/70 + 1x70)	3 x 630	231.39
3				

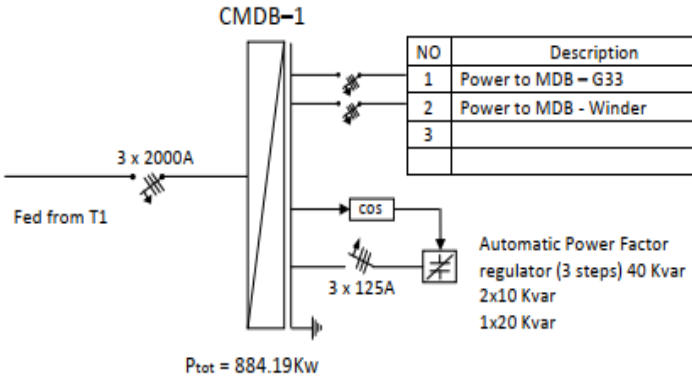
P_{tot} = 884.19Kw

MDB–G33



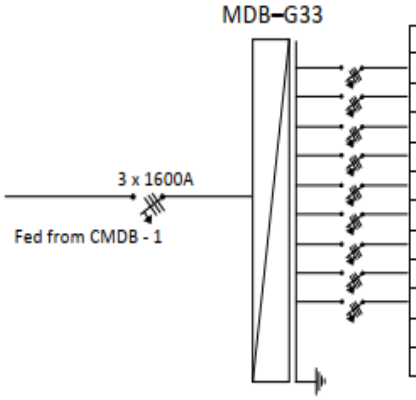
NO	Description	A(mm²)	I (A)	Load (KW)
1	Ring Frame – G33	3 x 95	3 x 200	81.6
2	Ring Frame – G33	3 x 95	3 x 200	81.6
3	Ring Frame – G33	3 x 95	3 x 200	81.6
4	Ring Frame – G33	3 x 95	3 x 200	81.6
5	Ring Frame – G33	3 x 95	3 x 200	81.6
6	Ring Frame – G35	3 x 95	3 x 200	81.6
7	Ring Frame – G35	3 x 95	3 x 200	81.6
8	Ring Frame – G35	3 x 95	3 x 200	81.6
9	Reserve (x 8)	-	3 x 25 (each)	-
10				

P_{tot} = 652.80 Kw



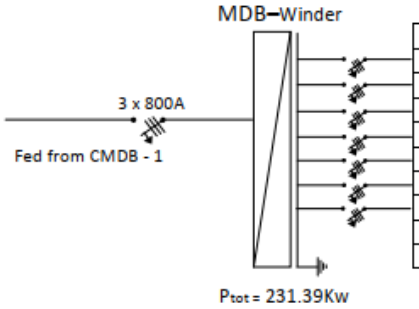
NO	Description	A(mm^2)	I (A)	Load (KW)
1	Power to MDB – G33	5(3x150/70 + 1x70)	3 x 1600	652.80
2	Power to MDB - Winder	2(3x120/70 + 1x70)	3 x 630	231.39
3				

P_{tot} = 884.19Kw

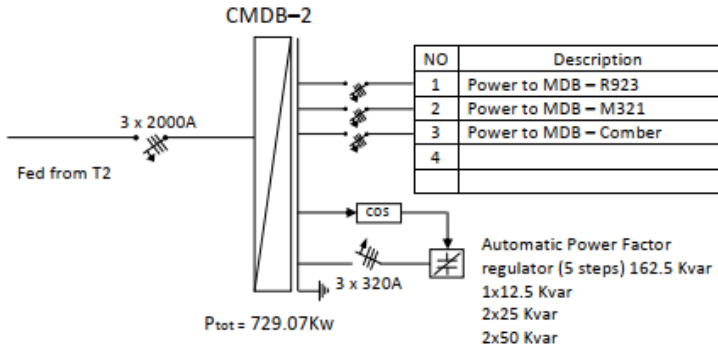


NO	Description	A(mm^2)	I (A)	Load (KW)
1	Ring Frame – G33	3 x 95	3 x 200	81.6
2	Ring Frame – G33	3 x 95	3 x 200	81.6
3	Ring Frame – G33	3 x 95	3 x 200	81.6
4	Ring Frame – G33	3 x 95	3 x 200	81.6
5	Ring Frame – G33	3 x 95	3 x 200	81.6
6	Ring Frame – G35	3 x 95	3 x 200	81.6
7	Ring Frame – G35	3 x 95	3 x 200	81.6
8	Ring Frame – G35	3 x 95	3 x 200	81.6
9	Reserve (x 8)	-	3 x 25 (each)	-
10				

P_{tot} = 652.80 Kw

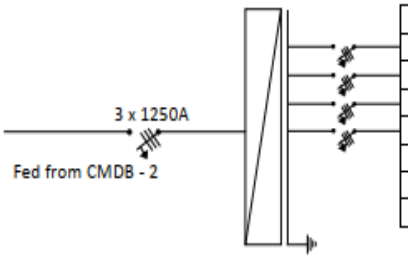


NO	Description	A(mm²)	I (A)	Load (KW)
1	Doubler - RIFA	3x4 + 1x4	3 x 25	6.75
2	Doubler - RITE	4 x 10	3 x 63	14.52
3	Doubler - RITE	4 x 10	3 x 63	14.52
4	Twister - RIFA	3 x 70	3 x 100	23.5
5	Twister - SAVIO	3 x 50	3 x160	62.7
6	Twister - SAVIO	3 x 70	3 x160	62.7
7	Twister - SAVIO	3 x 70	3 x160	46.7
8				



NO	Description	A(mm²)	I (A)	Load (KW)
1	Power to MDB – R923	4(3x150/70 + 1x70)	3 x 1250	392.00
2	Power to MDB – M321	2(3x150/70 + 1x70)	3 x 630	255.00
3	Power to MDB – Comber	3x120/70 + 1x70	3 x 250	82.07
4				

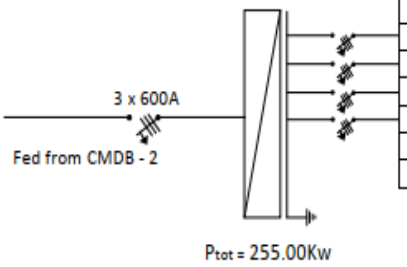
MDB–R923



NO	Description	A(mm^2)	I (A)	Load (KW)
1	Open End - R923	3 x 150/70	3 x 250	98
2	Open End - R923	3 x 150/70	3 x 250	98
3	Open End - R923	3 x 150/70	3 x 175	98
4	Open End - R923	3 x 150/70	3 x 175	98
5	Open End - R923 (Expansion)	3 x 150/70	-	-
6				

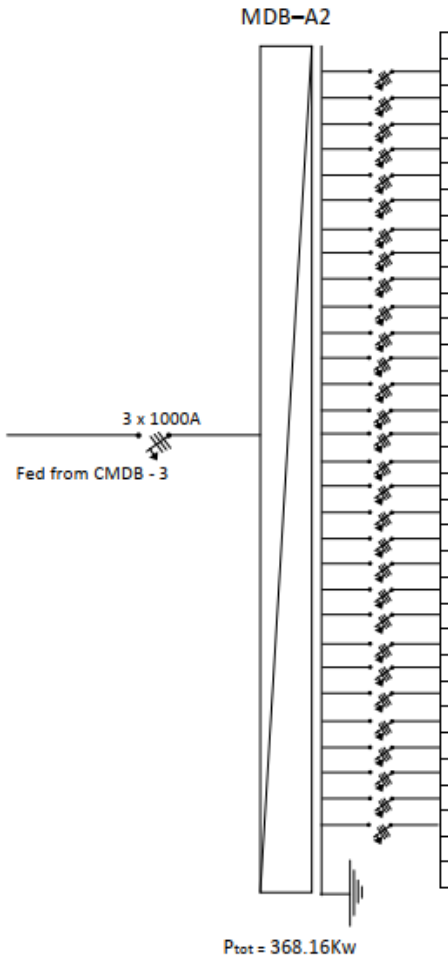
P_{tot} = 392.00Kw

MDB–M321

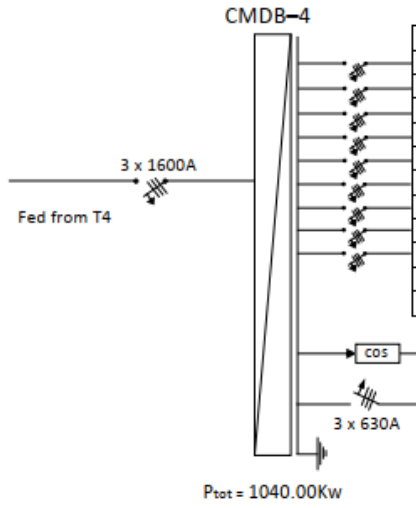


NO	Description	A(mm^2)	I (A)	Load (KW)
1	Winding- Muratec	3x35 + 1x16	3 x 100	36
2	Winding - Muratec	3x35 + 1x16	3 x 100	36
3	Winding-Muratec	3x35 + 1x16	3 x 100	41
4	Steamer	3x150/70	3 x 400	142
5				

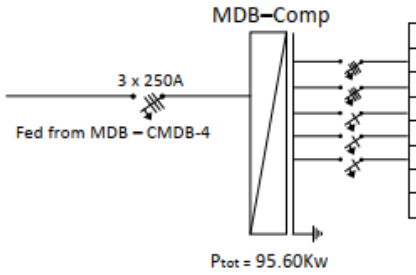
P_{tot} = 255.00Kw



NO	Description	A(mm^2)	I (A)	Load (KW)
1	Unifloc - A11	3x10 + 1x10	3 x 40	14.5
2	Uniclean - B11	3x10 + 1x10	3 x 40	11.25
3	Unimix - B70	3x6 + 1x6	3 x 25	4.25
4	Unimix - B70	3x6 + 1x6	3 x 25	4.25
5	Uniflex - B60	3x16 + 1x16	3 x 63	16.5
6	Uniflex - B60	3x16 + 1x16	3 x 63	16.5
7	Vision Shield	3x6 + 1x6	3 x 25	1.2
8	Vision Shield	3x6 + 1x6	3 x 25	1.2
9	Condenser - A21	3x2.5 + 1x2.5	3 x 25	3.75
10	Condenser - A21	3x2.5 + 1x2.5	3 x 25	3.75
11	Waste Transport - B25	3x2.5 + 1x2.5	3 x 25	3.15
12	Fan - A40/1	4 x 1.5	3 x 25	2.2
13	Fan - A40/1	4 x 1.5	3 x 25	2.2
14	Fan - A40/1	4 x 1.5	3 x 25	2.2
15	Fan - A40/1	4 x 1.5	3 x 25	2.2
16	Fan - A43/1	4 x 1.5	3 x 25	5.5
17	Fan - A43/1	4 x 1.5	3 x 25	5.5
18	Fan - A43/1	4 x 1.5	3 x 25	5.5
19	Fan - A43/1	4 x 1.5	3 x 25	5.5
20	Fan - A43/1	4 x 1.5	3 x 25	5.5
21	Fan - A44/1	3x10 + 1x10	3 x 40	7.5
22	Carding - C60H	3x25 + 1x16	3 x 80	33.98
23	Carding - C60H	3x25 + 1x16	3 x 80	33.98
24	Carding - C60H	3x25 + 1x16	3 x 80	33.98
25	Carding - C60H	3x25 + 1x16	3 x 80	29.4
26	Carding - C60	3x25 + 1x16	3 x 80	30.16
27	Carding - C60	3x25 + 1x16	3 x 80	30.16
28	Carding -C60	3x25 + 1x16	3 x 80	26.2
29	Carding -C60	3x25 + 1x16	3 x 80	26.2
30	Reserve (x 4)	-	3 x 25 (each)	-
31				



NO	Description	A(mm^2)	I (A)	Load (KW)
1	Power to SDB - Comp	2(3 x 35/25)	3 x 250	95.60
2	Power to SDB - Workshop	3x35 + 1x16	3 x 125	40.8
3	Power to SDB - Pump	4x70	3 x 160	210.65
4	Power to MDB - NL	4x120	3 x 200	67
5	Power to MDB - EM	4x120	3 x 250	202.45
6	Bale Press	3x6 + 1x6	3 x 32	8.5
7	AC 1 and 2	2(4x150)	3 x 630	261
8	AC 3 and 4	2(4x95)	3 x 400	154
9	Reserve	-	3 x 63	-
10				



NO	Description	A(mm^2)	I (A)	Load (KW)
1	Compressor – Sarmak	3 x35/16	3 x 125	46.1
2	Compressor – Sarmak	3 x35/16	3 x 125	47.2
3	Air Dryer	3 x 2.5	16	1
4	Air Dryer	3 x 2.5	16	1
6	Exhaust Fan	3 x 2.5	16	0.3
7				

Appendix B: Harmonic Distortion Data Measurement from all CMDBs

Table B.1: Measured Harmonic Distortion Data on CMDB-1

Date	Time	PF	Isec	Current Harmonic Distortion							Voltage Harmonic Distortion						
				THD_I	1^{st}	3^{rd}	5^{th}	7^{th}	9^{th}	11^{th}	THDv	1^{st}	3^{rd}	5^{th}	7^{th}	9^{th}	11^{th}
5/2/2022	8:30 AM	0.76	0.86	23.87	0.88	0.04	0.16	0.13	0	0	2.91	224	0	5	4	0	1
7/2/2022	9:05AM	0.74	0.81	21.73	0.78	0.02	0.15	0.07	0	0.03	1.63	223	0	2	3	0	0
9/2/2022	11:15 AM	0.81	0.78	16.75	0.76	0.01	0.08	0.09	0	0.04	1.67	225	0	3	2	0	1
12/2/2022	1:40 PM	0.83	0.92	15.25	0.87	0.03	0.09	0.09	0.01	0.02	2.21	227	0	3	4	0	0
14/2/2022	2:30 PM	0.72	0.82	22.15	0.8	0.04	0.15	0.08	0	0.03	1.28	222	0	2	2	0	0
17/2/2022	3:45 PM	0.79	0.63	19.91	0.59	0.02	0.07	0.09	0	0.02	1.57	230	0	3	2	0	0
22/2/2022	10:06 AM	0.8	0.78	26.36	0.82	0.03	0.17	0.12	0	0.05	1.62	233	0	2	3	0	1
24/2/2022	11:15 AM	0.83	0.69	35.85	0.62	0.06	0.19	0.09	0	0.04	1.97	228	0	4	2	0	0
25/2/2022	4:15 PM	0.75	0.92	16.71	0.84	0.04	0.08	0.09	0	0.06	2.04	226	0	2	4	0	1
3/3/2022	8:30 AM	0.74	0.67	16.53	0.64	0.06	0.05	0.07	0.01	0.01	1.95	224	0	3	3	0	1
7/3/2022	9:00 AM	0.82	0.85	16.84	0.62	0.05	0.02	0.08	0	0.04	2.05	223	0	4	2	0	1
11/3/2022	2:32 PM	0.81	0.78	17.90	0.76	0.02	0.06	0.12	0.01	0	1.28	221	0	2	2	0	0

Table B.2: Measured Harmonic Distortion Data on CMDB-2

Date	Time	PF	Isec	Current Harmonic Distortion							Voltage Harmonic Distortion						
				THD_I	1^{st}	3^{rd}	5^{th}	7^{th}	9^{th}	11^{th}	THDv	1^{st}	3^{rd}	5^{th}	7^{th}	9^{th}	11^{th}
5/2/2022	8:35 AM	0.89	0.88	7.2	0.87	0	0.06	0.02	0	0	1.37	219	1	0.07	1	0	1
7/2/2022	9:10 AM	0.84	0.8	5.2	0.8	0.02	0.03	0.02	0	0	0.92	221	0	2	0.3	0	0
9/2/2022	11:20 AM	0.88	0.79	6.54	0.78	0.01	0.03	0.04	0	0	1.9	220	0	4	1.1	0	0
12/2/2022	1:45 PM	0.9	0.91	5.1	0.9	0	0.04	0.02	0	0.01	2.41	227	0	2	5	0	1
14/2/2022	2:35 PM	0.8	0.84	6.52	0.84	0	0.02	0.05	0.01	0	2	224	0	4	2	0	0
17/2/2022	3:50 PM	0.79	0.6	5.72	0.58	0.01	0.01	0.03	0	0	1.15	231	1	1	2	0	1
22/2/2022	10:11 AM	0.85	0.78	8.93	0.8	0.03	0.05	0.04	0	0.01	1.53	220	0.2	2	2.5	0	1
24/2/2022	11:20 AM	0.86	0.71	5.55	0.65	0	0.02	0.03	0	0	1.22	223	0	2.2	0.9	1.3	0
25/2/2022	4:20 PM	0.83	0.73	5.89	0.72	0.01	0.03	0.02	0.02	0	1.51	215	0	1.6	2.8	0.2	0
3/3/2022	8:35 AM	0.84	0.76	6.90	0.78	0.02	0.03	0.04	0	0	1.24	220	0	1.8	2	0.4	0
7/3/2022	9:05 AM	0.86	0.78	6.76	0.81	0.01	0.05	0.02	0	0	1.77	222	1	3.1	2.2	0	0
11/3/2022	2:37 PM	0.85	0.77	7.27	0.79	0.02	0.03	0.04	0.02	0	2.08	218	1	1.4	4	0.8	1

Table B.3: Measured Harmonic Distortion Data on CMDB-3

Date	Time	PF	Isec	Current Harmonic Distortion							Voltage Harmonic Distortion						
				THD_I	1st	3rd	5th	7th	9th	11th	THDv	1st	3rd	5th	7th	9th	11th
5/2/2022	8:40 AM	0.72	0.62	23.2	0.59	0.02	0.12	0.05	0	0.01	1.51	220	1	1	3	0	0
7/2/2022	9:15 AM	0.71	0.59	33.73	0.61	0.03	0.18	0.09	0	0.03	0.63	218	0	0.8	0.5	1	0
9/2/2022	11:25 AM	0.73	0.98	20.14	1.04	0.01	0.2	0.06	0	0.01	2.32	216	0	4	3	0	0
12/2/2022	1:50 PM	0.76	0.88	20.71	0.83	0.01	0.17	0.02	0.01	0	1.34	224	0	2	2	0	1
14/2/2022	2:40 PM	0.81	0.76	19.46	0.68	0.05	0.08	0.09	0.02	0.01	1.85	229	0	1	4	1	0
17/2/2022	3:55 PM	0.78	0.54	22.34	0.52	0.01	0.07	0.09	0	0.02	1.81	232	1	3.4	2	0	1
22/2/2022	10:16 AM	0.7	0.73	16.14	0.72	0.02	0.09	0.07	0	0.01	1.7	225	0.6	1	3.5	0	1
24/2/2022	11:25 AM	0.75	0.58	17.67	0.56	0.01	0.05	0.08	0	0.01	2.05	221	0.2	3.7	2.4	1	0
25/2/2022	4:25 PM	0.77	0.76	18.34	0.74	0.01	0.1	0.09	0.01	0.01	1.55	217	0	1.5	3	0	0
3/3/2022	8:40 AM	0.79	0.60	16.08	0.67	0.04	0.06	0.08	0	0	1.60	228	1	3	1.5	1	0
7/3/2022	9:10 AM	0.81	0.55	17.15	0.78	0.03	0.12	0.05	0	0.01	1.88	215	0.4	2.5	3	0	1
11/3/2022	2:42 PM	0.76	0.78	16.20	0.80	0.05	0.09	0.07	0.02	0.03	1.40	231	0.8	0.7	2.7	1	1

Table B.4: Measured Harmonic Distortion Data on CMDB-4

Date	Time	PF	Isec	Current Harmonic Distortion							Voltage Harmonic Distortion						
				THD_I	1st	3rd	5th	7th	9th	11th	THDv	1st	3rd	5th	7th	9th	11th
5/2/2022	8:45 AM	0.88	2.36	2.13	2.25	0.02	0.03	0.03	0	0.01	1.14	215	0	2	1	0	1
7/2/2022	9:20 AM	0.93	2.42	3.81	2.38	0.01	0.04	0.08	0	0.01	1.42	222	0	1	3	0	0
9/2/2022	11:30 AM	0.91	2.64	3.77	2.53	0.01	0.08	0.05	0	0.01	1.03	218	0	2	1	0	0
12/2/2022	1:55 PM	0.9	2.29	2.94	2.33	0.01	0.03	0.06	0	0.01	0.95	227	0	0.8	2	0	0
14/2/2022	2:45 PM	0.95	2.79	2.36	2.65	0.02	0.03	0.04	0.03	0.01	1.61	224	0	3	2	0	0
17/2/2022	4:00 PM	0.92	2.12	2.29	2.51	0.02	0.02	0.04	0	0.03	0.75	231	0	1	1	0	1
22/2/2022	10:21 AM	0.86	2.58	2.96	2.62	0.03	0.05	0.05	0.01	0	1.005	226	0.4	2	1	0	0
24/2/2022	11:30 AM	0.89	2.13	2.62	2.26	0.04	0.03	0.03	0.01	0	1.41	225	0	1	3	0	0
25/2/2022	4:30 PM	0.84	2.23	2.55	2.32	0.03	0.04	0.03	0	0.01	1.12	219	0	1	2	0	1
3/3/2022	8:45 AM	0.92	2.32	3.12	2.60	0.01	0.06	0.05	0	0.02	1.15	210	0.2	0.9	2	0	1
7/3/2022	9:15 AM	0.88	2.60	3.07	2.58	0.03	0.02	0.07	0.01	0	0.99	229	0.4	2	1	0	0
11/3/2022	2:47 PM	0.94	2.45	3.28	2.42	0.02	0.07	0.03	0	0.01	1.37	230	0	3	1	0	0

Appendix C: Adama Spinning Factory monthly energy consumption report (July, 2020 - June, 2021)

	Company Name: ADAMA DEVELOPMENT PLC Adama Spinning Factory	Document No: ADSF- OF- 367	
Title	Annual Electric Energy Consumption	Revision No: 00	Page : 1 of 1

SPINNING — **Fiscal Year: 2020/2021**

Meter Constant(KWh/KVARh):	6000
Power Factor Penality Block Rate(Birr):	68.37
Active Energy Block Rate(Birr/KWh):	0.5778
Active Energy Block Rate(Birr/KWh):	0.8161
Active Energy Block Rate(Birr/KWh):	1.0544
Active Energy Block Rate(Birr/KWh):	1.2927
Max.Demand Block Rate(Birr/KWh):	50
Max.Demand Block Rate(Birr/KWh):	100
Max.Demand Block Rate(Birr/KWh):	150
Service Charge(Birr):	54

Contract No.:	549701302737482276464 4
Tariff Category:	41-ICS-INDUSTRIAL
Meter Number:	ECE000064/516776

S/N	Consumption period			Active Energy		Reactive Energy		Max. Demand			Power Factor	PF Penality (Birr)	Active Energy Cost (Birr)	Total Payment (Birr)	Production (Kg)	Unit Cost (Birr/Kg)
	Month	Days	Reading Date	Reading	KWh	Reading	KVARh	Reading	MD (KWh)	MD(kwhb)						
1	Jul, 2020	30	10-Jul-20	9935	#REF!	4809	270000	0.19	1140	114000	#REF!	#REF!	#REF!	#REF!		#REF!
2	Aug, 2020	31	10-Aug-20	10117	1092000	4907	588000	0	0	0	0.88047	0.00	1,151,404.8	1,151,458.80		#DIV/0!
3	Sep, 2020	33	12-Sep-20	10210	558000	4958	306000	0.000	0	0	0.87681	0.00	588,355.2	588,409.20		#DIV/0!
4	Oct, 2020	30	12-Oct-20	10260	300000	4981	138000	0.79	4740	474000	0.90849	0.00	316,320.0	790,374.00		#DIV/0!
5	Nov, 2020	31	12-Nov-20	10288	168000	4994	78000	0.09	540	54000	0.90701	0.00	177,139.2	231,193.20		#DIV/0!
6	Dec, 2020	36	18-Dec-20	10348	360000	5026	192000	0.1587	952.2	95220	0.88235	1148.86	379,584.0	476,006.86		#DIV/0!
7	Jan, 2021	28	15-Jan-21	10437	534000	5075	294000	0.168	1008	151200	0.87601	1653.45	690,301.8	843,209.25		#DIV/0!
8	Feb, 2021	32	16-Feb-21	10526	534000	5125	300000	0.2	1200	180000	0.87184	2310.60	690,301.8	872,666.40		#DIV/0!
9	Mar,2021	56	13-Apr-21	10629	618000	5184	354000	0.18	1080	162000	0.86772	2383.23	798,888.6	963,325.83		#DIV/0!
10	Apr, 2021	30	13-May-21	10727	588000	5241	342000	0.18	1080	162000	0.86442	2627.36	760,107.6	924,788.96		#DIV/0!
11	May,2021	34	16-Jun-21	10844	702000	5307	396000	0.19	1140	171000	0.87098	2261.99	907,475.4	1,080,791.39		#DIV/0!
12	Jun, 2021	27	13-Jul-21	10936	552000	5360	318000	0.15	900	135000	0.8665	2061.42	713,570.4	850,685.82		#DIV/0!
	Total	####			#REF!		3576000				#REF!	#REF!	#REF!	#REF!	-	#REF!

Prepared By: _____ Approved By: _____

Appendix D: Voltage Sag recorded for all CMDBs

Table D.1: Voltage sag data for CMDB-1

Date	Time	Voltage level			Duration	Remark
		A	B	C		
5/2/2022	9:23 AM	228.4V	229.2V	228.9V	0.2sec	Normal
7/2/2022	8:48 AM	225.45V	227.3V	227.8V	0.12sec	Normal
9/2/2022	10:25 AM	222.6V	222.4V	221.7V	0.1sec	Normal
12/2/2022	2:52 PM	225.8V	226.2V	226.4V	0.3sec	Normal
14/2/2022	11:31 AM	230.4V	230.9V	230.7V	0.3sec	Normal
17/2/2022	10:44 AM	227.5V	227.2V	226.8V	0.2sec	Normal
22/2/2022	3:12 PM	223.3V	223.6V	222.9V	0.19sec	Normal
25/2/2022	9:55 AM	220.2V	220.4V	221.3V	0.13sec	Normal
29/2/2022	4:27 PM	225.1V	224.7V	224.2V	0.17sec	Normal
3/3/2022	9:21 AM	220.5V	220.7V	219.9V	0.16sec	Normal
7/3/2022	8:39 AM	218.3V	219.2V	219.4V	0.25sec	Normal
11/3/2022	10:49 AM	223.1V	222.7V	222.5V	0.2sec	Normal

Table D.2: Voltage Sag data for CMDB-2

Date	Time	Voltage level			Duration	Remark
		A	B	C		
5/2/2022	10:11 AM	207.4V	206.8V	208.3V	0.18sec	Sag
7/2/2022	9:37 AM	215.47V	217.1V	216.2V	0.2sec	Normal
9/2/2022	10:18 AM	205.1V	204.5V	206.3V	0.12sec	Sag
12/2/2022	2:50 PM	222.4V	223.1V	222.7V	0.2sec	Normal
14/2/2022	10:32 AM	224.1V	223.9V	224.6V	0.17sec	Normal
17/2/2022	3:56 AM	205.6V	206.3V	205.4V	0.3sec	Sag
22/2/2022	4:23 PM	225.1V	226.2V	225.8V	0.16sec	Normal
25/2/2022	10:42 AM	228.1V	227.8V	228.3V	0.12sec	Normal
29/2/2022	8:36 AM	214.2V	214.8V	215.4V	0.15sec	Normal
3/3/2022	2:25 PM	216.6V	217.1V	217.2V	0.21sec	Normal
7/3/2022	3:30 PM	219.9V	220.3V	220.1V	0.23sec	Normal
11/3/2022	10:14 AM	223.5V	223.7V	222.8V	0.19sec	Normal

Table D.3: Voltage Sag data for CMDB-3

Date	Time	Voltage level			Duration	Remark
		A	B	C		
5/2/2022	10:27 AM	226.5V	227.1V	227.0V	0.15sec	Normal
7/2/2022	9:44 AM	223.5V	223.7V	224.2V	0.14sec	Normal
9/2/2022	10:42 AM	226.8V	226.6V	226.3V	0.16sec	Normal
12/2/2022	2:56 PM	228.4V	228.7V	229.1V	0.32sec	Normal
14/2/2022	11:23 AM	226.2V	225.9V	226.4V	0.2sec	Normal
17/2/2022	10:53 AM	222.1V	221.4V	220.9V	0.18sec	Normal
22/2/2022	3:22 PM	220.3V	221.2V	220.5V	0.21sec	Normal
25/2/2022	9:54 AM	219.4V	218.2V	217.6V	0.19sec	Normal
29/2/2022	4:35 PM	215.3V	216.3V	215.9V	0.17sec	Normal
3/3/2022	9:33 AM	218.8V	219.1V	218.7V	0.18sec	Normal
7/3/2022	10:48 AM	214.6V	215.2V	216.2V	0.15sec	Normal
11/3/2022	11:43 AM	219.8V	219.6V	220.2V	0.22sec	Normal

Table D.4: Voltage Sag data for CMDB-4

Date	Time	Voltage level			Duration	Remark
		A	B	C		
5/2/2022	10:58 AM	220.2V	220.4V	219.8V	0.2sec	Normal
7/2/2022	9:24 AM	203.4V	202.5V	204.1V	0.16sec	Sag
9/2/2022	9:22 AM	216.3V	216.6V	215.2V	0.18sec	Normal
12/2/2022	2:53 PM	204.3V	205.7V	206.2V	0.22sec	Sag
14/2/2022	10:33 AM	216.4V	215.8V	216.6V	0.12sec	Normal
17/2/2022	8:42 AM	215.2V	217.2V	216.7V	0.23sec	Normal
22/2/2022	4:19 PM	202.1V	201.3V	200.8V	0.15sec	Sag
25/2/2022	10:54 AM	207.6V	208.3V	207.2V	0.18sec	Sag
29/2/2022	4:48 PM	218.2V	218.5V	217.9V	0.14sec	Normal
3/3/2022	9:26 AM	224.5V	223.7V	224.2V	0.2sec	Normal
7/3/2022	10:27 AM	216.7V	216.3V	216.2V	0.22sec	Normal
11/3/2022	5:24 PM	221.2V	222.3V	221.8V	0.17sec	Normal