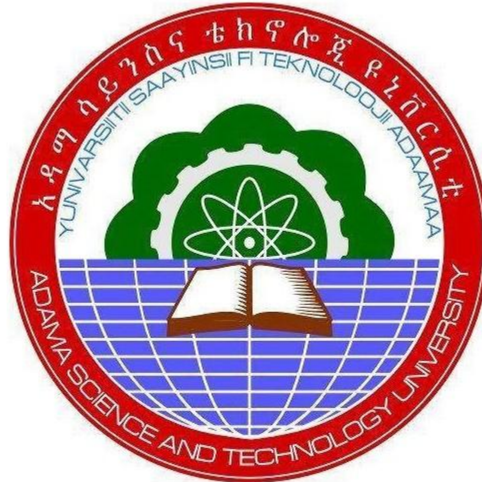
Optimization Of Double Gate Junctionless Field Effect Transistor For Low power Memory Application Using T-Cad Tools.



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1. Abstract:

This terminal report summarizes the completed project titled " Optimization Of Double Gate Junctionless Field Effect Transistor For Low power Memory Application Using T-Cad Tools.." The project aimed to develop a new structure for planar JLFETs that significantly decreases the off-state current.

To achieve this goal, the project pursued specific objectives. Firstly, the length, thickness, and construction materials of the spacer, which is the distance between the source/drain and the gate, were varied to improve the on-current and reduce the off-state current of the JLFETs. Through extensive simulations and analysis, optimal spacer parameters were determined.

Secondly, the project focused on reducing the action of the parasitic Bipolar Junction Transistor (BJT) by implementing high dielectric constant materials like hafnium dioxide between the channel and the ground plane. This implementation effectively minimized the unwanted current leakage, leading to improved device performance.

Additionally, different semiconductor materials, such as germanium, were utilized to increase the on-current through the channel. This approach enhanced the overall performance of the JLFETs and contributed to achieving higher on-current.

The project relied on the use of TCAD (Technology Computer-Aided Design) tools to simulate and optimize the proposed structure. Through rigorous simulations and analysis, the project yielded valuable insights into the optimization of double gate junctionless field-effect transistors.

In conclusion, the project successfully developed an improved structure for planar JLFETs that effectively reduced the gate-induced leakage current. By achieving the specific objectives outlined above, the project significantly enhanced the performance and efficiency of JLFETs, contributing to advancements in semiconductor technology. The findings of this project can be utilized in the design and fabrication of future JLFET devices, enabling improved functionality and reduced power consumption.

KEY WORD: junctionless, stack gates, short channel effect and Vertical TFET.

2. Acknowledgments.

I would like to express my sincere gratitude and acknowledge the contributions of several individuals and institutions who played a significant role in the successful completion of my project at Adama Science and Technology University in the Department of Applied Physics.

First, I would like to thank God for providing me with the strength, guidance, and inspiration throughout this journey. I am grateful to the reviewer of my project for their valuable feedback, suggestions, and constructive criticism, which greatly enhanced the quality of my work. I would also like to extend my appreciation to the purchaser of the school for their support and provision of necessary resources, which facilitated the smooth execution of the project. Furthermore, I would like to express my heartfelt thanks to Addis Ababa University for their kind cooperation in granting me access to their supercomputer for simulations. This opportunity was instrumental in conducting my research and obtaining accurate results. Lastly, but certainly not least, I want to express my deepest gratitude to my family. Their unwavering love, encouragement, and understanding were crucial in keeping me motivated and focused throughout this project. I am truly grateful to all these individuals and institutions for their invaluable contributions, without which the successful completion of my project would not have been possible

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6. Introduction

This research report presents the findings and outcomes of a project titled " Optimization Of Double Gate Junctionless Field Effect Transistor For Low power Memory Application Using T-Cad Tools.." The objective of this project was to develop a new structure for planar junctionless field-effect transistors (JLFETs) that significantly decreases the off-state current.

JLFETs have gained significant attention in recent years due to their potential to overcome the limitations of traditional transistors. However, one major challenge in their implementation is the presence of gate-induced leakage current, which adversely affects their performance and power efficiency. Therefore, this project aimed to address this issue by optimizing the JLFET structure.

To achieve this objective, we utilized TCAD (Technology Computer-Aided Design) tools, which provide a powerful platform for simulating and analyzing various parameters. By leveraging the capabilities of TCAD, we were able to simulate the behavior of JLFETs under different conditions and evaluate their performance.

The optimization process involved studying the impact of different design parameters, such as gate length, gate oxide thickness, and doping concentration, on the gate-induced leakage current. Through extensive simulations and analysis, we were able to identify the optimal combination of these parameters that minimizes the off-state current while maintaining the desired performance characteristics of the JLFETs.

The findings of this research report provide valuable insights into the optimization of JLFETs and offer potential solutions for reducing gate-induced leakage current. The outcomes of this project can contribute to the development of more efficient and reliable electronic devices, enabling advancements in various fields, including telecommunications, computing, and energy systems.

In summary, this research report presents the outcomes of a project focused on optimizing the double gate junctionless field effect transistor to reduce the gate-induced leakage current. By utilizing TCAD tools, we were able to simulate and analyze various parameters to identify an

optimal JLFET structure. The findings of this research have the potential to enhance the performance and power efficiency of electronic devices and open doors for further advancements in the field of transistor technology.

6.1 Objective:

The general objective of this study was to develop a new structure for planar JLFETs that significantly decreases the off-state current.

To achieve this, specific objectives were pursued:

i) Vary the length, thickness, and construction materials of the spacer (the distance between the source/drain and the gate) to improve the on-current and reduce the off-state current of the JLFETs.

ii) Reduce the action of the parasitic BJT (Bipolar Junction Transistor) by implementing high dielectric constant materials like hafnium dioxide between the channel and the ground plane.

iii) Increase the on-current through the channel by utilizing different semiconductor materials such as germanium.

6.2 Significance:

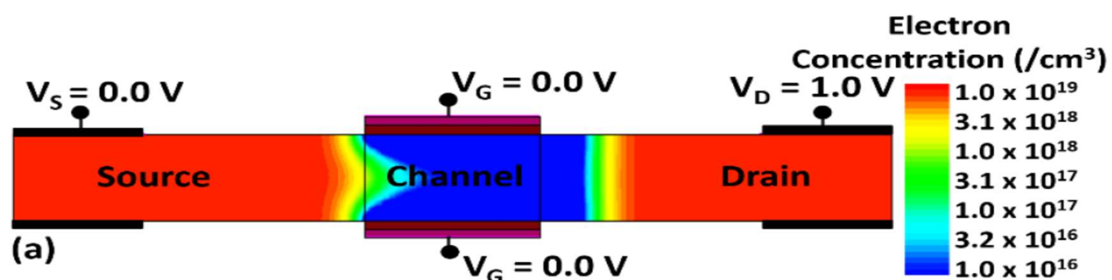
The significance of this project lies in the fact that it addresses the contemporary technology concept of junctionless transistors in the electronics world. The results of this research project serve as a valuable input for further studies in this area. Additionally, the project is expected to yield at least two publications in blind peer-reviewed journals, thereby enhancing the visibility and reputation of both the researchers involved and Adama Science and Technology University. Furthermore, the project provided an opportunity for two MSc students to conduct their thesis research in this specific area of study, fostering their research skills and contributing to the academic growth of the university. Overall, the optimization of double gate junctionless field-effect transistors to reduce gate-induced leakage current carries significant promise for advancing the field of electronics. The outcomes of this project not only contribute to scientific knowledge but also have practical implications for future electronic devices.

7. Literature review

The semiconductor industry has made significant progress, resulting in a growing demand for Nano scale devices in applications requiring analog or radio frequency (RF) capabilities and fast switching speeds [1]. However, power consumption and reliability remain major concerns in integrated circuits (ICs), making device compactness a critical problem in Nano scale systems. As per Moore's law, devices will continue to decrease in size and cost [2]. However, as conventional metal oxide semiconductor field effect transistors (MOSFETs) scale down, they face challenges such as increased OFF-state current and intensified short channel effects (SCE), with a limit of 60mV/Dec subthreshold swing (SS) that cannot be surpassed [3]. Additionally, low switch (Ion/Ioff) ratios and the drain induced barrier lowering (DIBL) effect are becoming more pronounced [4]. To overcome these issues, researchers have proposed and examined various innovative structures. Among them, the tunnel field effect transistor (TFET) has emerged as a promising candidate for future ultra-low power applications [1]. TFETs utilize a gate-controlled band to band tunneling (BTBT) mechanism to modulate carrier injection from the source to the channel. The conventional TFET structure consists of a gated p-type region, an intrinsic region, and an n-type region (p-i-n diode) operating under reverse bias. The gate bias determines the width of the quantum tunneling barrier at the source-channel interface [5]. TFETs offer compatibility with conventional complementary metal oxide semiconductor (CMOS) processes and can overcome the 60mV/Dec SS limit. They are also immune to short channel effects (SCE), and exhibit minimal leakage current in the OFF-state condition [2]. However, TFETs still face challenges such as low ON-state current and a large Miller capacitance [6]. To address these limitations, researchers have proposed novel TFET structures, including the L-shaped channel TFET (LTFET) [3], U-shaped channel TFET (UTFET) [4], symmetric TFET (S-TFET) [5], U-shaped channel with dual sources TFET (DS-UTFET) [6], covered source-channel TFETs (CSC-TFETs) [7], hetero junction TFET with T-shaped gate (HTG-TFET) [8], 2D materials channel TFET, and hetero-bilayer TFETs [9]. It is important to note that most TFETs reported in recent years have an abrupt junction at the tunneling interface, leading to challenges in terms of fabrication processes and thermal considerations [10]. Moreover, achieving a heavily doped concentration in the channel and active region during fabrication is difficult and can be influenced by random dopant fluctuations (RDFs) [10].

The concept of the junctionless transistor (JLT) was first introduced by J. E. Lilienfeld in the 1920s [11]. This unique device does not have a pn junction, eliminating the need for doping concentration gradients. As a result, the fabrication process for transistors with sizes below 10nm is simplified. To realize JLTs, two main requirements must be met. First, the transistor channel must have a high doping concentration of approximately 1X1019 cm-3. Second, the channel thickness should be in the nanometer scale, around 10nm. However, due to limitations in microfabrication technology, it took over 80 years to successfully implement the first junctionless transistor. The breakthrough came with the fabrication of a junctionless nanowire (NW) at the Tyndall Institute by Colinge et al. [12]. This marked the beginning of a new generation of transistors. In recent decades, various other junctionless devices have been proposed, including FinFET [13-17], Gate-All-Around (GAA) [18-22], Single Gate (SGJLT) [23-25], Double Gate (DGJLT) [26-30], Thin Film (TFT) [31-32], and Tunnel FET (TFET) [33-35]

The junctionless FET consists of a uniformly doped semiconductor film with a gate stack that controls the flow of carriers through the film (Fig.1). By adjusting the work function of the gate electrode, the entire thickness of the film can be depleted, achieving volume depletion in the OFF-state [36] (Fig.1(a)). Unlike MOSFETs, where the OFF-state leakage current is determined by the reverse biased p-n junction leakage current, in JLFETs, it is determined by the gate-induced depletion of the channel region [37]. Applying a positive gate voltage reduces the width of the depletion region, exposing a neutral channel region with free carriers in the silicon film, allowing current to flow (Fig.1(b)). Increasing the magnitude of the gate voltage further reduces the depletion region and increases the width of the conducting neutral region. At a certain gate voltage, the neutral region spans the entire thickness of the semiconductor film, resulting in the vanishing of the depletion region. This state is known as the flatband condition (Fig.1(c)). JLFETs are designed to operate at the flatband condition in the ON-state.



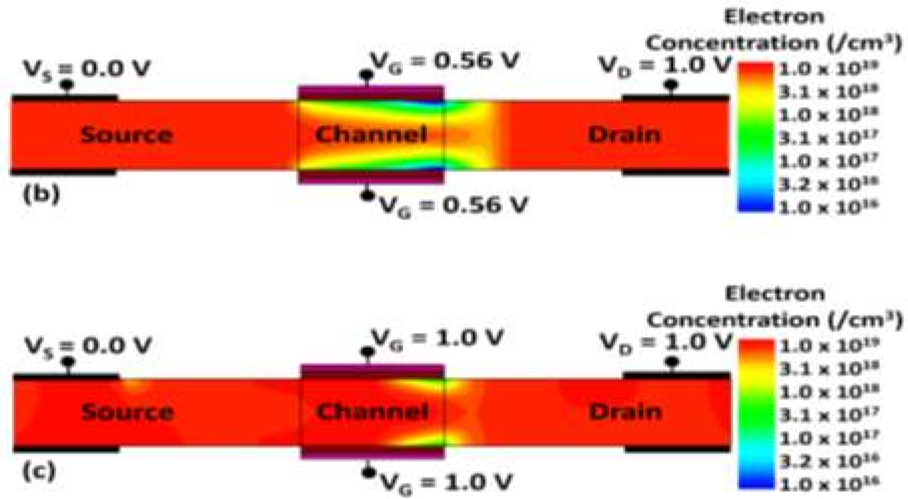


Figure 1 : Different operating regim of JLFET: (a) Full depletion mode (b) partial depeletion mode (c)Flatband mode

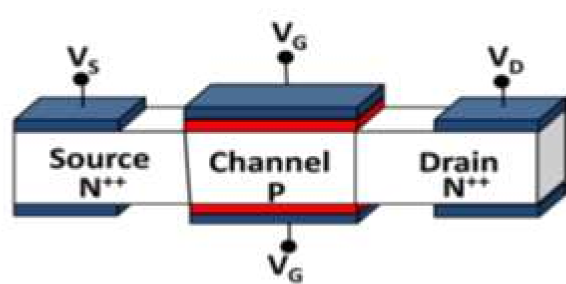


Figure 2 : 3-D view of double gate(DG) N-MOSFETFET

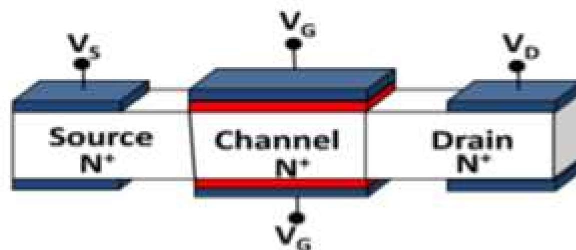


Figure 3 : 3-D view of double gate(DG) junctionless TFET

Figure2 shows the structure of a junctionless tunnel field effect transistor. The device is uniformly and highly doped. The middle gate acts as a control gate, while fixed voltages are applied at the side gates. When considering an n-type device, the tunneling effect can be

triggered by correctly fixing the voltages on the side gates, where the source, channel, and drain regions (n-n-n) are converted into a (p-i-n) structure. When a certain control voltage is applied, the barrier between the source and the channel becomes narrower. As a result, current flows because of tunneling. Therefore, the conduction mechanism is different with respect to the other JLTs, since it is not based on depletion. The high-k dielectric below the gate improves the internal electric field, and, thus, the gate control [33]. The low-k spacers are used to isolate the gates; by increasing the dielectric constant of the low-k spacers, it is possible to reduce I_{off} [34]. Increasing the device layer doping concentration leads to an increment of both I_{on} and I_{off}, with the latter being more sensitive to doping variations. Decreasing the doping concentration leads to an improvement of the SS, since its value decreases from 290mV/dec to 47mV/dec as the doping concentration decreases from $2X10^{19}$ cm^{-3} to $1X10^{19}$ cm^{-3}. Therefore, one of the main advantages of junctionless TFETs is the possibility to achieve sub 60mV/dec SS. Channel length reductions cause an increment of DIBL, and so of the I_{off} [34].

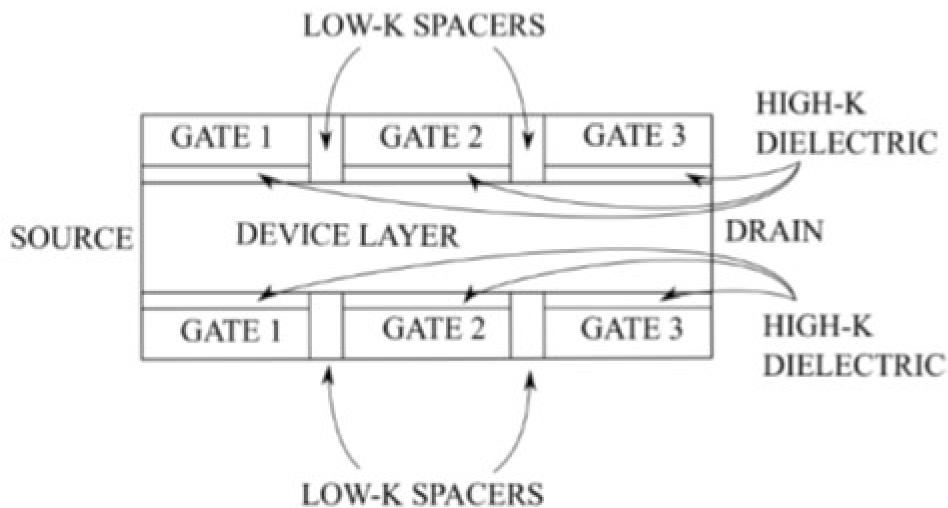


Figure 4 :Cross-sectional view of junctionless field effect transistors.

Regarding double gate junctionless TFETs (Figure 4), the increment of the dielectric constant k leads to an improvement of I_{on}. Increasing the insulation layer thickness causes an improvement in both I_{on} and SS. However, this design choice leads to an increment of the parasitic capacitances [33,34].

To improve the robustness of junctionless TFETs, it is possible to selectively introduce dielectric materials in the gate oxide, which can reduce the variations in the coupling capacitance, allowing for higher immunity in terms of sensitivity [33]. The performance can be further increased by implementing dual-material gate (Figure 4a) or heterojunctionless

structures (Figure 4.3b). The energy bandgap of these structures leads to higher Ion and I_{on}/I_{off}, and lower SS [33,34]. Besides silicon, other materials were used for the device layer: a junctionless TFET made of indium arsenide was proposed [33]. The figure of merits of the reported junctionless transistors are collected in Table 5.

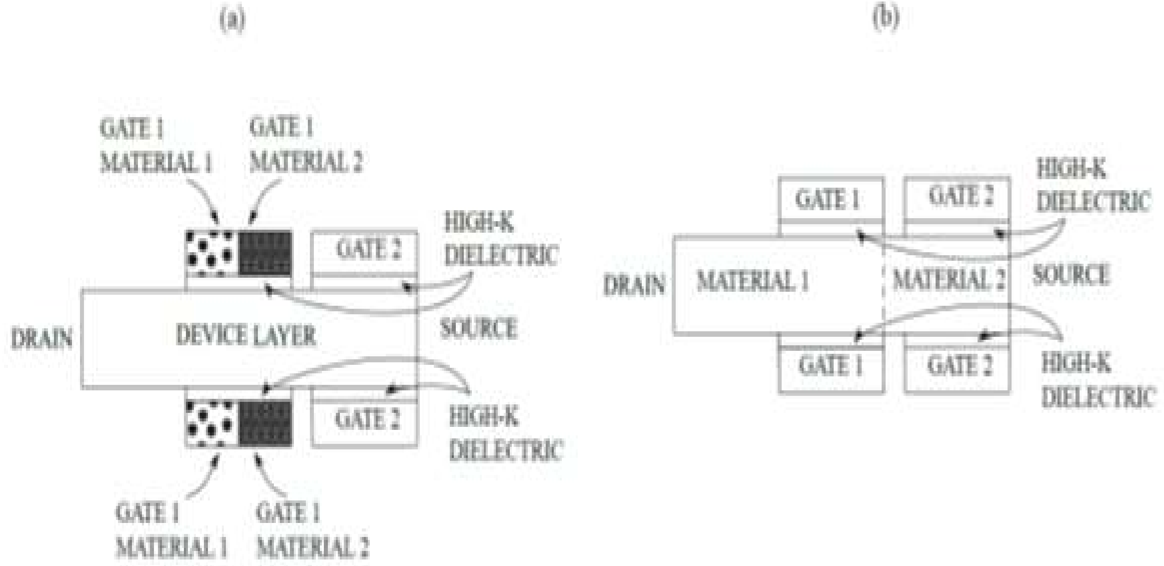


Figure 5: Cross-sectional view of a)JLT tunnel FET(JLTFET) With dual material gate b) JLTFET heterojunction.

8. Methodology

Figure 6 represents the two-dimensional schematics of the proposed JL-VTFET. The x-axis contours the width while the y-axis contours the length of the device. The conventional gate oxide is replaced by SiO_2/HfO_2 stacked gate oxide integrated bilaterally across the channel. For making the device junction-less, n-type doping of 1×10^{19} cm−3 is used as a silicon body, with channel length (L_{ch}) of 50nm and channel thickness (T_{ch}) of 10nm. Platinum metal contacts with work function (ϕ_M) of 5.93eV have been used for source electrodes to create p+ pockets. Highly reactive catalytic metals Cobalt ($\phi_M = 5.0$eV) has been used as gate metal. This validates the wide range of operation of the proposed structure. This contradicts the use of external doping requirements and thus deals with random dopant fluctuation (RDF) issues become unnecessary. The device is studied at a drain-to-source voltage (V_{ds}) and gate-to-source voltage (V_{gs}) of 1V each. All the simulations were performed using ATLAS Silvaco TCAD version 5.26.1.R (Silvaco International, Santa Clara, CA, USA). To consider the band to band tunneling phenomenon in the case of TFET and the spatial variation of the energy bands, the

nonlocal BTBT model (BBT.NONLOCAL) was implemented. The presence of a highly doped channel meant that the Shockley–Read–Hall related to concentration (CONSRH) was activated to account for the minority carrier recombination effects. In addition to this, Fermi statistics (FERMI) and band gap narrowing (BGN) model were also activated. Moreover, a quantum confinement model given by Hansch (HANSCHQM) was also used to take into account quantum confinement effects due to the increased doping levels and thinner gate oxide in the channel. Furthermore, the Schenk model for trap-assisted tunneling (SCHENK.TUNN) was also involved to include the tunneling of electrons from the valence band to the conduction band through trap or defect states and phonon-assisted tunneling effects Table 1 enlists the structural parameters utilized here.

Table 1: List of parameters used for the proposed JL-VTFET.

Parameters	**Symbol**	**Parameters**
Length of channel	L_C	10nm
Thickness of channel	T_C	10nm
Doping	N_D	1×10^{19} cm^{-3}
Gate stack thickness	t_{ox} (SiO_2)	0.5nm
	t_{ox}(HfO_2)	3nm
Source work function	ϕ_{ms}	5.93eV
Drain bias	V_{ds}	1V

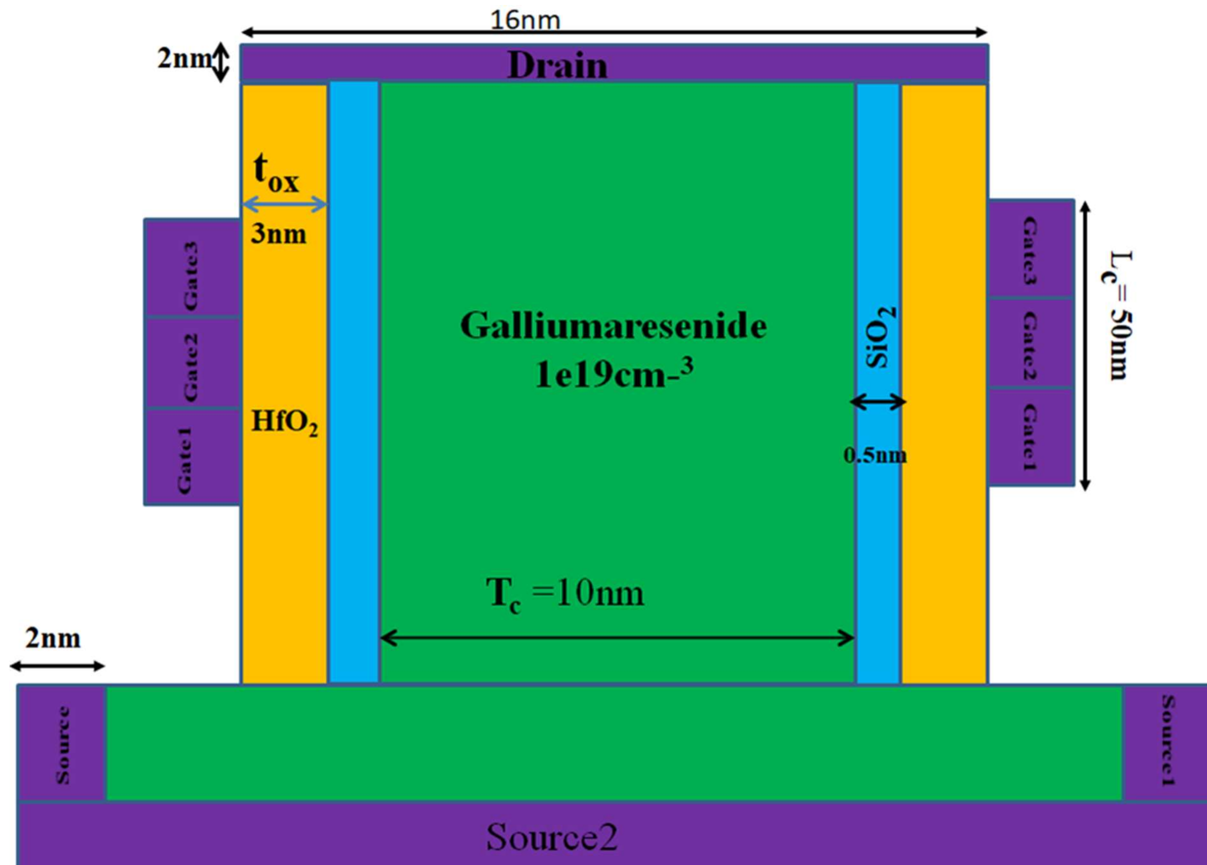


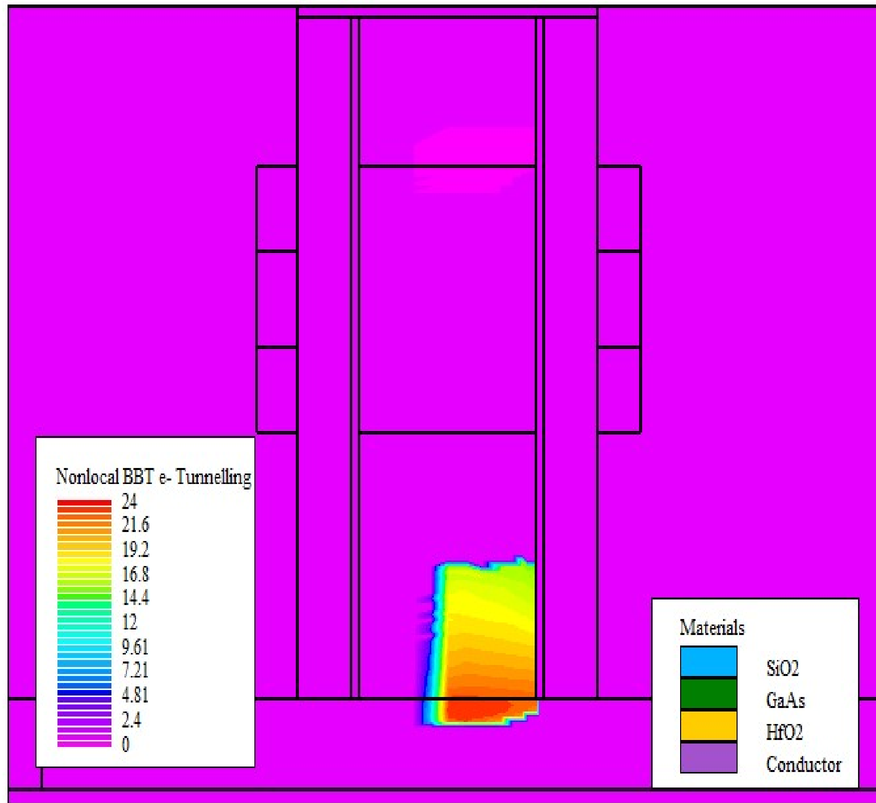
Figure 6 :Design of the proposed double gate junctionless tunnel field effect transistors.

9. Results and Discussion

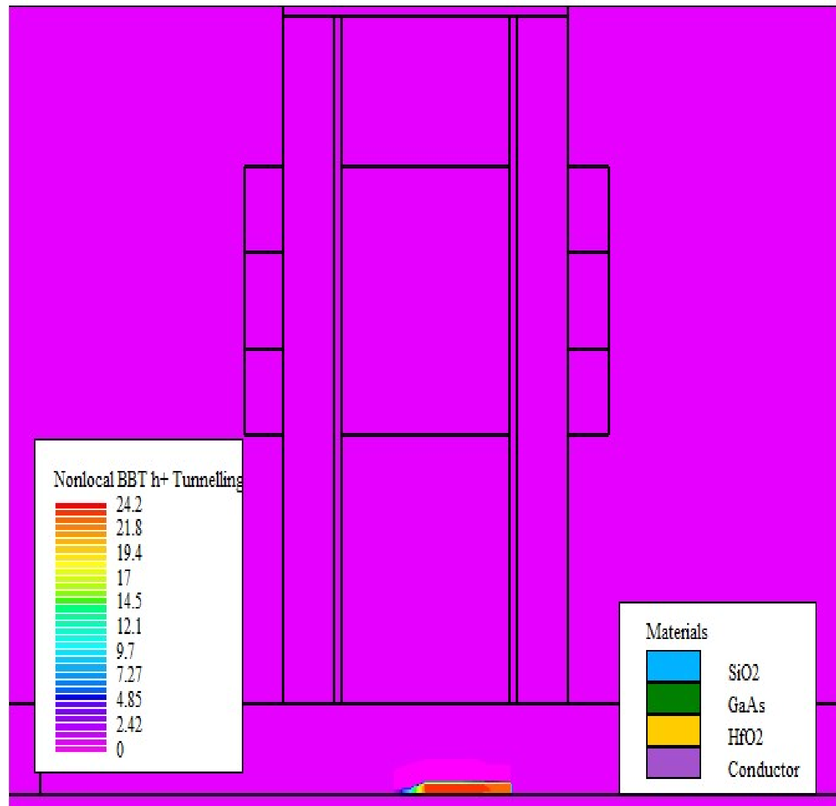
9.1 The Physical Mechanism of stack gate junction-less vertical tunnel field-effect-transistor (JVTFET).

Figure 7 a-d depicts the physical process of the JVTFET. When Vds=1V and Vgs=1V, Figure 4a shows the nonlocal BTBT tunnelling rate of electrons and Figure 7b shows the nonlocal BTBT tunnelling rate of holes of the JVTFET. It was clear that BTBT happened primarily at the source and channel interfaces. Figure 7c depicts the electric field distribution of a JVTFET at Vds=1V and Vgs=1V. It is easy to see from this figure that the value of the electric field was markedly improved near the interface between the channel and the di-electric materials, resulting in a significant increase in ON-state current. In addition, the total current density of

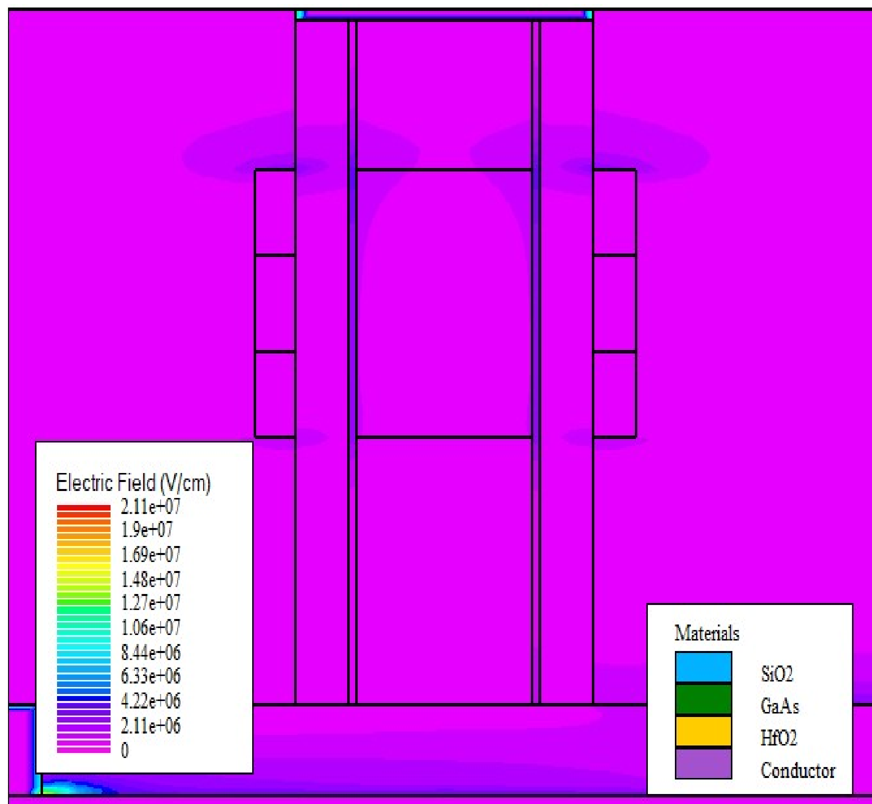
JVTFETs was investigated in order to fully comprehend the physical process, as illustrated in Figure.7 d



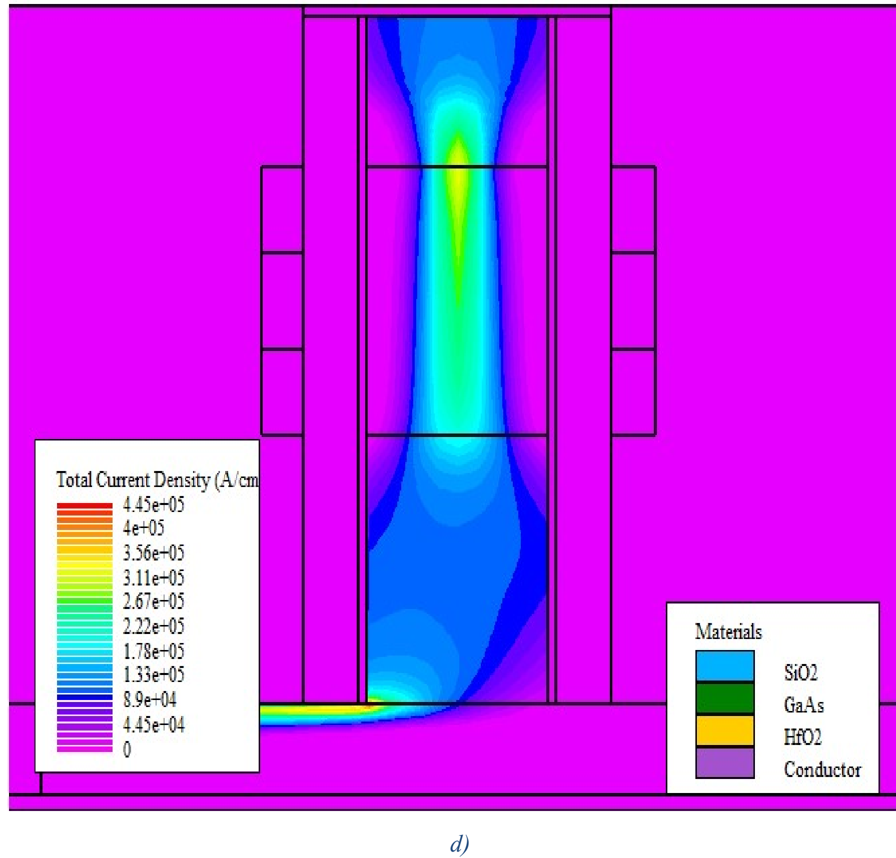
(a)



(b)



(c)



d)

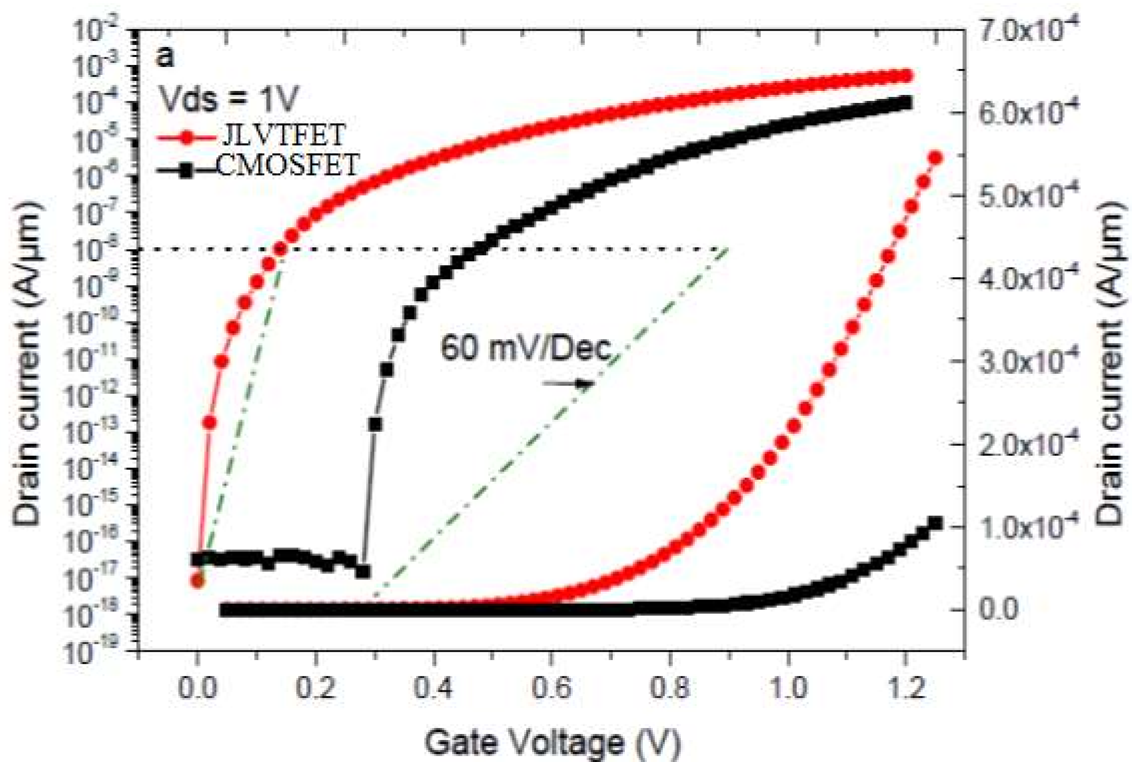
*Figure 7: (**a**) Nonlocal band to band tunneling (BTBT) rate of electrons; (**b**) nonlocal band to band tunneling (BTBT) rate of holes; (**c**) electric field distribution in JVTFET; (**d**) total current density of JVTFET.*

9.2 The Input Characteristics

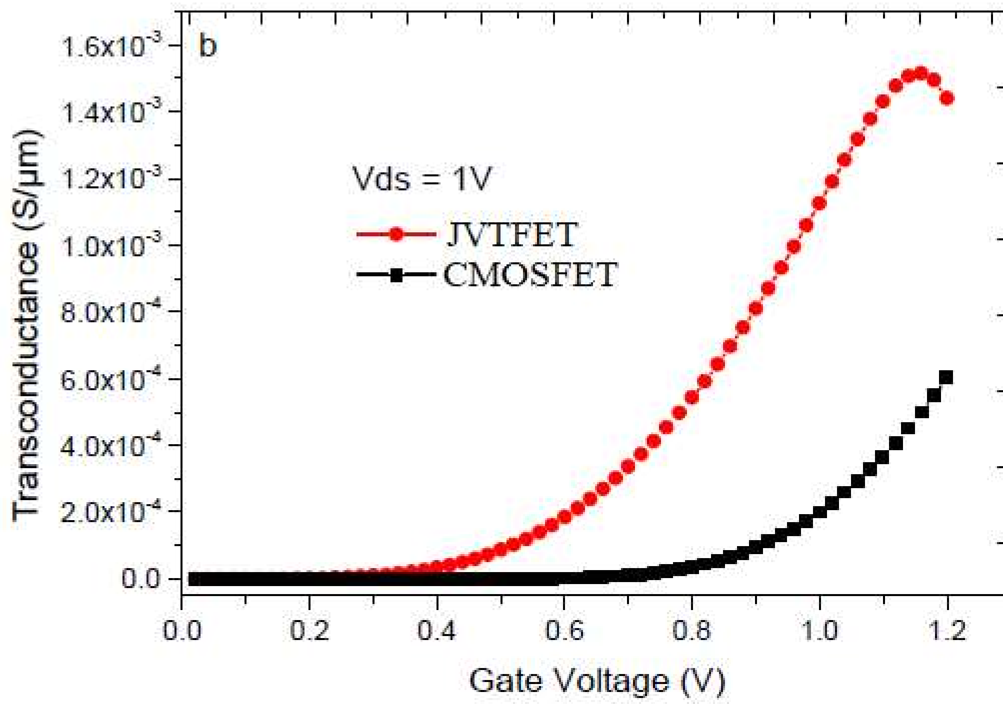
Figure 6.2 depicts the transfer properties of JLVTFETs and conventional MOSFETs (CMOSFET). The ON-state current of the JLVTFET was $1.52X10^{-4}$A/m at Vgs=1V, whereas the equivalent ON-state current of the CMOSFET was only $8X10^{-5}$A/m. Meanwhile, the OFF-state current of JLVTFET was $1.36X10^{-16}$A/m, while the OFF-state current of CMOSFET was $8X10^{-14}$A/m. As a result, the I_{on}/I_{off} ratio of the JLVTFET was raised by an order of magnitude when compared to the conventional MOSFET. Furthermore, due to structural innovation, the JLVTFET has a lower average subthreshold swing (SSave), the SSave (which is extracted from V_{min} to V_t; V_{min} is the gate voltage where drain current equals I_{off}, and V_t is the gate voltage

where drain current equals I_{off} the drain current becomes $1X10^7$A/m when the threshold voltage Vt numbers of the JLVTFET and CMOSFET are taken into account.

Figure 6.2a depicts the energy band diagrams of the JLVTFET and CMOSFET in ON-state (Vds = 1V, Vgs = 1V), where it was observed that the conduction band and valance band of JLVTFET at the source-channel interface were very close to each other and the tunnelling distance of JLVTFET was much smaller than the CMOSFET, i.e. tunnelling width and effective tunneling area of JLVTFET were clearly improved by Figure6.2b depicts the energy band diagrams of CMOSFET and JLVTFET in the OFF-state (Vds = 1V,Vgs = 0), and it is not difficult to deduce the spacing of the conduction band from this figure. The JLVTFET's valance band in the source/channel interface was much bigger than that of the CMOSFET. Furthermore, an additional barrier height happened in the channel region for JLVTFET This is because the gate electrode in the JLVTFET was divided into three parts: the auxiliary gate (M1), the control gate (M2), and the tunnel gate (M3), and the auxiliary gate (M1) generated the extra barrier height in the OFF-state.



a)



b)

Figure 6.2 : (a) JLVTFET and CMOSFET transfer properties; (b) JLVTFET and CMOSFET trans conductance.

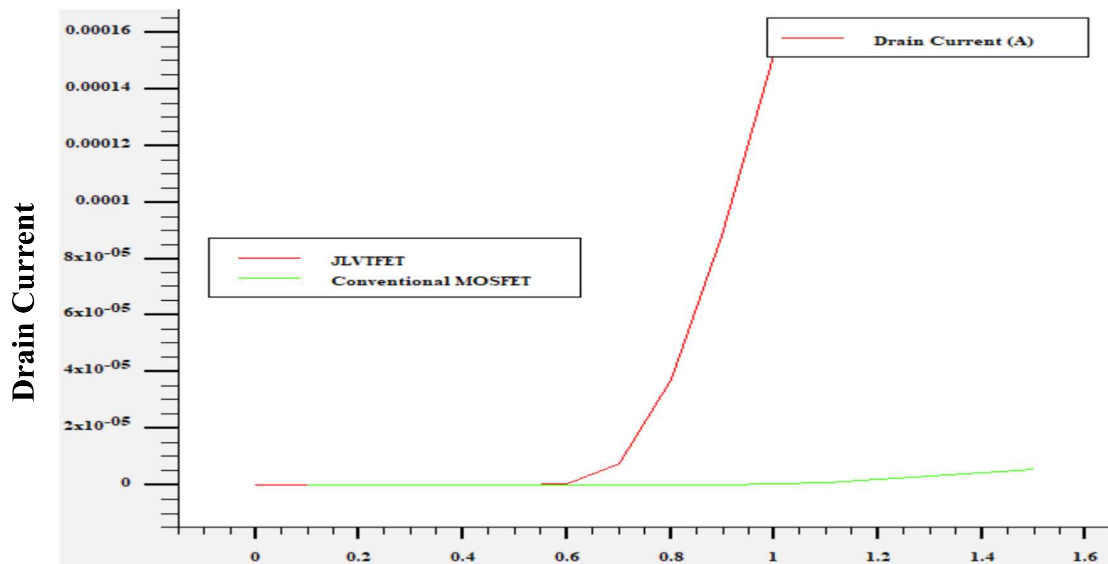


Figure 8 : The transfer characteristics of CMOSFET and JVTFET

9.3 Effect of device parameter on the transfer characteristics

In Figure 9, the effect of source doping concentration on transfer characteristics is depicted. It is evident from the figure that the ON-state current of the DMGE-HJLTFET decreases as the source doping concentration increases. Specifically, the ON-state current of the DMGE-HJLTFET decreases from 5.46 x 10^-4 A/μm to 3.61 x 10^-4 A/μm when the source doping concentration increases from 1 x 10^17 cm^-3 to 1 x 10^19 cm^-3. This can be attributed to the uniform N-type doping in the source, channel, and drain regions, which forms a P+-I-N+ structure with appropriate workfunction for PG(polar gate) and CG(control gate). Consequently, the hole concentration formed by polarization in the source region decreases with the increase in the lightly doped source's N-type concentration. Since the tunnel process involves the hole from the source valence band to the channel conduction band, increasing the source doping concentration leads to a decrease in the ON-state current. Additionally, the OFF-state current of the DMGE-HJLTFET consistently remains at the order of 10^-17 A/μm. In Figure 9, the variation of the ON-state current and the OFF-state current with the increase in source doping concentration is shown. It is evident that the OFF-state current is minimal when the source doping concentration is 5 x 10^17 cm^-3. Consequently, the ratio of I_{on}/I_{off} comes up to its maximum at this doping concentration, as shown in the inserted small graph in Figure 6.4. Therefore, a source doping concentration of 5 x 10^17 cm^-3 is selected to achieve the maximum I_{on}/I_{off} value.

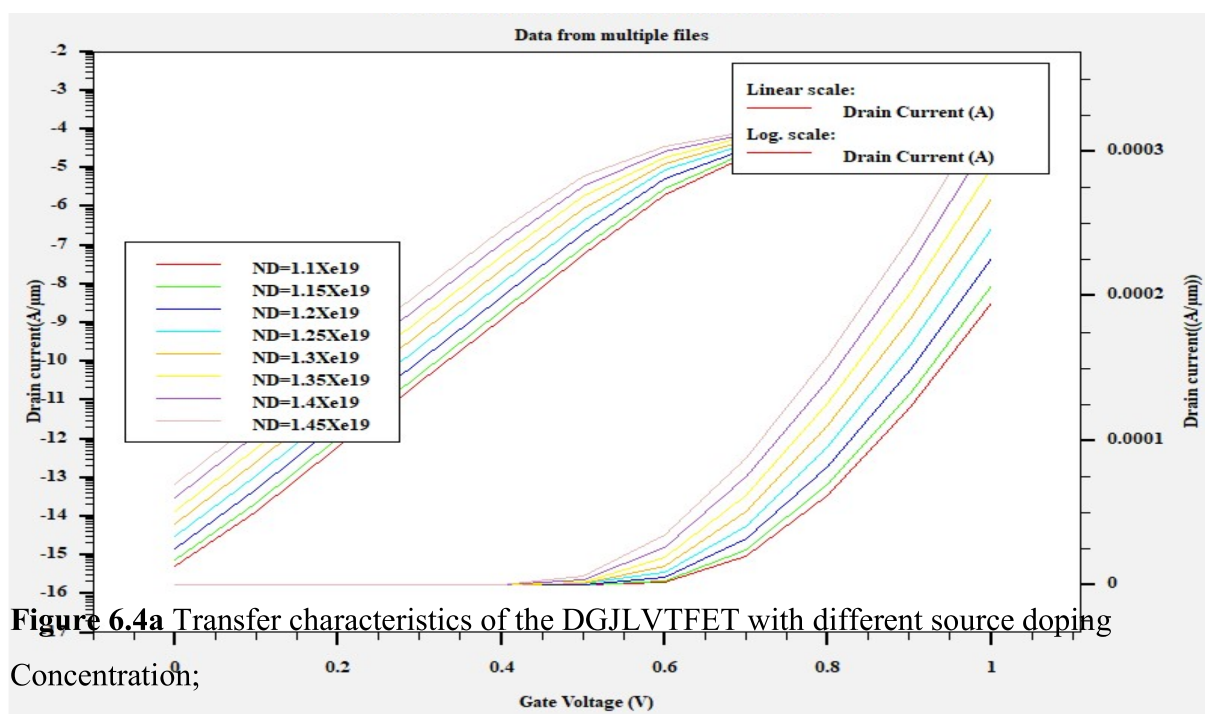


Figure 6.4a Transfer characteristics of the DGJLVTFET with different source doping Concentration;

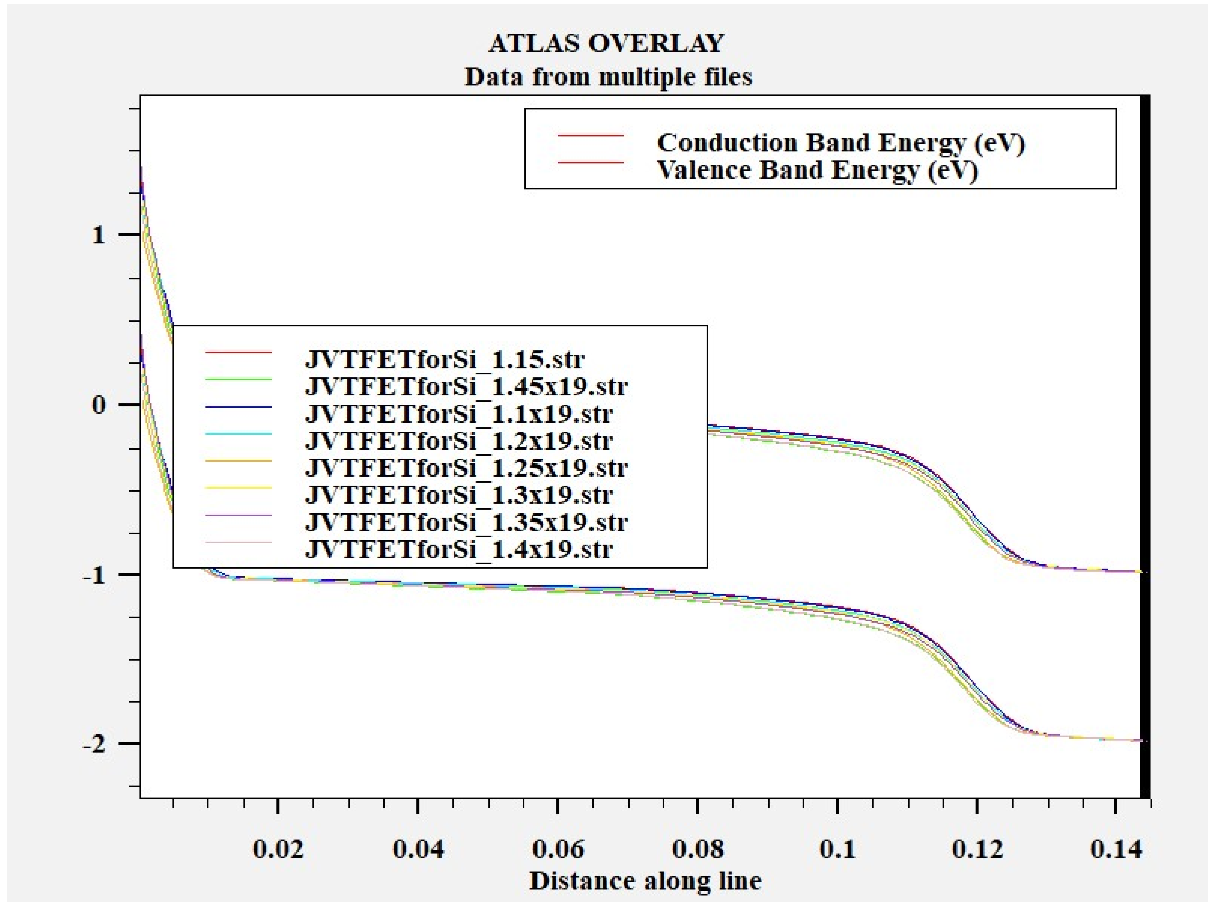
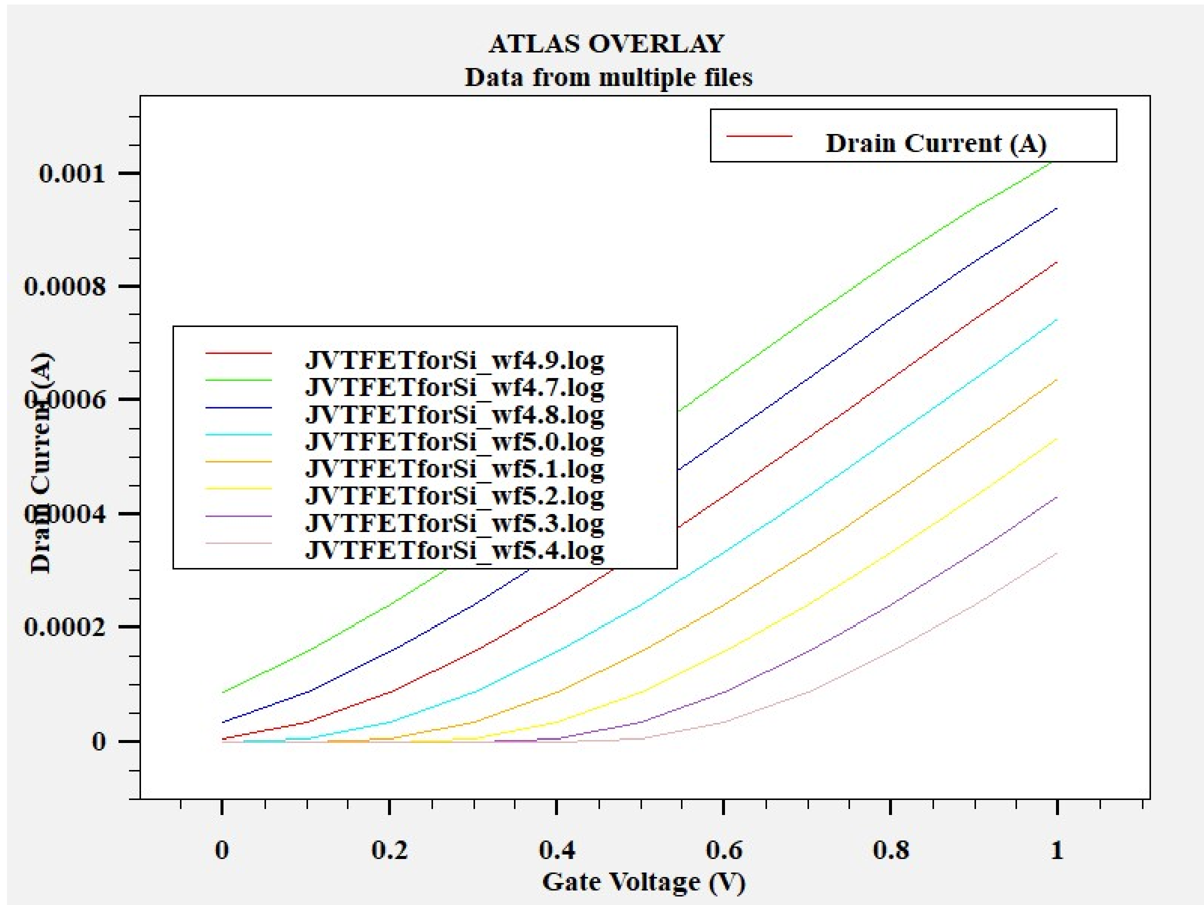


Figure 9 : the variation of energy band diagram with different doping concentration

In the previous discussion, we mentioned that the gate electrode consists of three parts: the auxiliary gate (M1), control gate (M2), and tunnel gate (M3) with respective workfunctions Φ_{M1}, Φ_{M2}, and Φ_{M3}, where $\Phi_{M1} = \Phi_{M3} < \Phi_{M2}$. Now, we will discuss the effects of these three parameters on the transfer characteristics. Figure 7a illustrates the impact of the polar gate workfunction (ΦPG) on transfer characteristics while keeping $\Phi_{M1} = \Phi_{M3} = 4.1$ eV and $\Phi_{M2} = 4.4$ eV. As observed from Figure 9a, the ON-state current of the DMGE-HJLTFET increases, and the OFF-state current remains at the order of 10^-17 A/µm with an increase in Φ_{PG}. Therefore, selecting an appropriate value for Φ_{PG} is crucial in achieving a higher ON-state current and a lower OFF-state current simultaneously. This is because Φ_{PG} significantly influences the formation of polarization charge in the source region. The amount of polarization charge increases with the polar gate workfunction, resulting in a variation in the energy band, as depicted in Figure 9 b. Figure 9b demonstrates the change in the energy band with different Φ_{PG}. As Φ_{PG} increases, the position of the conduction band and valence band in the source region becomes higher, enhancing the effective tunneling area of the channel-source interface.

Consequently, the ON-state current of the DGJVTFET increases with an increase in Φ_{PG}. Thus, Figure 9b further supports the conclusion drawn from Figure 9a.



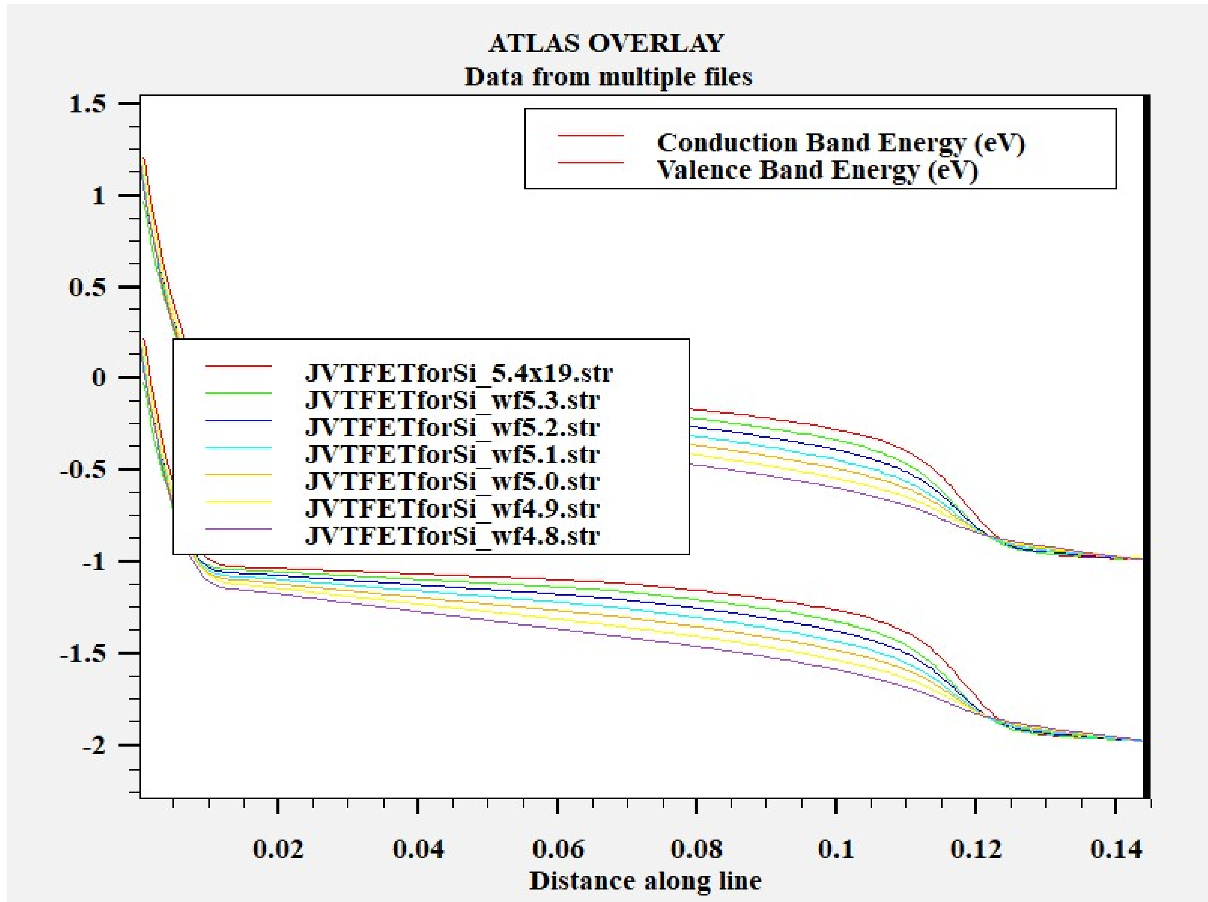


*Figure 10: (**a**) Transfer characteristics of the DGVTFET with different gate work function (Φ_{PG}); (**b**) the variation of energy band diagram with different gate workfunction (Φ_{PG}).*

The research titled "Optimization of Double Gate Junctionless Field Effect Transistor for Low Memory Application Using T-CAD Tools" aimed to optimize the performance of a double gate junctionless field effect transistor (DG-JLTFET) for low memory applications. The study utilized T-CAD tools to analyze and improve the device characteristics, leading to several noteworthy conclusions.

10. Conclusion and recommendation

Firstly, the impact of source doping concentration on the transfer characteristics of the DG-JLTFET was investigated. It was observed that the ON-state current of the device decreased with an increase in source doping concentration. This behavior could be attributed to the uniform N-type doping in the source, channel, and drain regions. The uniform doping resulted in a decrease in the hole concentration formed by polarization in the source region. Consequently, the tunneling process from the source valence band to the channel conduction

band was hindered, leading to a decrease in the ON-state current. The research determined that an optimal source doping concentration of 5 x 10^17 cm^-3 yielded the maximum Ion/Ioff ratio.

Secondly, the study examined the influence of the polar gate workfunction (Φ_{PG}) on the transfer characteristics of the DG-JLVTFET. It was found that Φ_{PG} had a significant impact on the performance of the device. As Φ_{PG} increased, the ON-state current of the DG-JLTFET also increased, while the OFF-state current remained at the order of 10^-17 A/µm. This behavior was attributed to the effect of Φ_{PG} on the formation of polarization charge in the source region. With an increase in Φ_{PG}, the amount of polarization charge increased, resulting in a variation in the energy band. This variation caused the position of the conduction band and valence band in the source region to become higher. Consequently, the effective tunneling area of the channel-source interface was boosted, leading to an increase in the ON-state current. The research emphasized the importance of selecting an appropriate value for Φ_{PG} to achieve higher ON-state current and lower OFF-state current simultaneously.

The findings of this research have significant implications for the optimization of DG-JLTFETs for low memory applications. By carefully adjusting the source doping concentration and polar gate workfunction, it is possible to enhance the performance of the device and achieve the desired characteristics for low-power memory applications. The research contributes to the advancement and development of DG-JLTFET technology, providing valuable insights for future memory device designs.

Furthermore, the utilization of T-CAD tools in this research highlights the importance of computer-aided design tools in the optimization process. T-CAD tools enable researchers to simulate and analyze the behavior of complex electronic devices, providing a valuable platform for exploring different design parameters and optimizing device performance. The research showcases the effectiveness of T-CAD tools in understanding the underlying physics and optimizing the performance of DG-JLTFETs.
Finally the optimization of DG-JLTFETs for low memory applications is a promising avenue of research. Through the careful adjustment of source doping concentration and polar gate workfunction, it is possible to enhance the performance of these devices, achieving higher ON-state current and lower OFF-state current simultaneously. The findings of this research contribute to the advancement of DG-JLTFET technology, providing valuable insights for the

development of future low-power memory devices. The utilization of T-CAD tools further emphasizes the importance of computer-aided design in the optimization process.

11. References

1.Choi,W.Y.; Park, B.-G.; Lee, J.D.; Liu, T.-J.K. Tunneling Field-E_ect Transistors (TFETs)With Subthreshold Swing (SS) Less Than 60 mV/dec. IEEE Electron. Device Lett. 2007, 28, 743–745. [CrossRef]

2. Kim, J.H.; Kim, S.; Park, B.-G. Double-Gate TFET with Vertical Channel Sandwiched by Lightly Doped Si. IEEE Trans. Electron. Devices 2019, 66, 1656–1661. [CrossRef]

3. Yang, Z. Tunnel Field-E_ect Transistor with an L-Shaped Gate. IEEE Electron. Device Lett. 2016, 37, 1. [CrossRef]

4. Kim, J.H.; Kim, S.; Park, B.-G. Symmetric U-Shaped Gate Tunnel Field-Effect Transistor. IEEE Trans. Electron. Devices 2017, 64, 1343–1349.

5. Nam, H.; Cho, M.H.; Shin, C. Symmetric tunnel field-effect transistor (S-TFET). Curr. Appl. Phys. 2015, 15, 71–77. [CrossRef]

6. Jiang, Z.; Zhuang, Y.; Li, C.;Wang, P. Dual Sources U-shape Gate Tunnel FETs with High On-current and Steep SS. In Proceedings of the 2016 16th International Workshop on Junction Technology (IWJT), Shanghai, China, 9–10 May 2015; pp. 25–27.

7. Sola,W.; Sangsig, K. Covered Source–Channel Tunnel Field-E_ect Transistors with Trench Gate Structures. IEEE Trans. Nanotechnol. 2018, 18, 114–118.

8. Li,W.; Liu, H.;Wang, S.; Chen, S.; Yang, Z. Design of High Performance Si/SiGe Heterojunction Tunneling FETs with a T-Shaped Gate. Nanoscale Res. Lett. 2017, 12, 198. [CrossRef] [PubMed]

9. Szabo, A.; Koester, S.J.; Luisier, M. Ab-Initio Simulation of van der Waals MoTe2–SnS2. Heterotunneling FETs for Low-Power Electronics. IEEE Electron. Device Lett. 2015, 36, 514–516. [CrossRef]

10. Raad, B.R.; Tirkey, S.; Sharma, D.; Kondekar, P. A New Design Approach of Dopingless Tunnel FET for Enhancement of Device Characteristics. IEEE Trans. Electron. Devices 2017, 64, 1830–1836. [CrossRef]

11. Lilienfeld, J. Method and Apparatus for Controlling Electric Currents. U.S. Patent 1,745,175, 28 January 1930.

12. Colinge, J.P.; Lee, C.W.; Afzalian, A.; Akhavan, N.D.; Yan, R.; Ferain, I.; Razavi, P.; O'neill, B.; Blake, A.; White, M.; et al. Nanowire transistors without junctions. Nat. Nanotechnol. **2010**, 5, 225.

13. Han, M.H.; Chang, C.Y.; Chen, H.B.; Cheng, Y.C.; Wu, Y.C. Device and circuit performance estimation of junctionless bulk FinFETs. IEEE Trans. Electron. Devices **2013**, 60, 1807–1813.
14. Priya, A.; Rai, S.; Mishra, R.A. Comparative analysis of junctionless bulk and SOI/SON FinFET. In Proceedings of the 2017 4th International Conference on Power, Control & Embedded Systems (ICPCES), Allahabad, India , 9–11 March 2017; pp. 1–4.
15. Bharathi, R.; Durga, G.; Kumar, N.V.; Nagarajan, K.; Srinivasan, R. Performance optimization of bulk junctionless FinFETs through work function engineering. In Proceedings of the 2014 International Conference on Circuits, Power and Computing Technologies [ICCPCT-2014], Nagercoil, India, 20–21 March 2014; pp. 1291–1295.
16. Bousari, N.B.; Anvarifard, M.K.; Haji-Nasiri, S. Improving the Electrical Characteristics of Nanoscale Triple-Gate Junctionless FinFET Using Gate Oxide Engineering. AEU Int. J. Electron. Commun. **2019**, 108, 226–234.
17. Kaundal, S.; Rana, A.K. Threshold voltage modeling for a Gaussian-doped junctionless FinFET. J. Comput. Electron. **2019**, 18, 83–90.
18. Djeffal, F.; Ferhati, H.; Bentrcia, T. Improved analog and RF performances of gate-all-around junctionless MOSFET with drain and source extensions. Superlattices Microstruct. **2016**, 90, 132–140.
19. Sharma, M.; Gupta, M.; Narang, R.; Saxena, M. Investigation of Gate All Around Junctionless Nanowire Transistor with Arbitrary Polygonal Cross Section. In Proceedings of the 2018 4th International Conference on Devices, Circuits and Systems (ICDCS), Coimbatore, India, 16–17 March 2018; pp. 159–163.
20. Nobrega, R.; Fonseca, Y.; A Costa, R.; Duarte, U. Comparative Study on the Performance of Silicon and III-V Nanowire Gate-All-Around Field-Effect Transistors for Different Gate Oxides. In Proceedings of the XIII Workshop on Semiconductors and Micro & Nano Technology, São Bernardo do Campo, Brazil, 19–20 April 2018.
21. Sharma, S. An Extensive Evaluation of Futuristic Gate All Around Junctionless Nanowire MOSFET Using Numerical Simulation. Int. J. Res. Appl. Sci. Eng. Technol. **2017**, V, 1974–1979. doi:10.22214/ijraset.2017.8279.
22. Lime, F.; Ávila-Herrera, F.; Cerdeira, A.; Iñiguez, B. A compact explicit DC model for short channel Gate-All-Around junctionless MOSFETs. Solid State Electron. **2017**, 131, 24–29.

23. Scarlet, S.P.; Srinivasan, R. Impact of Doping and Spacer on the Performance of Bulk Planar Junctionless devices. In Proceedings of the 2018 4th International Conference on Electrical Energy Systems (ICEES), Chennai, India, 7–9 February 2018; pp. 267–273.
24. Ramarao, G.; Ghosekar, I.C.; Patil, G.C. Dual-k HfO 2 Spacer Bulk Planar Junctionless Transistor for Sub-30 nm Low Power CMOS. In Proceedings of the 2017 14th IEEE India Council International Conference (INDICON), Roorkee, India, 15–17 December 2017; pp. 1–4.
25. Ehteshamuddin, M.; Loan, S.A.; Rafat, M. Planar junctionless silicon-on-insulator transistor with buried metal layer. IEEE Electron. Device Lett. **2018**, 39, 799–802.
26. Adnan, M.M.R.; Khosru, Q.D.M. A Simple Analytical Model of Threshold Voltage for P-Channel Double Gate Junctionless Transistor. In Proceedings of the 2018 IEEE International Conference on Electron, Devices and Solid State Circuits (EDSSC), Shenzhen, China, 6–8 June 2018; pp. 1–5.
27. Bora, N.; Das, P.; Subadar, R. An Analytical Universal Model for Symmetric Double Gate Junctionless Transistors. J. Nano Electron. Phys. **2016**, 8, 02003-1.
28. Yesayan, A.; Prégaldiny, F.; Sallese, J.M. Explicit drain current model of junctionless double-gate field-effect transistors. Solid State Electron. **2013**, 89, 134–138.
29. Chen, Z.; Xiao, Y.; Tang, M.; Xiong, Y.; Huang, J.; Li, J.; Gu, X.; Zhou, Y. Surface-potential-based drain current model for long-channel junctionless double-gate MOSFETs. IEEE Trans. Electron. Devices **2012**, 59, 3292–3298.
30. Bhuvaneshwari, Y.; Kranti, A. Extraction of mobility and degradation coefficients in double gate junctionless transistors. Semicond. Sci. Technol. **2017**, 32, 125011.
31. Baidya, A.; Baishya, S.; Lenka, T.R. Impact of thin high-k dielectrics and gate metals on RF characteristics of 3D double gate junctionless transistor. Mater. Sci. Semicond. Process. **2017**, 71, 413–420.
32. Kang, T.K.; Peng, Y.H. Drain Conductance Oscillations in Poly-Si Junctionless Nanowire Thin-Film Transistors. IEEE Trans. Electron. Devices **2018**, 66, 451–456.
33. Rahi, S.B.; Asthana, P.; Gupta, S. Heterogate junctionless tunnel field-effect transistor: future of low-power devices. J. Comput. Electron. **2017**, 16, 30–38.
34. Ghosh, B.; Bal, P.; Mondal, P. A junctionless tunnel field effect transistor with low subthreshold slope. J. Comput. Electron. 2013, 12, 428–436.
35. Asthana, P.K.; Goswami, Y.; Ghosh, B. A novel sub 20nm single gate tunnel field effect transistor with intrinsic channel for ultra-low power applications. J. Semicond. **2016**, 37, 054002.

36. S. Migita, Y. Morita, T. Matsukawa, M. Masahara, and Hiroyuki, “Experimental demonstration of ultrashort-channel (3 nm) junctionless FETs utilizing atomically sharp v-grooves on SOI,” *IEEE trans. on Nanotech.*, vol. 13, no. 2, pp. 208-215, Mar. 2014.
37. J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O’Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, “Nanowire transistors without junctions,” *Nature Nanotechnol.*, vol. 5, no. 3, pp. 225–229, Mar. 2010.