Design, Modeling and Performance Analysis of Smart Transformer for Distribution System

Yalisho Girma Loaena

A Dissertation Submitted to

The department of Electrical Power and Control Engineering

School of Electrical Engineering and Computing

Presented in Fulfillment of the Requirement for the Degree of Doctor of Philosophy in Electrical Engineering

Office of Graduate Studies

Adama Science and Technology University

Nov, 2023

Adama, Ethiopia

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Supervisor(s)

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Declaration

I hereby declare that this Dissertation entitled "Design, Modeling and Performance Analysis of Smart Transformer for Distribution System" is my original work. That is, it has not been submitted for the award of any academic degree, diploma or certificate in any other university. All sources of materials used for this thesis have been duly acknowledged through appropriate citations.

_____	_____	_____
Name of student	Signature	Date

Recommendation

We, the supervisor(s) of this dissertation, hereby certify that we have read and revised the dissertation entitled "Design, Modeling and Performance Analysis of Smart Transformer for Distribution System" prepared under our guidance by Yalisho Girma Loaena submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Electrical Engineering. Therefore, we recommend the submission of the dissertation to the department for further review and defense.

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Co-Supervisor	Signature	Date

Approval of Ph.D. Dissertation

We hereby certify that the recommendations and suggestions made by the board of examiners are appropriately incorporated into the final version of the dissertation entitled "Design, Modeling and Performance Analysis of Smart Transformer for Distribution System" by Yalisho Girma Loaena**.**

Major Supervisor	Signature	Date
Co-Supervisor	Signature	Date

We, the undersigned, members of the Board of Examiners of the dissertation open defense by Yalisho Girma Loaena have read and evaluated the dissertation entitled "Design, Modeling and Performance Analysis of Smart Transformer for Distribution System " and examined the candidate during open defense. This is, therefore, to certify that the dissertation is accepted for partial fulfillment of the requirement of the degree of Doctor of Philosophy in Electrical Engineering.

Chair Person	Signature	Date
Dr. Mengesha Mamo		12 Dec 2023
Internal Examiner 1	Signature	Date
Internal Examiner 2	Signature	Date
Prof Innocent E Davidson		10 Dec 2023
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Finally, approval and acceptance of the dissertation is contingent upon submission of its final copy to the Office of Postgraduate Studies (OPGS) through the candidate's Department Graduate Council (DGC) and School Graduate Committee (SGC).

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Dedicated to My enlightened Father

Githa Danna (Gramashe Loaena)

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List of Acronym and Abbreviation

AAC	All Aluminium Conductor
AC	Alternating Current
AGC	Automatic Generation Control
ANFIS	Adaptive-Neuro_Fuzzy Inference System
APOD	Alternate Phase Opposition Disposition
AQAB	Asymmetric Quadruple Active Bridge
BESS	Battery Energy Storage System
BPL	Broad band over Power line
CHB:	Cascaded Half Bridge
CT	Conventional Transformer
CST	Composite Smart Transformer
DAB	Dual Active Bridge
DC	Direct Current
DERs	Distributed Energy Resources
DPDS	Dual Primary Dual Secondary
EHV	Extra High voltage
EPRI	Electric Power Research Institute
FACTS	Flexible Alternating Current Transmission System
FBSM	Full Bridge Sub-Module
FC	Flying Capacitor
FIS	Fuzzy Inference System
FRD	Fast Recovery Diode
FREEDM	Future Renewable Electric Energy Development and Management
FWD	Freewheeling Diode
GMR	Geometric Mean Radius
GSE	Generalized Steinmetz Equation
GTO	Gate Turnover Thyristor
HBSM	Half Bridge Sub-Module

HV	High Voltage
HVDC	High Voltage Direct Current
HAN	Home Area Network
ICT	Information Communication Technology
IGSE	Improved Generalized Steinmetz Equation
LFC	Load Frequency Control
IGBT	Insulated Gate Bipolar Transistor
IPOP	Input parallel Output Parallel
ISOP	Input Series Output Parallel
ISOS	Input Series Output Series
LS-PWM	Level Shift Pulse Width Modulation
LV	Low Voltage
Mi	Modulation Index
MAB	Multiple Active Bridge
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
MMC	Modular Multilevel Converter
MV	Medium Voltage
NAN	Neighbour Area network
NPC	Neutral Point Clamped
OSE	Original Steinmetz Equation
PCC	Point of Common Coupling
PD	Phase Disposion
PDS	Power Distribution System
PHEV	Plug-in Hybrid Electric Vehicle
PI	Proportional and Integral
PID	Proportional, Integral and Derivative
PLC	Programmable logic controller, Power line communication
PLECS	Peace wise Linear Electronics Circuit System
PMU	Phasor Measurement Unit

POD	Phase Opposition Disposition
PS-PWM	Phase shift Pulse Width Modulation
PV	Photovoltaic
QAB	Quadruple Active Bridge
SAPF	Shunt Active Power Filter
SQAB	Symmetric Quadruple Active Bridge
SMAB	Symmetric Multiple Active Bridge
SRC	Series Resonant Converter
ST	Smart Transformer
THD	Total Harmonic Distortion
VOC	Voltage Oriented Control
WAN	Wide Area network
WBG	Wide Band Gap
WiMax	Worldwide Interoperability for Microwave Access

Abstract

The changing architecture of electric power grid from centralized to decentralized form by integration of distributed energy resources (DERs) to ensure a reliable, efficient and environmentally friendly power supply to customers is becoming an opportunity and challenge for power companies. The decentralized electric power grid, poses many challenges to a hundreds of years old conventional transformers as it is a unidirectional power system infrastructure which doesn't compensate for harmonics and reactive power. Moreover, the conventional transformers in distribution system are bulky in size and volume; use a mechanical tap changer, which toggles between different tap positions many times per day, reducing life time of transformer by wear and tear. It doesn't allow integration of micro grids without investing on additional power converter equipment. The aforementioned short comings of conventional transformers are overcome by emerging technology known as a smart transformer. In this dissertation work, design, modeling and analysis of a three stage multiport smart transformer (ST) based on modular multilevel converter (MMC) is presented in Simulink/PLECS simulation platform using different controllers, modulation techniques and converter configurations. In addition, integration of smart transformer (ST) in to the existing feeder model of ArbaMinch distribution system containing 72 distribution transformers has been done and its impact on voltage regulation, loss minimization and power quality (PQ) improvement has been assessed. Observations of simulation result showed that Fuzzy Inference System (FIS) and Adaptive-Neuro-Fuzzy Inference System (ANFIS) controllers yield better output than Proportional-Integral (PI) controller for front stage of ST. Simulation result of Input-Series-Output-Parallel Dual Active Bridge (DAB-ISOP) configuration for DC-DC stage proved voltage sharing at input side and current sharing at output side reducing device voltage and current stress and increasing availability. The MMC topology for back-end converter yields a reduced voltage total harmonic reduction (THD) value (3.8%), higher efficiency (96.7%) and reduced current stress (61%) than its cascaded H bridge (CHB) counterpart having voltage THD of 13.7% and efficiency of 83% for the same sub-module (SM) used. It has been observed from the simulation result that the maximum voltage drop in the feeder model without ST integration is 781V with voltage regulation of 9.9%. However, the maximum voltage drop after integration of an ST model is reduced to 444V with voltage regulation of 5.4% (improvement by 4.5%). The line loss without ST integration is 1096.7kW, which is reduced to 823.2kW when ST is integrated in to the feeder model (power loss reduction by 273.5 kW).

Key words: Distribution system, Smart transformer, Conventional transformer, Modular multilevel converter.

CHAPTER ONE
INTRODUCTION

1.1 Background of the study

The conventional electric power grid is among the most sophisticated and complex engineering system of the 20th century. It contains energy infrastructures such as centralized large generating plants, transmission system, distribution system, loads and some local and limited automatic controls such as automatic governor control (AGC) and load frequency control (LFC) to ensure predictable behavior of generators and transmission systems. The generating plants can be powered by hydropower, nuclear power, fossil fuel wind power, thermal power and located in different geographical regions far apart from the consumers. The generating plants are interconnected to form a synchronous grid so that loss of one generating plant does not result in total loss of power to the loads, thus increasing the reliability of the power system and facilitating the maintenance of generators without shutting down the loads. The transmission system contains components such as transmission substations, transmission tower, transmission lines, protection devices, transformers and voltage regulating devices that are designed to handle high voltage (HV) or extra high voltage (EHV) to transfer a bulk power from generating stations to transmission systems and then to distribution systems. The distribution system feeding load is a part of the power grid which contains major components such as step down transformers, the medium voltage and low voltage distribution lines, distribution substation, voltage regulators, high voltage and low voltage switchgear. The classical power grid mentioned so far is very extensive, but is almost entirely passive with little communication and only limited local controls. Except for very large loads such as steelworks or in aluminum smelters, there is no real-time monitoring of either the voltage being offered to a load or the current being drawn by it. Other than supply of demanded load energy, there is little interaction between the load and the power system.

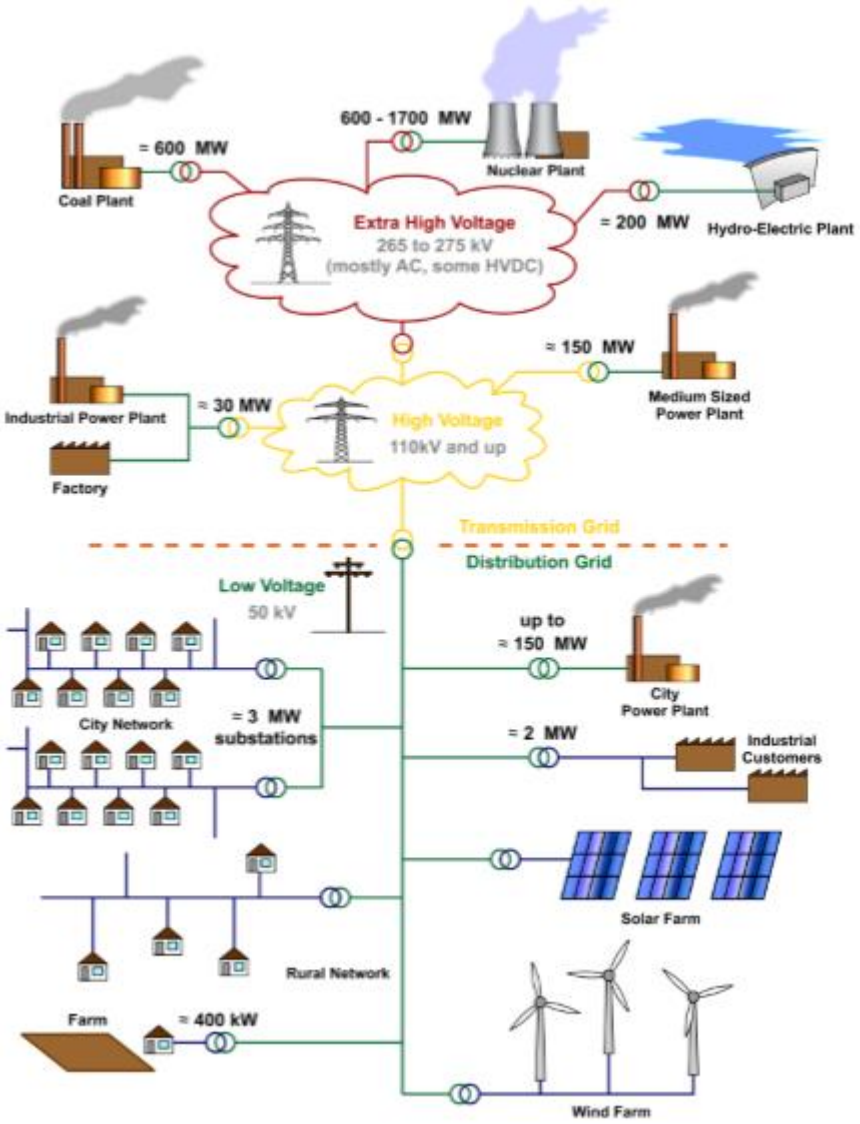

Fig1. 1 Electric power system structure [15]

1.2 Trends in Electric Power Grid

The present-day electric power grid has served well in providing unidirectional power supply to the users in seamless ways. However, the electric power grid in general and the power distribution in particular are currently undergoing significant changes in the way of generation, transmission, distribution and consumption because of the following major shifts in its own sector and other sectors benefiting from it.

- Fast growing demand driven by rapid growth in population, adoption of energy-efficient technologies, fast changing economic conditions, extensive electrification, and increasing mass market potential availability for plug-in hybrid electric vehicles.

- Diversified generation mix including resources such as renewable, nuclear, oil and natural gas, and coal and changing location mix such as centralized, distributed, and off-shore, in the Nation's generation portfolio driven by technology, market, and policy developments.
- Rapidly changing variability of generation and load patterns, including the integration of variable renewable energy sources, more active participation of consumers, and the implementation and accommodation of new technologies and techniques.
- Growing risks to electric infrastructure due to more frequent and intense extreme weather events, increases in cyber vulnerabilities and threats, physical attacks, and increasing interdependencies with natural gas and water infrastructure.
- Aging and rapidly becoming outdated electricity infrastructure in view of the other changes happening system-wide, causing greater vulnerabilities.

Adoption of real time monitoring and control, advanced sensors, communication system, advanced data analytics and cyber security are some of the efforts under implementation to address the above changes in the power grid land scape. Use of these technological solutions has improved the visibility and controllability of the system, leading to greater reliability, efficiency, flexibility, security, and resilience. However, along with the implementation of the above technologies, upgrading the fundamental hardware components and systems that make up the electric delivery infrastructure is mandatory to address the full spectrum of advances and functionalities needed. Some of the evolutions in the upgrades of the hardware components of electric power systems include increased penetration of distributed energy resources (DERs), adoption of smart power substation (SPSS) and smart transformers (ST) which enhances the system flexibility, adaptability, security, and resiliency (US DOE,2020)

Evolution of the electric power system caused changes in the landscape of generation and load-side technologies, which in turn result in fundamental altering of the electric power flow and physical phenomena that the grid was designed to accommodate. For instance, high penetration of distributed energy resources (DERs) causes large-scale conventional generation systems such as coal-fueled power plants to operate more in more flexible manner than how they were designed initially to operate (i.e., purely base-load). Increased penetration of distributed generation system (DGS), integration of information communication technology (ICT), usage of advanced sensing , measuring, monitoring and control technologies have transformed the classical electric power grid in to a smart grid having features of self-healing, higher efficiency, reliability, resilience, low carbon emission and greater customer participation.(A. Huang, M, 2011)

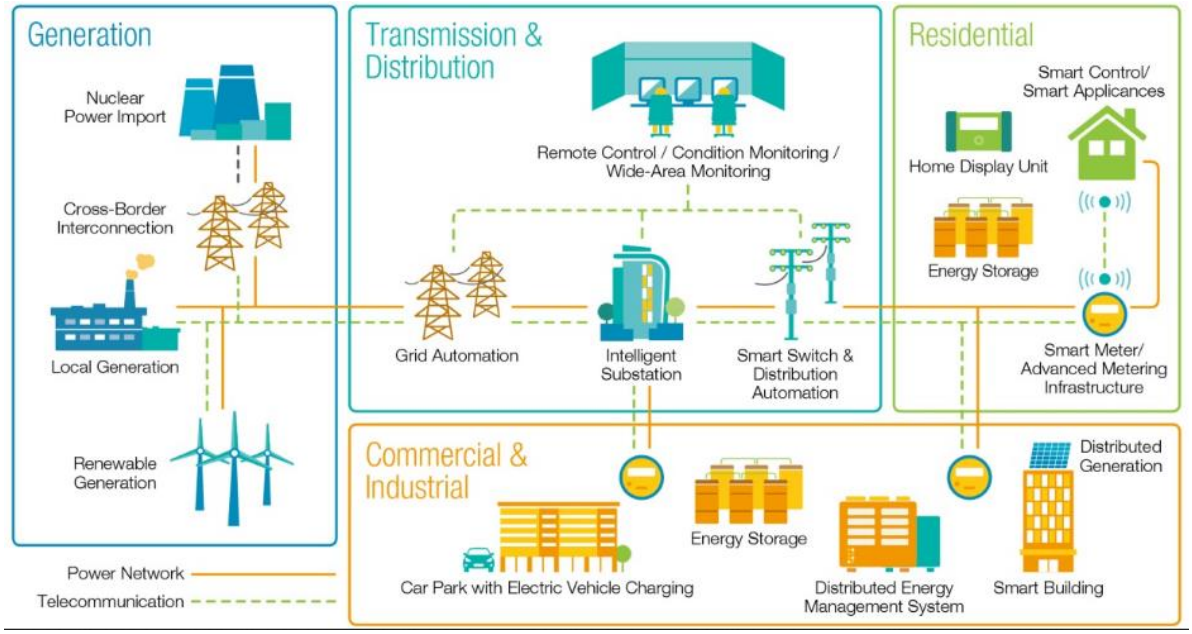

Fig1. 2 Smart grid [6]

1.3 Components of Smart Grid

A smart grid also known as intelligent electric grid is a self-sustainable electricity supply network using ICT technology for control, analysis and monitoring within the supply chain to ensure efficient and reliable operation. To achieve its envisioned targets, smart grid employs wide varieties of advanced technologies in addition to the legacy electricity grid (generation, transmission, and distribution) which are grouped under the following key groups [6]:

- **Integrated Information Communication System**: This can be programmable logic controller (PLC), wireless networks (both short range and long range capacity) such as wide area network (WAN), neighbor area network (NAN), home area network (HAN), WiMAX, 3G/4G cellular wireless, ZigBee, wired network such as broad band over power line (BPL) and optical fiber. The choice among these communication technologies depends on many factors such as security, easy deployment, latency, data carrying capacity, coverage capability, interoperability, reliability, geographical location, availability and cost

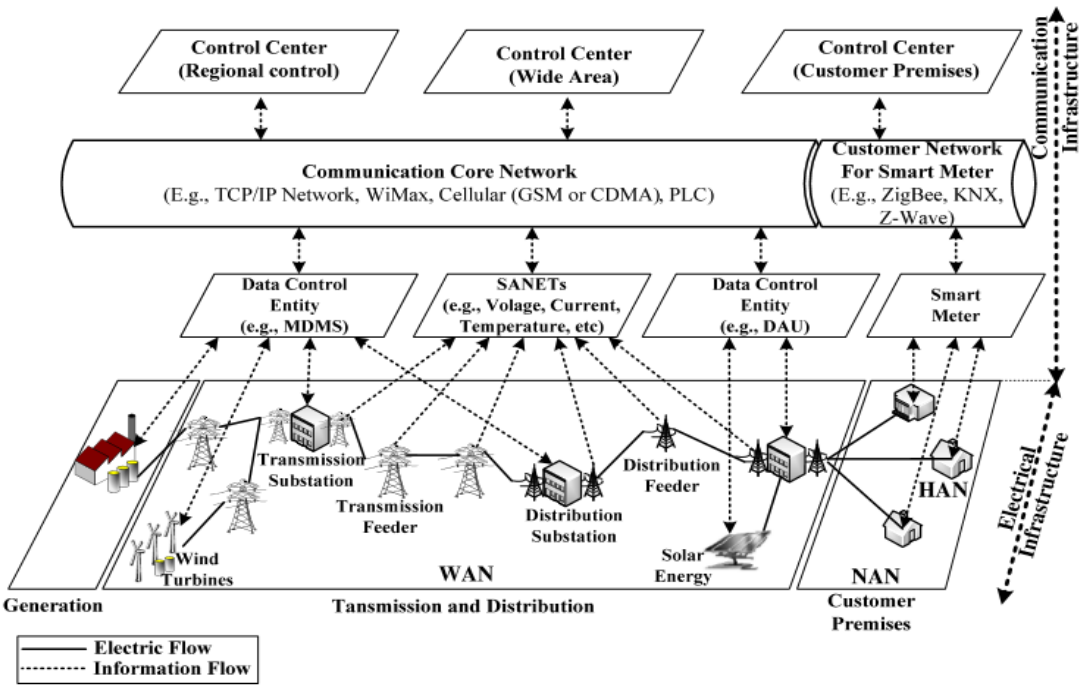

Fig1. 3 **Smart grid communication network (**Nipendra Kayastha, etal., 2014)

- **Smart Power Meters:** It is also referred to as advanced metering infrastructure (AMI).The smart power meters provide bi-directional communication between power providers and the end user consumers to automate billing data collections, detect device failures and dispatch repair crews to the exact location much faster.

Fig1. 4 Smart power meter

- **Intelligent Appliances:** such as automated space heaters, air conditioners, plug-in hybrid electric vehicles (PHEV), etc. which has smart sensors capable to make decisions based

on customer pre-set preferences to consume energy. This leads to going a path towards reducing peak loads which might have an impact on electricity generation costs.

- **Phasor Measurement Units (PMU):** This advanced measuring instrument is used to measure the electrical waves on an electricity grid using a common time source for synchronization. Synchronized real-time measurements of multiple remote measurement points on the grid are realized by the time synchronizer in PMU.
- **Smart Substations:** Monitoring and control of critical and non-critical operational data such as power factor performance, transformer status, power status, breaker status, security, etc. Voltage transformation at several times in many locations for providing safe and reliable delivery of energy is also among the several operations in electrical substations. Smart substations are also necessary for splitting the path of electricity flow into many directions, in addition to performing equipment state checking. Substations require large and very expensive equipment to operate, including transformers, switches, capacitor banks, circuit breakers, a network protected relays and several others.
- **Modern grid infrastructures:** these can be super conducting cables, flexible alternating current technology system (FACTS**),** high voltage DC (HVDC) transmission which is capable of providing power transmission over long distance,, automated monitoring and analysis tools to enable faults detection by itself.

It also comprises large intermittent renewable power supply, distributed generations, storage devices that can be connected at the point of end users.

- **Advanced Control and Automation systems**: these can be analytical tools with software algorithm, computers and intelligent agents to monitor, collect data from sensors for making rapid diagnosis and precise solutions for specific grid disruption

1.4 Power Distribution System

The power distribution system (PDS) is a part of electric power grid which is connected to industrial loads, residential loads and commercial loads located at different premises in the distribution grid catchment. From customer point of view, PDS operator has to provide the customer loads with high energy quality and reliability, defined by the local and global standards. The conventional power distribution system has the following major elements: Medium voltage (MV) grid, where industrial high power loads are connected, Low voltage (LV) grid, where industrial, residential and commercial loads characterized by low power are

connected, distribution transformers which interconnect the MV/LV grids and allow exchange of energy between them (A. J. Aristizabal et'al, 2016; I. P. and E. Society, 2015)

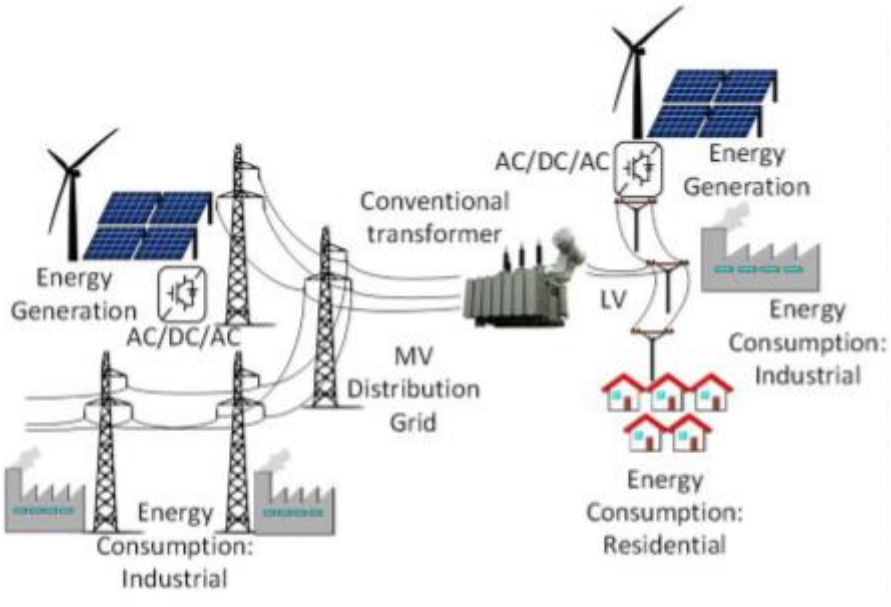

Fig1. 5 Conventional power distribution system

In comparison to classical power distribution system, the modern PDS also known as DGS includes additional distributed energy resources (DERs) such as PV power plants, wind turbines, energy storages, plug-in hybrid electric vehicle (PHEV), as shown in Fig.1.6. These distributed grid infrastructures are connected to the grid nodes through power electronics enabling technology. The vital and indispensable element of both classical PDS and DGS is the transformer. It is hard to think the roles of conventional transformers in power transmission and distribution networks for stepping up, stepping down, regulating voltages and keeping the high voltage equipment side electrically isolated from the low voltage equipment side. Although the conventional transformer is efficient and rugged, the dynamically changing architecture of power system network due to integration distributed energy resources (DERs) and information communication technology (ICT) as a result of increased concern for high reliability, power quality and low carbon footprint, pose intolerable challenges to it. Some of the challenges include requirement for bidirectional power and data flow, remote monitoring and control of equipment state, resilient operation, absence of mechanical on-load tap changing mechanism, flexible control of active and reactive powers, and flexible integration of micro grid. In addition, the conventional transformers have the following technical gaps (A. Huang et'al, 2011; W. McMurray, 1970).

• Its size and weight are bulky and heavy,

• Leakage of mineral oil in low frequency transformer (LFT) may negatively affect the environment

• Occurrence of large voltage drop under peak loading condition,

• Absence of flicker mitigation,

• Vulnerability to harmonics,

• Performance degradation under presence of DC-offset load unbalances,

• Limitations to convert single-phase service to three-phase to power three phase loads,

• Absence of energy-storage systems

• Propagation of unwanted voltage characteristics (e.g. voltage sags, harmonics) from low voltage (LV) side to upstream high voltage (HV) side or vice versa,

• Experience low efficiency at low loading level: low frequency distribution transformers exhibit their maximum efficiency at their nominal load; however the distribution transformer's average load is by far below their nominal load.

To cope up with aforementioned shortcomings of conventional transformer, researchers started searching for a new type transformer through application of power electronics. A power electronic based transformer which fills the technical gaps of conventional power transformer with reduced volume and size requirement is known as Smart Transformer (ST) or power electronic transformer (PET)

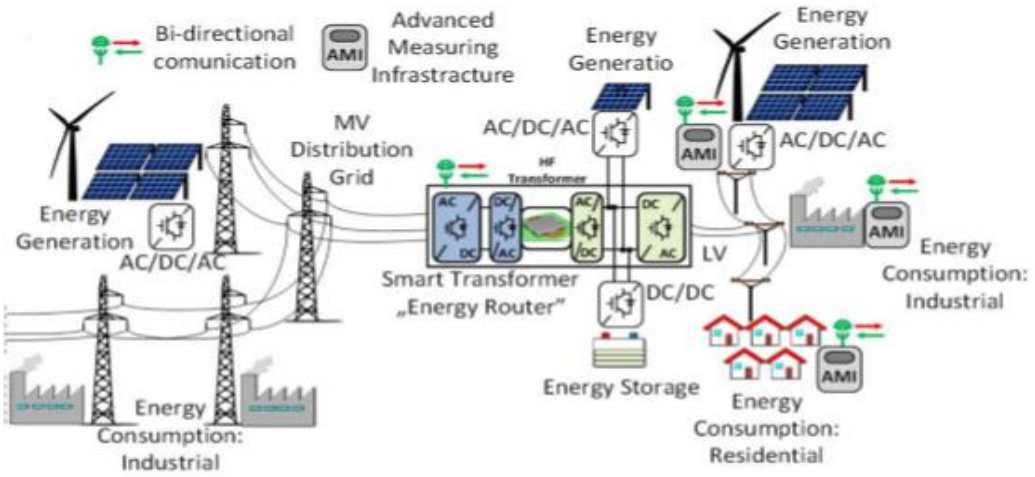

Fig1. 6 Smart transformer enabled power distribution system

1.5 Smart Transformer

A smart transformer is power electronics based intelligent equipment characterized by effective control and communication. It is considered to be the core or heart of emerging smart grid. As a vital part of the smart grid, smart transformers independently work to continuously regulate voltage and maintain contact with the smart grid in order to allow remote monitoring if needed. Also, through its effective communication, it provides information and feedback about the conditions of power supply and status of the transformers themselves. Through a mechanism of voltage optimization, the smart transformer delivers the exact amount of power that is required, and instantly responds to fluctuations within the power grid, serving as a voltage regulator to ascertain that the optimized voltage is unchanged. Smart transformers directly reduce energy losses and hence, they reduce greenhouse gas emissions as well. This feature makes them a viable option of any energy substitute for conventional transformers. In addition to reducing energy loss, by providing loads with a stable, optimal supply voltage, they also protect electrical equipment from power fluctuations, thereby, extending the life span of electrical equipment. Moreover, through their smart grid connection, smart transformers can be monitored dynamically, allowing operators to administer and manage the facilities directly during periods of power fluctuation, and helping them ensure that their power supply remains voltage optimized even when new demands come in to being (Chandan Kumar et'al, 2015).

1.6 Roles of Smart Transformer (ST) in Smart Power Distribution Grid

The smart transformers are aimed to manage and monitor power supply during time of fluctuations and ascertain that the power supply is voltage optimized during placement of new demands. The ancillary services that can be obtained by integration of smart transformer in the power distribution network are summarized as follows (L. Heinemann et;al, 2001; A. Shiri 2013).

- Isolating the source side from load side disturbances such as load transients, voltage sags, load harmonics, hence protecting the power system from such unwanted conditions.
- Maintaining unity power factor with sinusoidal currents under non-linear loads.
- Improving power quality by symmetrizing loads having same phase current even for unbalanced loads.
- Minimizing grid losses and improving the reliability of power supply.

- Provides a multiport connectivity service to utilize input or output in AC or DC form
- Protects the user load from the mains supply side disturbances.
- Avoids the requirement of mechanical tap change.
- Accommodates backup and reduces the length of outages.
- Control of voltage and frequency levels
- Provide reactive power compensation and system harmonic filtering.
- Can be used to feed control equipment or to feed DC micro grid in substations,
- Reduction of volume and weight (less footprint)

The requirement to maintain a high efficiency and high reliability while offering the aforementioned new services has a direct impact on the choice of power converter architectures of that build the smart transformer. On the basis of the number of power converters stages, the smart transformer may be classified as single stage, two stage or three stage type from which a three stage smart transformer is the most preferred as it gives the expected potential functionalities (US DOE office of Electricity, 2020].

Degree of modularity is the next choice in terms of converter architecture. The modular architecture which comprises several low-voltage/current rating modules is used as a building block of the entire system. On the contrary, the non-modular system is based on a single power converter structure that takes the advantages of the wideband-gap semiconductors. Several advantages such as power and voltage scalability, easy maintenance and fault-tolerant strategy implementation can be obtained from the modular architecture. The non-modular architecture, on the other hand, has the advantages to use lesser number of semiconductors, drivers, sensors with single high frequency transformer in comparison with the modular architecture.

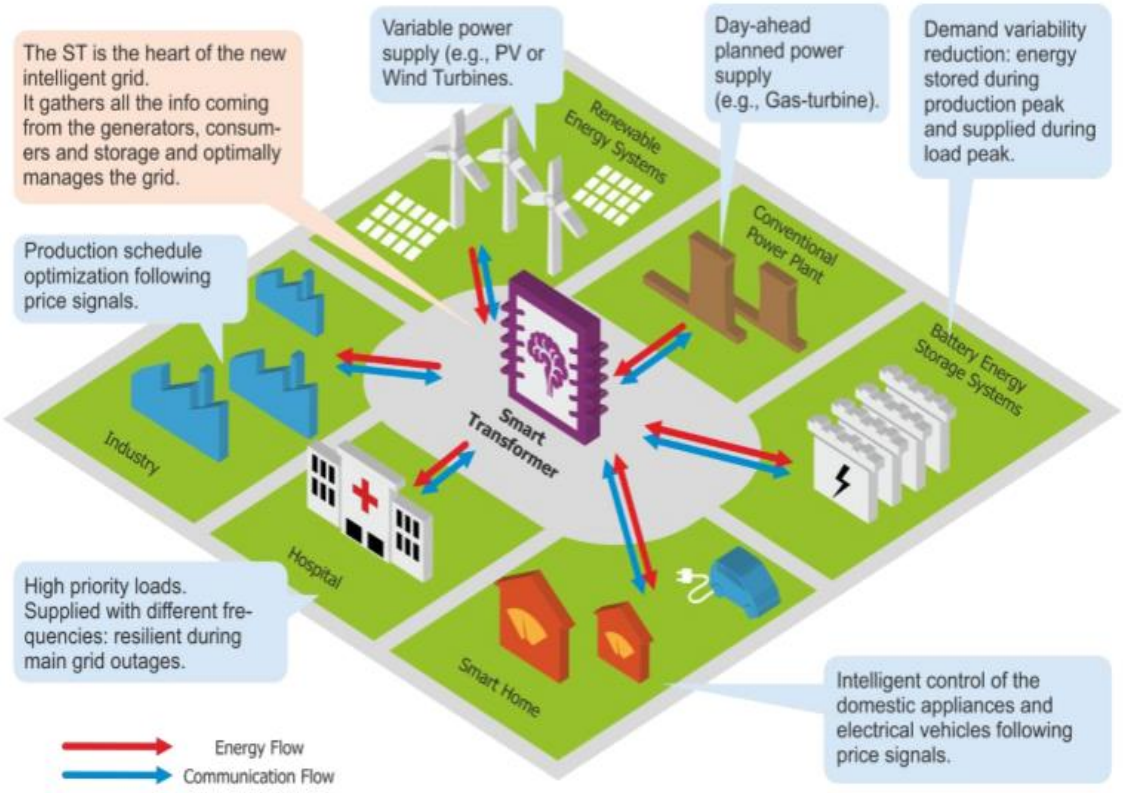

Fig1. 7 Roles of smart transformer in smart grid (M.Liserre , 2010).

1.7. Statement of the Problem

1) The Secha feeder in ArbaMinch Town power distribution system is getting overloaded in peak load times and node voltages at remote ends are low, causing poor operation of user loads. Moreover, there is a growing trend in the use of distributed energy resources in the distribution system, and hence the conventional transformer (CT) is not suitable for handling flexible control of active power and reactive power, mitigation of load harmonics and improvement of voltage sag for short circuits happening on the medium voltage (MV) line.

2) Owing to the above mentioned shortcomings of conventional transformer (CT), modular smart transformer (ST) is becoming its potential competitive substitute in distribution systems containing distributed energy resources (DERs).

3) The smart transformer being used as energy substitute of conventional transformer is constructed from power converters made of semiconductor switches having limited voltage blocking capacity. The power converters can be modular or non-modular leading to modular and non-modular architecture of smart transformer of which the modular architecture is gaining popularity as it is constructed from readily available power switches having low voltage and current ratings.

4) Therefore, in this dissertation, a modular smart transformer is designed, modeled, analyzed and integrated in to the existing Secha feeder line of ArbaMinch town distribution system for system performance enhancement.

1.8. Research hypothesis

1) Integration of modular smart transformer in to distribution system can improve efficiency, voltage sag and non-linear voltage and current distortions

2) Use of modular multilevel converter (MMC) based smart transformer can produce a better performance than a CHB based smart transformer (Comparison of MMC with CHB topology)

3) Use of fuzzy logic controller (FLC) and adaptive-neuro fuzzy inference system (ANFIS) in various ST stages can give better performance than a conventional PI controller.

1.9 Objectives

- General objectives:

The general objectives of this research work (dissertation) are outlined as follows:

- to design, model and analyze modular smart transformer for power distribution system
- to integrate a modular smart transformer in to existing distribution system containing conventional transformer for evaluating efficiency, voltage regulation and harmonics distortions

- Specific Objectives:

This dissertation or research work is specifically aimed:

- to design, model and simulate front side modular converter of smart transformer
- to design, model and simulate isolation stage(DC//DC) converter of smart transformer
- to design, model and simulate the back end converter of smart transformer
- to integrate an ST model into existing distribution system model and analyze its impact on the performance the distribution system.

1.10 Description of Study Area and Delimitation

ArbaMinch town distribution system is supplied from ArbaMinch distribution substation which has a maximum capacity of 49MVA, supplied by two power transformers of the following ratings:

- Two winding transformer: 132/15kV, 16/25MVA
- Three winding transformer: 132/33/15 kV, 20/16/8MVA

The substation has eight (8) outgoing feeders: five on 15kV level and three on 33 kV level. The five 15 kV outgoing feeders supply various loads in ArbaMinch town (Sikela and Secha sub-towns), Textile factory, ArbaMinch University main campus (AMU) and rural areas. The two 33kV outgoing feeders supply loads in Kamba and Boreda areas while the remaining 15kV outgoing branch is left idle (standby).

At present time, the ArbaMinch town distribution network covers 66km of medium voltage radial distribution lines (distributers) feeding loads at Sikela, Secha and nearby premises. The Town distribution network contains more than 193 distribution transformers of different capacities (25kVA, 50kVA, 100kVA, 200kVA, 315kVA, 500kVA, 630kVA, 800kVA and 1250kVA) which are installed at various sites in the Sikela and Secha sub-towns to supply power to commercial, residential and industrial loads. The town distribution system contains 51869 residential customers, 785 commercial customers and 6273 commercial customer, having a total of 58927 customers. The layout diagram of ArbaMinch distribution substation is shown in Fig.1.8

The research work is confined to 15kV/0.415kV medium voltage (MV) distribution system of ArbaMinch town, in particular a feeder supplying 50kVA transformer in Secha sub-town. The main focus of the project is design and modeling of 15kV/0.415kV multiport smart transformer made from modular multilevel converters. The three stage ST based on modular converters is integrated to the existing Secha feeder supplying Ayssa common residence to see the impact of ST. Performance analysis of modified Secha distribution system in the presence of the smart transformer to evaluate the role of ST in improving voltage regulation, fault tolerance, reactive power support and voltage quality is also in the domain of the research scope.

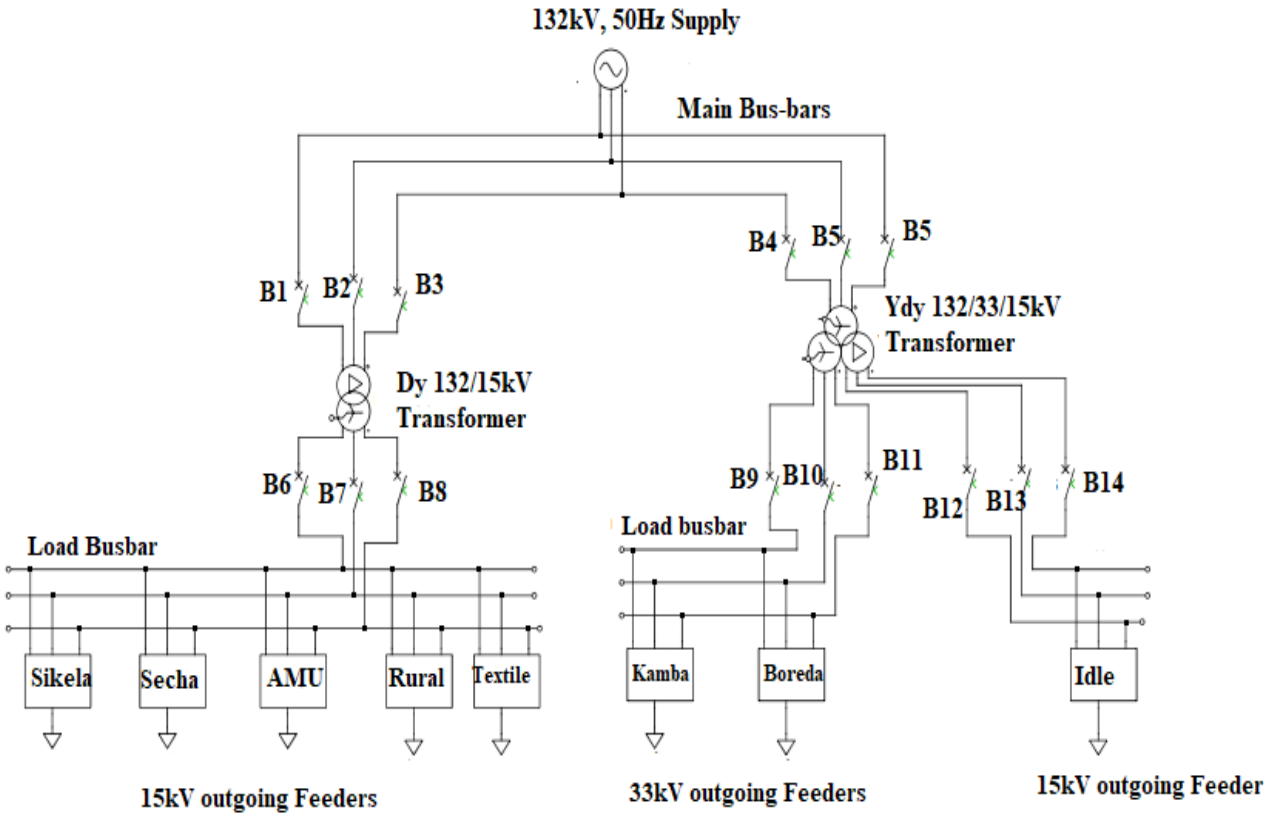

Fig1. 8 Layout of ArbaMinch distribution substation

1.10 Methodology

This research work uses the following methodology to achieve its set objectives:

- **Identification of technical gaps and limitations in performance of classical transformer and smart transformer:**

This can be done by making observation on the existing distribution transformer performance with regard to voltage control, active power control, reactive power control, harmonics and harmonics mitigation technics. Limitations of smart transformer can be found by survey of relevant literatures

- **Sampling Technique**

The distribution system under study contains two medium voltage levels, 33kV and 15kV feeders, where the 33kV feeders supply rural loads and 15kV feeders supply loads in the town premises. Out of the two voltage levels, a 15kV medium voltage level is randomly selected as

a medium voltage for the study to make the data collection process easy. From five outgoing feeders on 15kV bus bar, the Secha feeder is selected for study as it goes long distance (15km) and supplies heavy loads of many organizations. Observation of distribution system under study shows that transformers on 15kV voltage level have ratings of 50kVA, 100kVA, 200kVA, 315kVA, 500kVA, 630kVA, 800kVAand 1250kVA, each located on different parts of the town. Out of the above mentioned ratings of distribution transformers, a 50kVA transformer on Secha feeder supplying small village is randomly selected to be studied and replaced by a smart transformer.

- **Data Collection (Primary and Secondary data)**

The data may include relevant distribution system data such as transformer number and ratings, outgoing feeder size and length, average and peak demand and load types.
Instrument such as power quality analyzer can be used to measure the active power, reactive power and apparent power at the distribution feeder under study

- **Analyzing load data:**

The hourly collected power data on the outgoing feeder(s) of transformer was analyzed in Microsoft Excel using descriptive statistics to get the total average active and reactive power values of each parameter of the feeder.

- **Selection of modeling software**

Following determination of load data for the selected feeder, evaluation of modeling software was done to choose the one which suits the research objectives. SIMULINK/PLECS modeling platform has been used

- **Design and modeling of Smart transformer:**

After determination of medium voltage ac (MVAC) voltage, load data, design of front stage converter, middle stage converter and back stage converter of smart transformer (ST) was done by considering voltage ratings, current rating and overload requirements of power semi-conductor devices.

- **Simulating:**

Simulation is carried out for peak system loading to see the performance of modular smart transformer for efficiency, voltage regulation and power flow control for different scenarios

such as linear loads, nonlinear loads and faults on the modular converter. Simulation parameters such as voltage, current, power loss, reactive power flow, total harmonic distortion are taken for steady state condition.

- **Making Comparison:**

After getting simulation results with conventional transformers and modular smart transformers, comparison of system performance with conventional transformer and with modular smart transformer was done for evaluating the impacts of using smart transformer in the distribution grid.

1.11 Relevance and Scope of the Research

This research work is significant to the area of electrical power engineering in the context that the traditional centralized power system architecture is evolving to decentralized power system architecture, where the smart transformer serves as an integral part for energy transfer, voltage regulation and flexible integration of hybrid micro grid. In particular, the research work has benefits to:

- Ethiopian Electric Power(EEP) as it improves operating performance of distribution system
- customers as it improves power system reliability and allows bi-directional power and data flow
- researchers in electrical engineering as a basis for future study

This dissertation work is limited to design and modeling of three-stage smart transformer for 15kV distribution system. The work doesn't include integration of intermittent renewable energy sources or other distributed energy sources and cost feasibility analysis of the proposed model, which are recommended for future work

1.12 Organization of the Dissertation

This dissertation work is organized into five (5) chapters. Chapter one discusses about introduction to conventional electric grid and smart grid, problem statements, objectives and methodology. Chapter two (2) presents about Background theory and literature survey on smart transformer concept, architecture of smart transformer, power converter topologies, control and modulation techniques, review of modeling platforms and power semiconductor modules. Chapter three (3) describes design, modeling and simulation of front stage converter, middle stage converter, and back stage converter of modular smart transformer. It

also deals with modeling of control and modulation system for smart transformer and distribution system under study. Chapter four (4) is dealing with integration of modular smart transformer in to the existing distribution system model and evaluation of its impact on distribution system performance. Chapter five (5) makes general conclusions and recommendations of the dissertation work.

1.13 Publications Emanating from this Dissertation

From this research work, two publications are produced as per the ASTU guideline for postgraduate studies. One in international journal with Scopus/web of science index and the other in peer reviewed accredited national journal. The following publications are produced from the research work:

- Design and Analysis of Front Side Modular Multilevel Converter for Smart Transformer in 15 kV Arba Minch Distribution Network Using Diverse Controllers and Multicarrier Modulation (Journal of Engineering, Volume 2022, Article ID 7678241, 14 pages https://doi.org/10.1155/2022/7678241)
- A comparative study on modeling and performances of modular converter based three phase inverters for smart transformer application (Journal of Science and Inclusive Development Vol. 5, No. 2, DOI:10.20372/jsid/2023-256©2023)

CHAPTER TWO
BACKGROUND THEORY AND REVIEW OF LITERATURE

2.1 Overview

Several solutions proposed in order to improve the reliability, stability and power quality of the power system are based on power electronics technologies. Some of these technologies are Flexible AC Transmission Systems (FACTS), electronic circuit breakers, High Voltage Direct Current (HVDC) transmission, active filters, electronic on-load tap changer (OLTC) and Solid State Transformers (SSTs) (M. Liserre et'al., 2010; M. Liserre, et'al.,2016). A distribution transformer based on power electronics devices can be considered as an optimal candidate to improve and implement new operation in the form of ancillary services (Chandan Kumar et'al., 2015). A Solid State Transformer also known as Smart Transformer consists of power electronic converters interfaced to a high frequency transformer(s) with an effective control and communication system. The concept of a Solid State Transformer has been started since 1970 by W. McMurray (W. McMurray, 1970) who developed the initial high frequency link AC/AC converter, with purpose of converting AC to AC to step-up or step down voltage with the same function as that of a conventional low frequency transformer. A high-power SST with AC/AC conversion having capability of distribution transformer has been proposed shortly afterwards by author (J. C. Bowers et'al., 1980). For that topology, the incoming AC wave form is modulated by a power-electronic converter to a high frequency square wave and passed through a small high-frequency transformer. Since 2002, various research institutes such as Electrical Power Research Institute (EPRI) and Future Renewable Electric Energy Delivery and Management (FREEDM) have been researching on this electronic device having in mind features of modularity and intelligence (W. McMurray, 1970; J.E. Huber et'al., 2016; Kang.M. et'al., 1999). The growth on power semiconductor devices with high voltage and current handling capacity as well as discovery of new magnetic materials having higher saturation flux density and low core loss have contributed much for SSTs to be feasible economically and technically, attracting the interest of global research institutions such ABB, Siemens, Schneider, G.E, etc.

2.2 Smart Transformer Architecture

The type of smart transformer architectures to be used depends on factors such as type of application, required efficiency, reliability and functionalities. There are different approaches to classify smart transformer architecture. These factors can be number of power converter

stages, number of ports, and control of isolation stage, voltage level and modularity. An easy-to-use method to classify ST architecture and choose the convenient configuration according to the specific system requirement was suggested by the following authors (Falcones, et'al., 2010; Mohammed A. et'al, 2020) based on number of power converter stages. On the basis of this classification, four basic topology variants can be distinguished as shown in Fig.2.1.

a) single-stage topology having direct AC-to-AC conversion,
b) two-stage topology having low voltage DC link (LVDC),
c) two-stage topology having medium voltage DC link (MVDC),
d) three-stage topology having both HVDC and LVDC link.

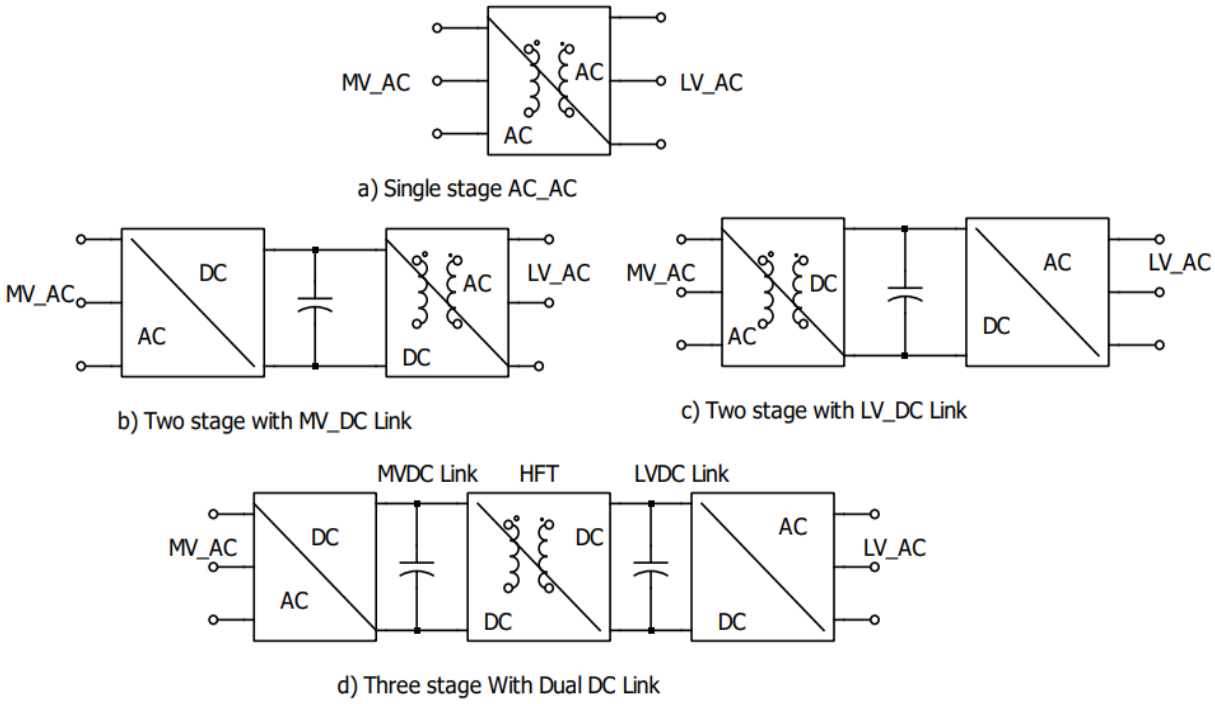

Fig2. 1 Block diagram of smart transformer configurations

a) Single stage topology

This type of SST topology is the earliest one and contains only one power processing converter stage. It includes a direct AC/AC, DC/DC or a matrix converter with no DC link. It is single primary single secondary (SPSS) configuration based on number of ports per power stage. The drawback of this type topology can be viewed from the lack of providing DC links since the DC link enables an ST capable of delivering additional services such as connection to hybrid distributed generators, reactive power compensation

to the grid. Moreover, many key components in a smart-grid such photovoltaic array, fuel cell, storage devices, and Inspire of limited functionalities, STs having one stage STs need simple control with reduced number of switching devices and hence have low switching losses as compared to other topologies (S. D. F. Zambrano, 2011).

As shown in power circuit in Fig.2.2, in single stage ST, an input high voltage is turned into a high-frequency square wave and passed through the medium frequency transformer (MFT) to the low voltage side where it is converted back to 50 Hz sinusoidal shape voltage

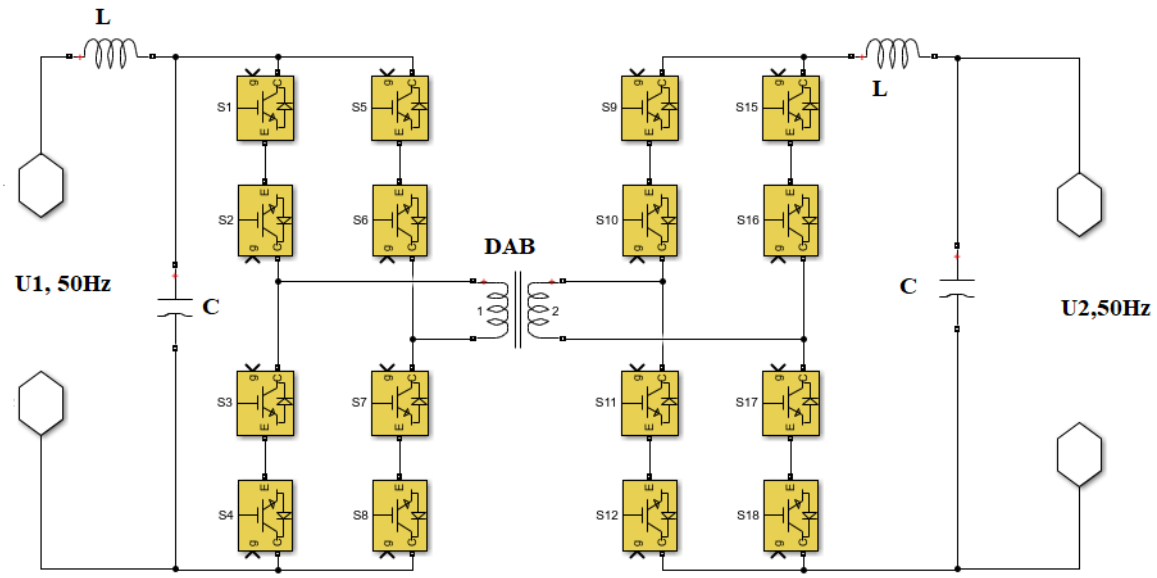

Fig2. 2 Power circuit of single stage ST constructed from full bridge

b) Two-Stage Topology

An SST having two-stage topology can be constructed with single primary dual secondary (SPDS) configuration or dual primary single secondary (DPSS) configuration. The smart transformer having dual stage topology based on an AC-DC converter and a PWM inverter is shown in Fig. 2.3. The switches on the high side must be four-quadrant to withstand bi-polar voltages and currents. An SST containing two-stages with an LVDC link facilitates easy integration of storage devices and DC sources. Furthermore, additional functionalities such as power factor correction can also be obtained from this type configuration. Seamless bi-directional control of the power and capability of zero voltage switching for a wide range of loads can be achieved by use of a dual active bridge (DAB) However, high sensitivity of the

average active power flow to leakage inductance variation and the large ripple currents are some of disadvantages of this topology. The application of the two-stage SST (Fig.2.3) with MVDC link is confined to providing additional services to the HVAC grid (S. D. F. Zambrano, 2011).

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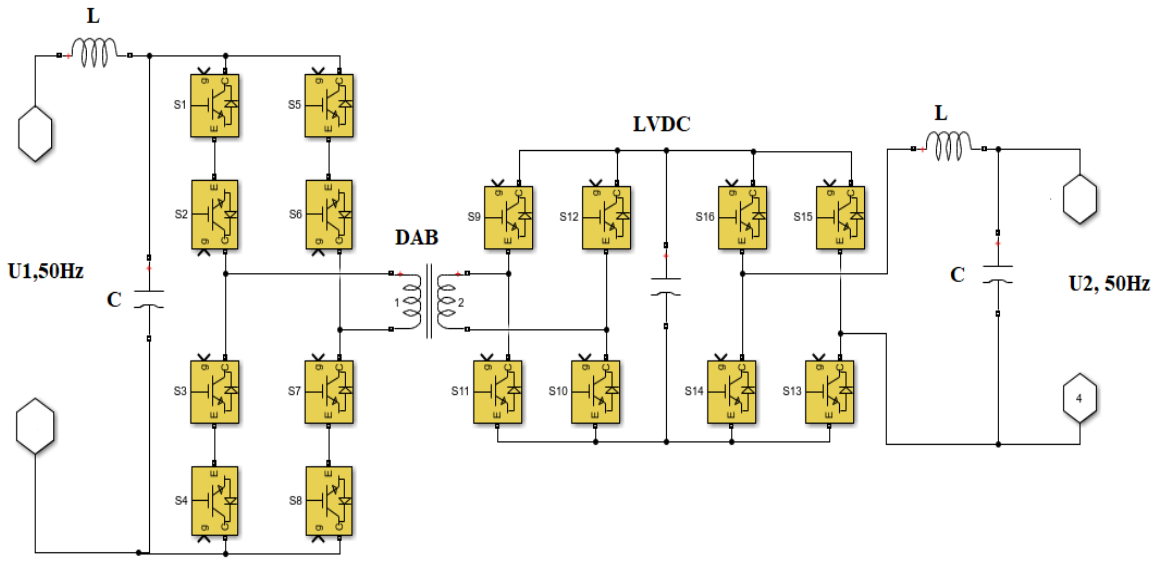


Fig2. 3 Power circuit of two-stage ST

c) Three-Stage Topology

Three-stage topology offers many potential services that smart transformers are expected to play in smart power distribution system [26]. This topology comprises front-end converter, middle stage converter and back-end converter. This topology can be constructed with dual primary dual secondary (DPDS), single primary triple secondary (SPTS) or triple primary single secondary (TPSS) based on relative position of isolation stage and other converter blocks. Power circuit of three-stage topology with DSDS configuration is shown in Fig. 2.5. In normal power flow condition, front-end converter rectifies the AC input voltage to output DC voltage, forming an MVDC link this way. In the middle stage converter, the MVDC voltage is converted into medium frequency square shape AC voltage and fed to the MFT, where the level of voltage is stepped down and again rectified to a low voltage DC level, forming an LVDC link this way. The low rectified DC voltage is fed to the back-end converter where it is again converted into 50 Hz AC voltage. It is clear that the levels of voltage in the MVAC port and MVDC link are governed by the voltage withstand capacity of

the switches. Consideration of the state-of-the-art IGBTs, which have a blocking voltage level of 6.5 kV, the MVDC and MVAC voltage levels are usually confined to 4 kV and 3 kV, respectively. The blocking voltage levels mentioned above are not high enough to allow connection to a typical AC and/or DC distribution networks with voltage rating of 15kV to 33kV. This limitation could be overcome by parallel and series combination of power modules and converters to form a modular structure with high voltage blocking capacity, current capacity and reliability. It was reported in (Xu She, Xunwei, et'al., 2014; S. Mad husood hanan, et'al., 2015; F. Wang,et'al, 2014; H. Qin, et;al., 2013) that modular three-stage topology (Fig.2.4) is more attractive type than one-stage and two-stage topology with regard to power and voltage scalability, maintenance, and also fault-tolerance , voltage regulation and power factor correction, and hence a modular three-stage smart transformer is proposed in this dissertation work.

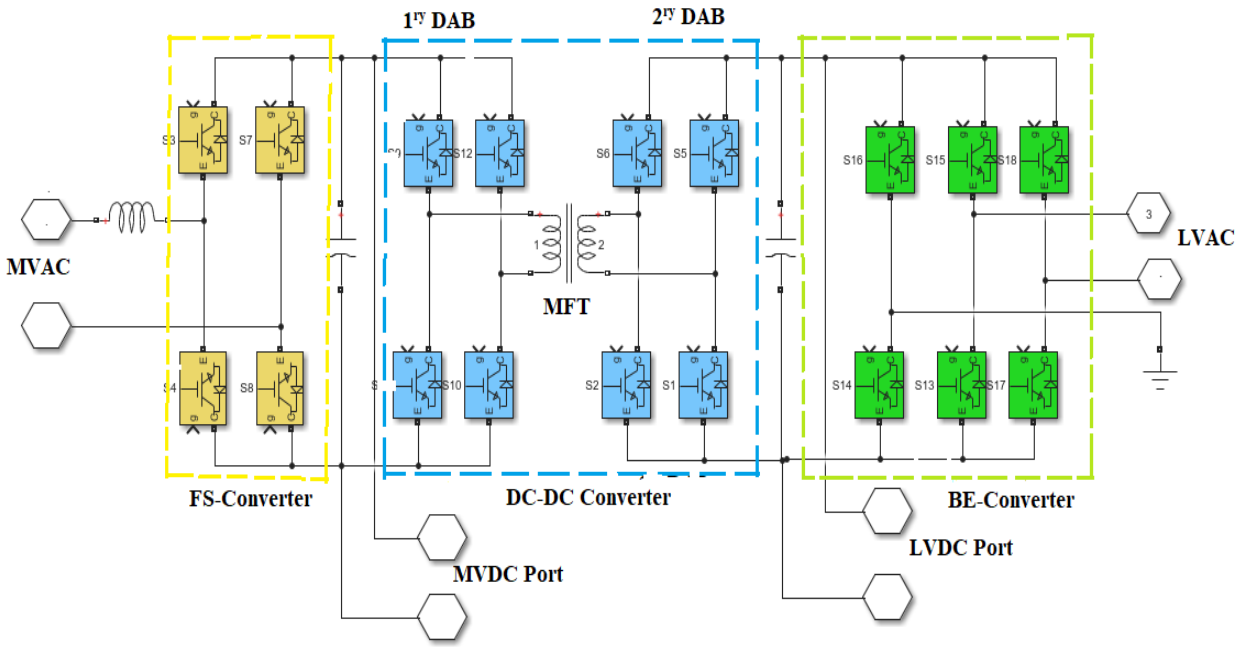


Fig2. 4 Power circuit of single phase three-stage smart transformer

2.3 Composition of Modular Smart Transformer

As shown in Fig. 2.4, the three-stage modular STs designed typically for the purposes of smart grid applications are made up of three converters, viz: the Front-end converter, isolation stage converter and back-end converter with characteristic features fully described in the following subsections. Since power electronic converters are at the heart of ST, ensuring that their design and circuit topologies can meet operating and security requirements across a range of applications is very important. Converters architectures for ST is capable of

expanding functionality, scaling-up in power and voltage ratings as needed, and compatible with legacy and new components. Apart from these, other features that should be considered are connection to hybrid sources/loads, multi-frequency inputs , outputs with multiple ports, bi-directional flow of power, self-protection, galvanic isolation, re-configurability of components, system reliability under non-ideal and faulted conditions, integration with controls and communications, and built-in cyber-physical security.

2.3.1 Front End Converter

The front end converter takes a medium voltage ac in put (MVAC) and converts to MVDC through the rectifying process or vice versa. The converter enables the ST to filter out the reactive power in the MV grid and taking only the active power and feed it to the next stage. The various power converter topologies suitable for front stage medium voltage level of ST applications are: Neutral Point Clamped (NPC) or Diode Clamped, Flying Capacitor (FC), Cascaded H-Bridge (CHB) and Modular Multilevel Converter (MMC) (M. Liserre et'al., 2010; Mahammad A. et'al 2020; M. Liserre, et'al, 2016).

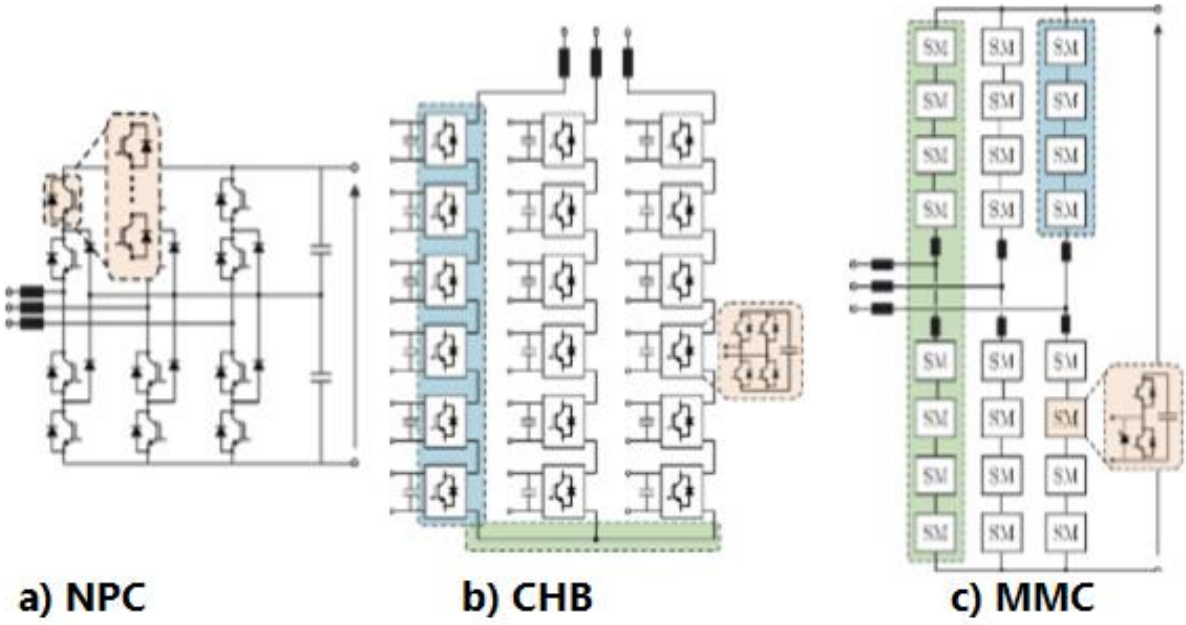


Fig2. 5 Front-end converter topology (M. Liserre , et'al., 2010]

The neutral point clamped converter, also known as diode clamped converter, is shown in Fig.2.5a). It is made of a number of two-level voltage source inverters which are joined together via the clamping diodes forming the neutral point that splits into half the DC link voltage. Due to the presence of neutral point, the power switches from which the converter is formed should withstand only half of the DC link voltage. This topology offers advantages

such as reduced capacitor requirement because of equal sharing of DC bus voltage by all phases, controllable reactive power and simple pre-charging of capacitors. The drawbacks of this topology are increase in clamping diodes in square function as the number of voltage levels increase, flow of different magnitude of the phase RMS current through the switches as some switches conduct for a longer time than others and difficulty in real power flow control due to the overcharging or discharging of the DC link capacitors which do not allow an accurate control.

A flying capacitor converter has similar structure to that of the neutral point clamped one. Its difference is that the diodes in the former are replaced by capacitors. It has advantages of controllable reactive power flow, maintaining operability during short outages or deep voltage sag as a result of large number of capacitors. However, large number of capacitors results in expensive, bulky and difficult packaging system. Its efficiency compared with other topologies is low as the pre-charging of the capacitors is complex. A flying capacitor converter fed to the three phase is shown in Fig. 2.6

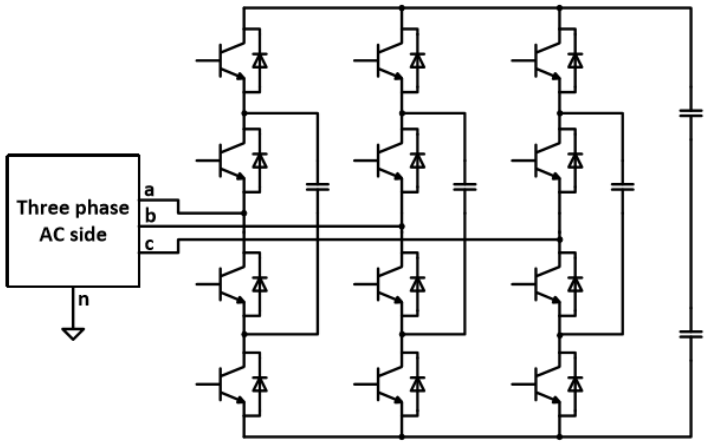


Fig2. 6 Flying capacitor converter

The cascade H-bridge converter (Fig.2.6b) is the widely used topology. It comprises several single phase H-bridge converters which are serially connected. In this kind of topology a wide rating of output power and voltage are allowed because the single H-bridge output voltages can be combined to fulfill the requirements of the application. The modularized layout and easy packaging is also among the attracting features of this topology because each level has the same structure. In order to form the modular converter configurations, the DC bus voltages could be connected in parallel or series. The major pitfalls of this converter are the absence of the DC link and the need of isolated voltage supplies at cell level.

Another topological variant that fulfills the quality of low-frequency operation and modularity is the Modular Multilevel Converter (MMC) (Fig. 2.5c).Unlike CHB, MMC does not require separate DC voltage supply at cell level; instead, it uses floating capacitors for energy transfer and is modular in nature. An MMC could be a better option on the HV/MV side of distribution network as compared to the other multilevel converter topology. This is due to the presence of the DC link, simple voltage scaling, easy bypass of faulty cells in case of faults, its robustness and modular nature while obtaining an improved power quality.

However, the complexity in control circuits and the huge DC capacitors together with many components constitute a problem of reliability though its availability is high. Commonly used sub-modules used for implementing an MMC are full bridge and half bridge, though other sub-modules such as cross connected half bridge can also be used. Using half bridge power modules has advantages of small switch count yielding higher efficiency though the device suffers four times higher DC link voltage. MMC based on half bridge power module will be used in this project

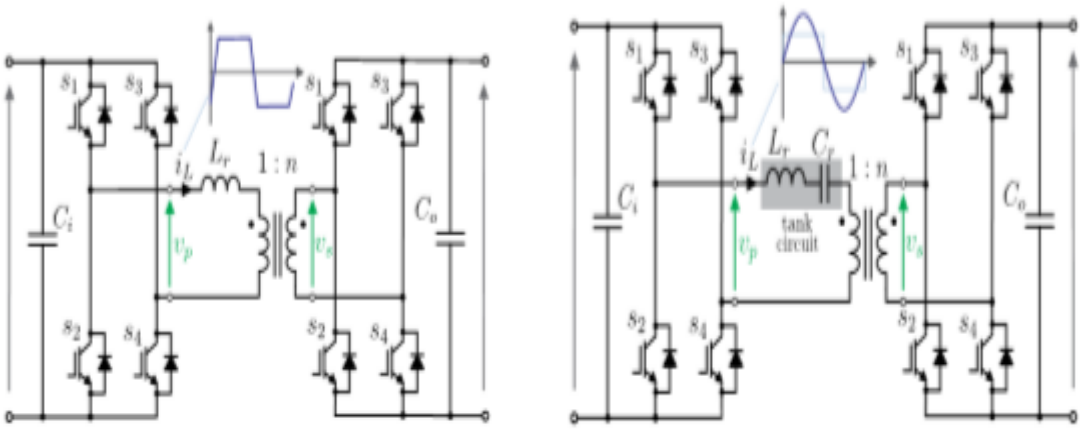
2.3.2 Isolation Stage (DC//DC Stage)

The isolation stage of modular smart transformer comprises a medium frequency DC/AC converter, medium frequency transformer (MFT) and medium frequency AC/DC converter. As the input of this stage comes in the form of DC and the output goes out in DC form, this stage is also named as DC//DC converter with double slash indicating presence of MFT for isolation. This stage presents the most difficult task in the design of the ST because it has rigorous requirements such as high current burden in LV side, high voltage burden in MV side, high rated power, high frequency operation of isolation transformer and high efficiency. Two solutions have been widely investigated to address aforementioned requirements: the first one is using standard converters made of high voltage rating devices, while the second one is using a modular concept, in which several modules are cascaded for purpose of sharing total power and voltage among them. The modular solution, though presents a high number of components, it offers many advantages compared to the first solution, such as: low dv/dt (low EMI emission), possibility to use standard low voltage rating devices that favor modularity for allowing to implement redundant strategy to increase the fault tolerance and availability (Mahammad A , et'al, 2020).

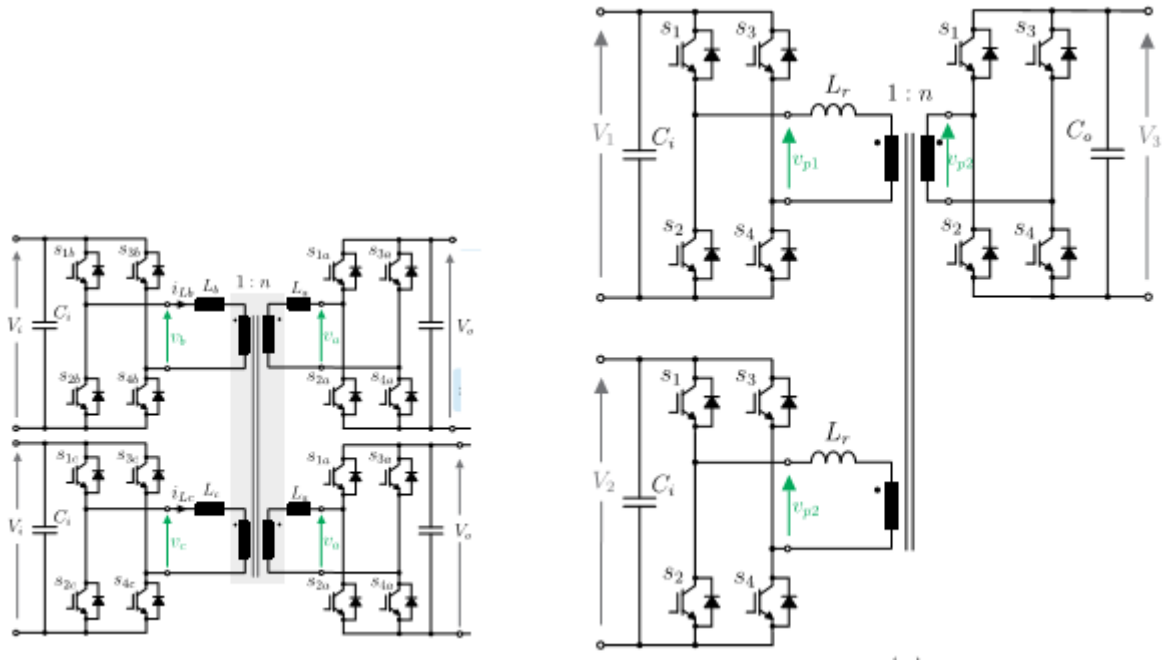
For isolation stage, different types of converter topologies can be used to interface the HV and LV terminals of high frequency transformer (HFT). Candidate converter topologies for

isolation stage include the series resonant converter (SRC), dual-half bridge (DHB), dual-active bridge (DAB), asymmetrical-quadruple-active bridge (AQAB), and symmetrical quadruple-active bridge (SQAB). Series-Resonant converter (SRC) has advantages of soft-switching, high efficiency and power density. It offers a good regulated output voltage for a wide range of loads operating in discontinuous-conduction mode avoids the requirement of control loops and reduces the number of sensors. However, with regard to the control of power flow control or output voltage, the DAB converter is superior since it works with active control of the transferred power. Many variant topologies can be stemmed from the DAB by coupling many active bridges to the same medium frequency multi-winding transformer, forming multiple active bridges (MAB). MAB can be configured in the form of asymmetrical-quadruple-active bridge (AQAB) and symmetrical quadruple-active bridge (SQAB) having same feature as DAB, but with additional characteristics to integrate many active bridges to a single MFT. This structure enables the connection of many sources or loads with different voltage levels. It is also possible to use hybrid combination of SRC with DAB and SRC with QAB to harness the advantages of each type (Mahammad A, et'al, 2020; M. Liserre, et'al., 2016; L. F. Costa, et'al., 2017).

Candidate single phase converter topologies for DC//DC stage are given in Fig.2.8 a-d



a) Dual Active Bridge(DAB) b) Series Resonant Circuit (SRC)



c) Multiple Active Bridge in SQAB configuration d) Multiple Active Bridge in AQAB configuration

Fig2. 7 Power Circuit of DC//DC Converter

DAB can also be configured in a three-phase version by addition of extra leg to the existing active bridge (converting it to the three-phase bridge) and making use of three phase MFF transformer, as described in Fig. 2.8 (a)-(c) (L. F. Costa, et'al 2016).The major benefit of this structure over the single phase DAB is the reduction of output current ripple, thereby allowing smaller size bank of capacitors.. Except the reason mentioned above, both converters have similar performances with regard the voltage and current stress on the semiconductors and transformer. The drawback is the complex transformer structure and large number of switches. When the duty cycle (d) = 1, the three-phase DAB operates with ZVS regardless the load type. Therefore, for constant input and output voltage, the converter can be designed properly to operate with soft-switching for the entire range of load, in the same manner to the single-phase DAB. Different transformers connections such as Y-Y and Y-Δ connection have been investigated but there was no significant change on the efficiency [41]. A variety of topologies that use six legs and three single-phase transformers, as illustrated in Fig. 2.9 (c), were proposed in (L. F. Costa, et'al 2016). In this dissertation work, AQAB, SMAB and DAB in ISOP configurations are proposed to see their impact on system performances.

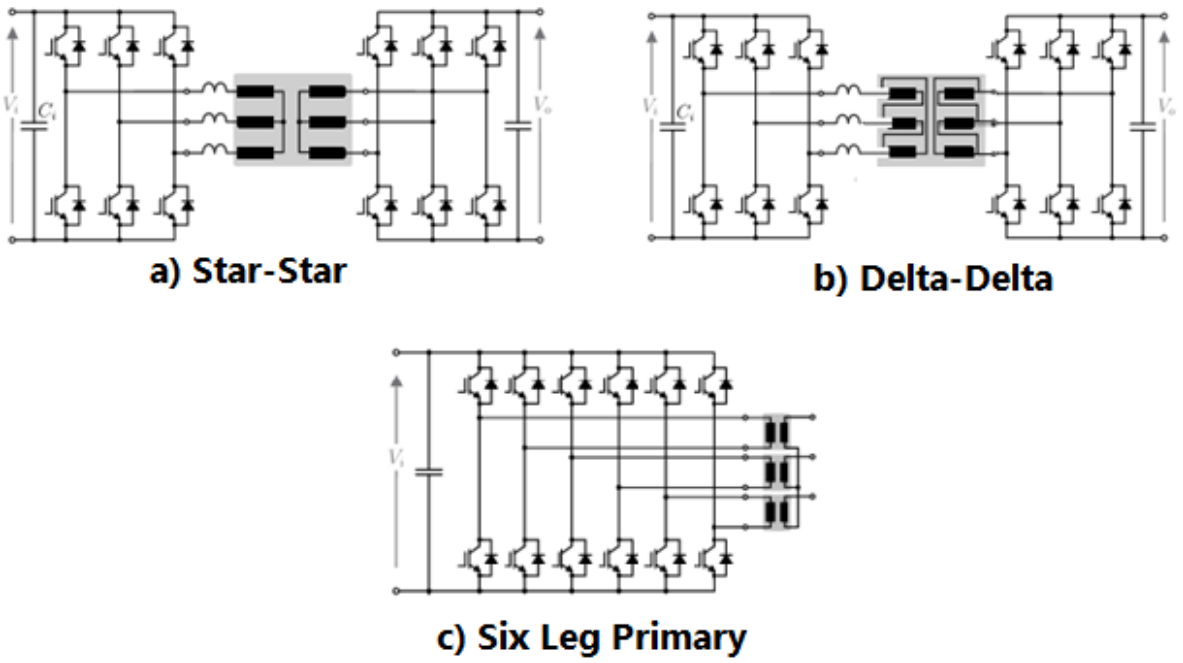


Fig2. 8 Three phase dual active bridge (DAB) topologies

2.3.2.1 The Dual Active Bridge (DAB) operating principle

A simplified DC//DC converter stage constructed from a DAB can be illustrated by bringing the secondary bridge to the primary side and representing the medium frequency transformer by its leakage inductance, *Lk*, as described in Fig. 2.9 (R. W. De Doncker , et'al., 1991; G. G. Oggier ,et'al., 2006; G. G. Oggier,et'al, 2009). With the assumption that a very larger magnetizing inductance is present in comparison with the leakage inductance, an open circuit can be considered in the magnetizing branch. The leakage inductance of the medium frequency transformer acts as the main energy storage and transfer element (F. Krismer, et'al 2012).

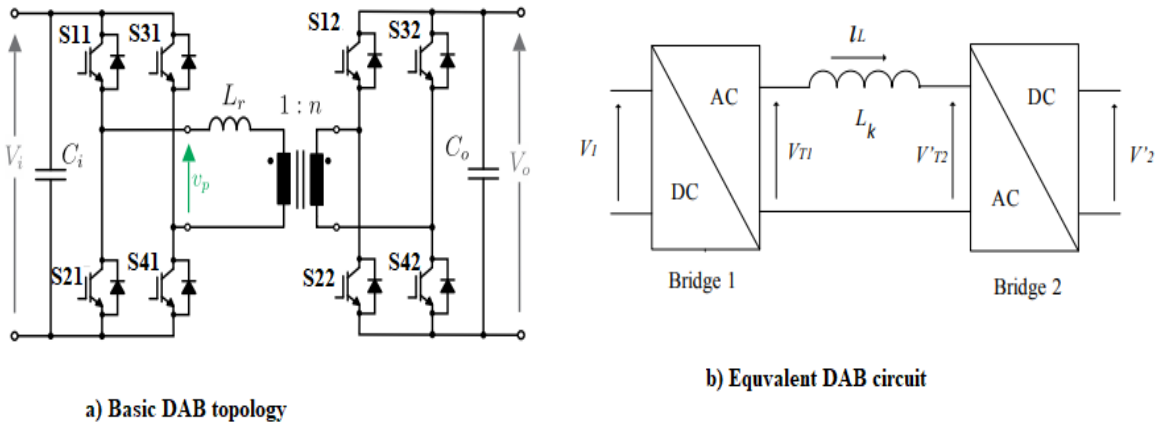


Fig2. 9 Representation of dual active bridge (DAB)

The phase shift between the primary and secondary voltages decides the amount of power being transferred between them. Although many modulation techniques are proposed in literature, a phase shift pulse-width modulation (PSPWM), which have certain advantages over the traditional phase-shift modulation (PSM) is used. By Using the PSPWM method the zero-voltage switching (ZVS) operating range can be extended for allowing the use of wide input or output voltage variations, and reduces the RMS currents of transformer ((F. Krismer, et'al 2012).. The ideal voltage and current waveforms of the DAB using PSM are shown in Fig. 2.10, where $\theta = \omega t = 2\pi fswt$, fsw is the carrier frequency, δ is the zero-crossing angle of inductor current (iL), ϕ stands for the phase-shift angle, and ip is the primary current (Falcones , et'al., 2010). These waveforms are applicable to any of the chosen ST topologies for the case to where VT1 >VT2 for which power flow is from first bridge to second bridge (K. D. Hoang , et'al, 2012; R. W. De Doncker, et'al, 1999).

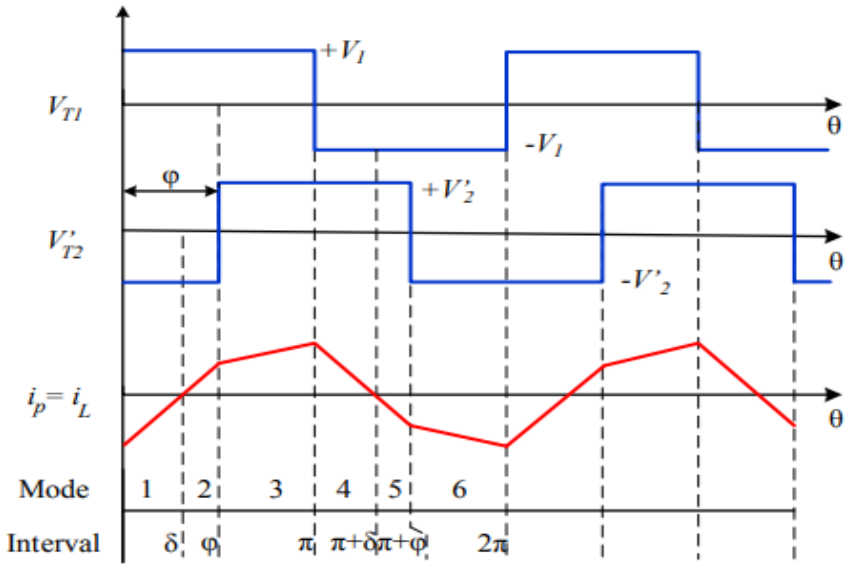


Fig2. 10 Dual active bridge (DAB) operating wave form

As shown in Fig. 2.10, six operating modes associated with the operating state change of a switching device are observed in one cycle. However, every half cycle of the switching frequency the current waveform is reversed due to symmetry. Therefore, it is only necessary to derive the equations for the inductor current for mode 1 and mode 3 intervals to determine the dynamics of iL (K. D. Hoang, et'al., 2012). For the specified intervals, the conducting switches, including freewheeling diodes are shown in the table 2.1

Table2.1 Switches and diodes conduction transition of DAB

$0 < \theta \leq \delta$		$\delta < \theta \leq \varphi$		$\varphi < \theta \leq \pi$	
First Bridge	Second Bridge	First Bridge	Second Bridge	First Bridge	Second Bridge
D11 ,D41	D22, D32	S11, S41	S22, S32	S11, S41	D12, D42

The dynamics of inductor current (iL) for simplified representation of the DC-DC stage shown in Fig. 2.11(b) can be expressed as::

$$\frac{d\mathrm{iL(t)}}{dt} = \frac{\mathrm{VT1\ (t) - VT2\ (t)}}{\mathrm{Lk}} \qquad (2.1)$$

Making use of ideal current form of Fig.2.10 and solving for inductor current (iL) in the first half cycle for each interval gives the following relations:

For $0 < \theta \leq \delta$

$$(iL(\theta) = \frac{\mathrm{V1\ (t) - V2'(t)}}{\omega \mathrm{Lk}}\theta \quad + iL(0) \qquad (2.2)$$

For $\delta < \theta \leq \phi$,

$$(iL(\theta) = \frac{\mathrm{V1\ (t) - V2'(t)}}{\omega \mathrm{Lk}}(\theta - \delta) \quad + iL(\delta) \qquad (2.3)$$

For $\delta < \theta \leq \pi$,

$$(iL(\theta) = \frac{\mathrm{V1\ (t) - V2'(t)}}{\omega \mathrm{Lk}}(\theta - \phi) \quad + iL(\phi) \qquad (2.4)$$

By equating the average value of iL in one cycle to be equal to zero, the initial condition is calculated, hence $iL\ (0) = -iL\ (\pi)$ which results in:

$$(iL(0) = -\left[\frac{2V2'\phi + \pi(V1 - V2')}{2(\omega Lk)}\right] \qquad (2.5)$$

Observation of Fig2.12 shows that at θ = δ, inductor current (iL) is equal to zero.

Equating equation (2.2) to zero at δ gives the following relation:

$$\delta = \left[\frac{2V2'\phi + \pi(V1 - V2')}{2\big((V1 - V2')\big)}\right] \qquad (2.6)$$

The instantaneous value, (ϕ), is calculated from (2-3) for $\theta = \phi$

$$(iL(\phi) = \frac{2V1\phi - \pi(V1 - V2')}{2\omega Lk}\theta \qquad (2.7)$$

2.3.2.2 Maximum Power Transfer

The average transferred power between the DAB primary and secondary converters can be obtained by considering primary side and secondary side converter voltages and dynamics of inductor current equations as given below (G. G. Oggier , etal., 2006).

$$Po = \frac{1}{Ts}\int_0^{Ts} VT1(\theta)iL(\theta) \qquad (2.8)$$

where, Ts is the switching period

Solving (2.8) gives the following equation for transferred power:

$$P_O = \frac{V1V2'}{\omega Lk\pi}\phi(\pi - \phi) \qquad (2.9)$$

Looking in to equation (2.9) shows that the amount and direction of power flow is dictated by the phase shift angle (ϕ) between the voltages at primary side converter and secondary side converter (F. Krismer, et'al., 2012; G. G. Oggier, et'al., 2009). For $\phi > 0$, power flow is from DAB-1 to DAB- 2 and for $\phi < 0$; power flow direction is reversed**.** The value of ϕ for which maximum power transfer happens is obtained by taking the derivative of (2-9) and equaling it to zero.

$$\frac{\partial Po}{\partial \phi} = \frac{V1V2'}{\omega Lk\pi}(\pi - 2\phi) = 0 \qquad (2.11)$$

Solving equation (2.11) for ϕ gives its value for maximum transferred power to be:

$$\phi = \pm\frac{\pi}{2} \qquad (2.12)$$

For the value of ϕ varying from 0 to $\pi/2$, the magnitude of power flow varies from zero to maximum However, to get the advantage of ZVS for full-operating region, the voltage ratio between primary side and secondary side voltages equals one (1). For a voltage ratio other than unity (1), the ZVS range where maximum converter efficiency can be achieved is reduced to a smaller operating region (G. G. Oggier , et'al., 2009).

2.3.3 Back-End Converter (BEC)

Back-End Converter of the ST, which is connected to the LV AC grid or loads, is a voltage source inverter (VSI) generating sinusoidal AC voltage having 220 V (P-N) or 415 V (L-L), 50Hz specification. It is the most vulnerable stage to the LV grid disturbance and hence its filter circuit (common mode and differential mode filter) should be prudently designed. The low grid voltage level at this stage for the power conversion process enables the use of mature topologies, with standard semiconductor having industry accepted low blocking voltage (1.2 kV, 1.7kV, 3.3kV. The high current involved and the EMI filter design are the major difficulties of this stage. Depending on the amount of power to be served, redundant converter approach can be used to handle the high current. In order to avoid high frequency disturbance injection to the grid, the EMI filter circuit must be properly designed. Availability of the neutral conductor is requirement of this ST stage as the low voltage power distribution grid is based on the Terra-Terra (TT) configuration. The zero sequence current that is injected by the non-linear and unbalanced loads should also be properly handled by this stage. A three phase three wire or four wire VSI can be used but the four wire VSI is the most appropriate one with regard to choice of freedom and control of neutral current. Among the commonly used topologies, standard two level voltage source inverter (VSI), the three-level neutral point clamped (NPC) and the T-type topologies can be highlighted as demonstrated in Fig.2.11 and Fig.2.12 (Mahammad A , et'al., 2020).

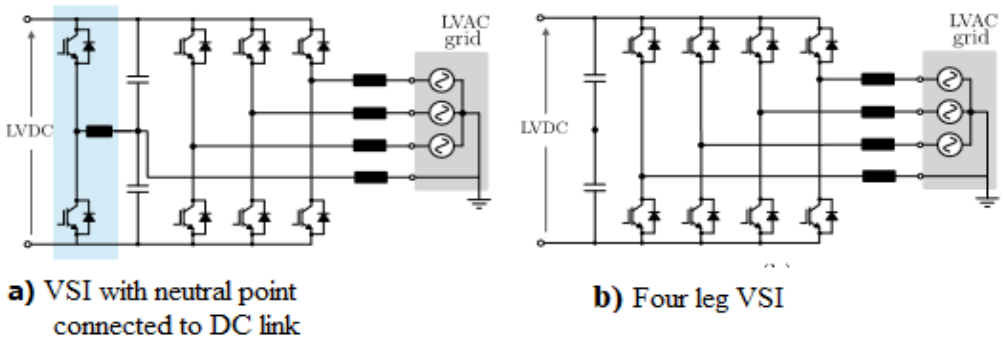


Fig2. 11 Topological variants of two level VSI

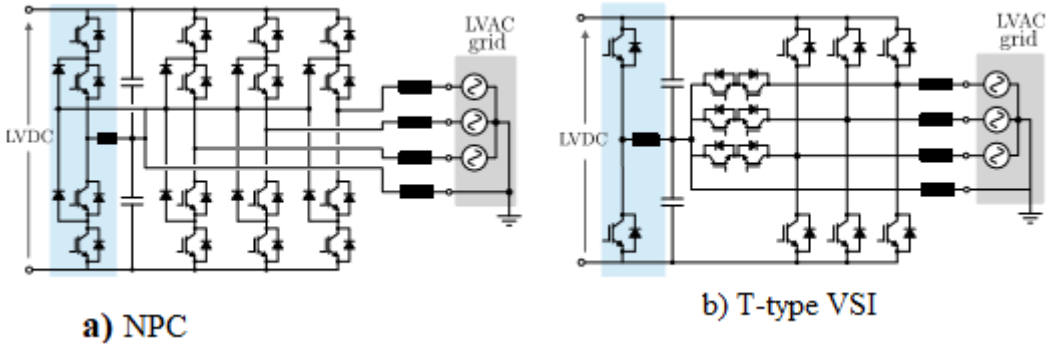


Fig2. 12 Configurations of three level Voltage Source Inverter (VSI)

The two-level and three-level VSI suffers from high dv/dt, di/dt and lack intelligent operation (activation and deactivation of modules) in the time of partial loading of distribution grid. A possible solution to these problems is to use different types of multilevel inverters which have been discussed in (LI Wei, et'al., 2011) due to their low switching frequency operation. The CHB and MMC shown in Fig.2.13 are commonly used multilevel converters of because they have several advantages such as design modularity based on identical module structure, simple voltage scaling using a combination of cells, and possibility of using redundant converters for power scaling.

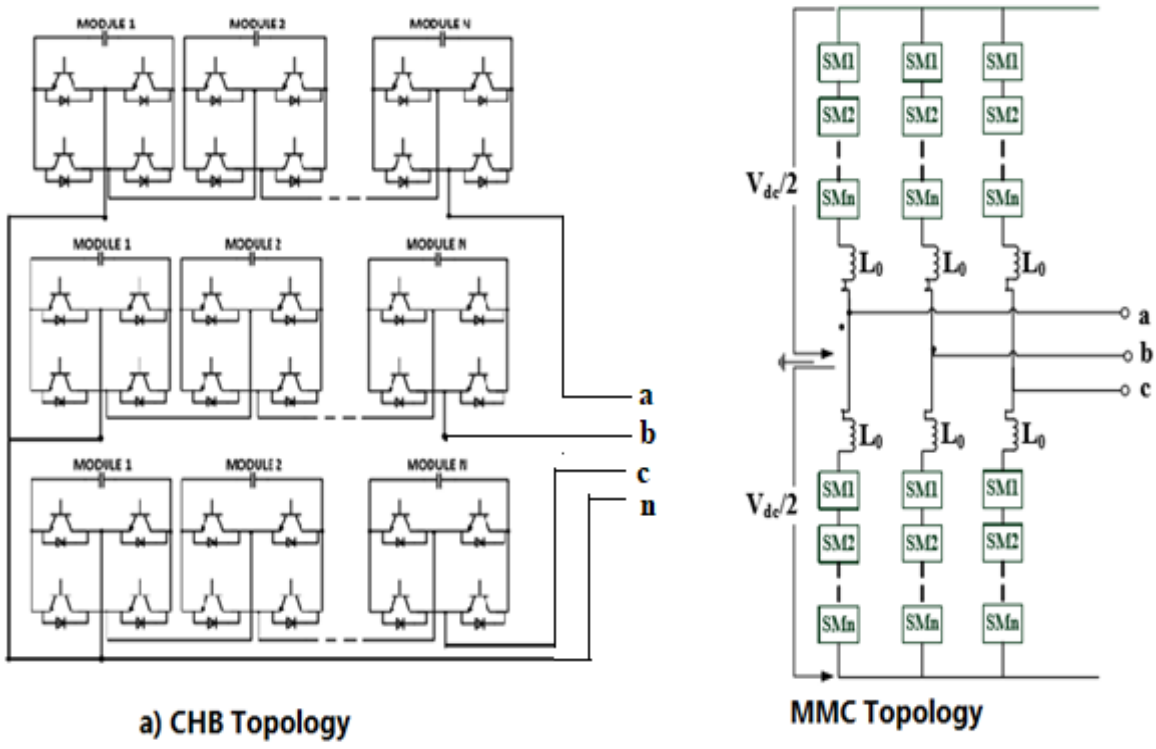


Fig2. 13 Modular Multilevel Inverter Configurations

2.4 Medium Frequency Transformer (MFT)

MFT is at the heart of ST which brought about a substantial reduction in volume and weight of ST as compared to low frequency transformer (LFT). This advantage of SST is achieved as a result of small size windings required by high frequency magnetic field (Banaei , et'al., 2011)

The operation principle of MFT is same as that of LFT, with a difference in frequency level. Selection of core material, wire and winding placement has a profound impact on the optimized operation of MFT. Silicon Steel, soft ferrite, amorphous core and Nano crystalline core materials can be used, of which Nano-crystalline is most preferred as it has smaller core loss and average flux density. In general, core materials having thin silicon steel laminations, amorphous or nano-crystalline are appropriate to be considered for ST applications. However, the eventual choice is based on the designer criteria such as design tradeoffs among volume, efficiency and cost. Table.2.2 shows the property of various core materials to be used for ST (EMETOR,, Ferroxcube, 2013; Metglas®, 2015)

Table2. 2 Property of MFT core material

Core Material	Core material Property			
	Permeability @ 20 kHz, μi	**Flux Density (T)**	**Core loss density** (Pfe) @ 20 kHz, 0.2 T(W/kg)	**Temperature (^{0}C)**
Silicon Steel (Arnon 7)	16k	1.53	<400	730
Ferrite 3C94	2k	0.47	<18	220
Amorphous metglas (2605SA1)	10 k-150 k	1.56	<40	399
Nano-crystalline Vitroperm 500F	20k	1.2	<8	600

Selection of winding material is done in such a way that loss due to skin effect is minimal. This is achieved by subdividing a wire in to smaller strands with proper shields to for a Litz wire. Many thin insulated strands are used to form a thicker wire whose thickness is calculated by volt power calculation (J. W. Kolar, et'al., 2016]

Transformer winding geometry is another factor which affects the performance of HFT/MFT. Solenoid type and coaxial winding are candidate winding geometry, with solenoid type the most recommended one because of its low cost and easy manufacturing.

Based on the core geometry, the solenoid structure is further divided in to core-type, shell type and matrix type, each having different qualities of providing mechanical protection, leakage inductance and ac resistance. Mutual inductance and coupling coefficient, which could have impact on loss, is greatly influenced by winding placement.

To address the varied characteristics of power converters, multiport ST which utilizes multiple winding HFT/MFT is used (Mahmoud Mazhar Samad , 2019].

2.4.1 Core Loss in MFT

This section makes a deeper insight to the losses in so as to know the characterization of magnetic material. Eddy current loss, hysteresis loss, and residual loss constitute the core losses in a magnetic material (UNIFLEX, 2013).The re-orientation of the magnetic domains during magnetization and demagnetization process causes the hysteresis loss. By the application of magnetic field intensity (H) to the magnetic material, the magnetization curve follows path (1) as shown in Fig. 2.14 till saturation flux density (Bsat) is reached.. Reduction

of the magnetic field causes the flux of the material to follow path (2). When the magnetic field intensity becomes zero, the magnetic material retains a remanence flux density (Br), which is fraction of the magnetization. In order to bring the residual flux density to zero, a coercive field, labeled as Hc, must be applied. Further increase of the magnetic field in the negative direction causes saturation in the reverse direction. The reduction of magnetic field in negative direction causes the material to follow path (3) and close the hysteresis loop. The re-orientation of the magnetic domains caused by the change in the field direction happened with expenditure of energy (W. G. Hurley, et'al., 2013; W. Shen , 2006; J. B. Goodenough, 2003). This energy which is spent in re-orientation of magnetic domains is referred to as hysteresis loss. The magnitude of hysteresis loss is proportional to the area of the hysteresis loop shown in Fig. 2.14. Eddy-current loss is another kind of losses which is caused by the voltage induced within the magnetic core in similar way that it is induced across the windings as illustrated by Faraday. This voltage causes currents that flow within a core surface. Minimization of the eddy-current loss is achieved by reducing the current-flow paths within the core. Reducing the eddy current path in the core material is effected by using core material made up of laminations. Hysteresis and eddy-current losses contribute the major percent of total core loss; the remaining loss is contributed by the residual losses that is associated with a more complex mechanism and usually related to the process of relaxation in the magnetic material (B. Goodenough, 2003).

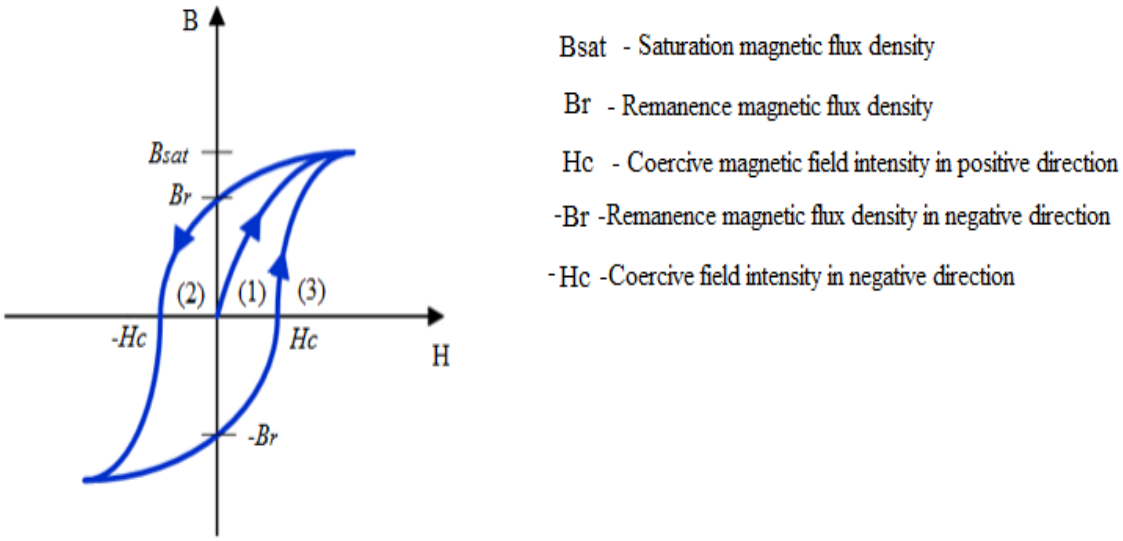


Fig2. 14 Hysteresis loop of Magnetic core

Opposed to the low frequency conventional transformer, the total losses in ST include the losses in MFT as well as the losses in various power electronic converters in each stage. Therefore, the MFT should have as high efficiency as possible to reduce the total loss of the ST. Hence, the design procedure of MFT should be followed by a flux density optimization as explained in (B. Goodenough, 2003; F. Dong Tan, et'al., 1995). The copper loss is inversely related with the square of flux density and frequency, but the core loss is directly related to frequency and flux density per the Steinmetz equation:

$$P_{CU} \propto \frac{1}{B^2 f^2} \tag{2.13}$$

$$P_{fe} \propto B^{\beta} f^{\alpha} \tag{2.14}$$

The MFT total loss is assumed to be minimal at a point where the copper loss approximately equals the core loss.

On the basis of the above assumptions, the formula to compute the optimum flux density as derived in (I. Villar, et'al., 2009) is given by:

$$B_{opt} = \frac{[h_c K_a \Delta T]^{2/3}}{2^{2/3}\,[K_W K_U \rho_W]^{1/12}\,[K_C K f^{\alpha}]^{7/12}} \left[\frac{K_V K_f f K_U]^{1/6}}{\sum VA}\right] \tag{2.15}$$

Where, the coefficients ka, kc, kw are dimensionless and obtained from studies of different dimensions of cores, ρw is the wire resistivity; hc is the heat transfer coefficient; ku the utilization factor of window; $\sum VA$ is the total power rating of transformer; ΔT refers to rise in the temperature; Kv refers to the waveform factor dependent on the shape of the applied voltage waveform to the windings; and kf is the stacking factor which correlates the net cross-sectional area to the physical core area.

2.4.2 Calculation Methods of Core Loss

Many core losses determination approaches have been reported in in the literature. The segregation of losses is among the approaches used to determine the core losses (I. Villar, et'al., 2009). Hysteresis modeling approaches such as the Preisach model and Jiles-Atherton model are the other types (J. Mühlethaler, et'al., 2012). The accuracy of these approaches is undeniable; however, estimation of core loss is commonly done on empirical equations based

on measured data. The original Steinmetz Equation (OS3E) given below is a widely used equation for core loss

$$P_V = Kf^{\alpha}B_m^{\beta} \qquad (2.16)$$

where P_V refers to the average power loss per unit volume; α , β and K are parameters obtained from material manufacturer's datasheet or fixed by curve fitting the material loss curve under sinusoidal excitation; and Bm is the maximum flux density obtained when an excitation voltage with frequency f is used. However, equation 2.13 has limitation of sinusoidal excitation application and hence not valid for power electronics systems where the core is exited with non-sinusoidal magnetic field (J. Reinert, et'al., 2001; J. Li , et'al., 2001). This becomes evident in the case of DAB converter with phase-shift modulation having rectangular waveforms in both primary and secondary transformer windings. To overcome the limitations of OSE, several modifications have been suggested among which the Modified Steinmetz Equation (MSE) equates the core loss with rate of change of the flux density (dB/dt) and to the core losses and equivalent frequency feq as given below (J. Reinert, et'al., 2001).

$$P_V\,(MSE) = \left(K\, f_{eq}^{\alpha-1}B_m^{\beta}\right) f_r \qquad (2.17)$$

Where f_r is fundamental frequency of excitation and f_{eq} is given by:

$$f_{eq} = \frac{2}{\Delta B^2 \pi^2}\int_0^T \left(\frac{dB}{dt}\right)^2 dt \qquad (2.18)$$

In equation 2.18, peak-to-peak flux density is labeled by ΔB and T refers to the period of excitation wave form.

Equation (2.17) has shown has been proved by experimental validations to be used as a general equation for arbitrary waveforms though it shows accuracy for some non-sinusoidal waveforms.

To overcome the pitfalls of the MSE, the Generalized Steinmetz Equation (GSE) was proposed. The idea behind the GSE is that the core-loss depends not only on the rate of change of the flux density, but also on its instantaneous value B(t) as shown in the equation below (J. Li , et'al., 2001).

$$P_V\,(GSE) = \frac{1}{T}\int_0^T K_1 \left|\frac{dB(t)}{dt}\right|^{\alpha} |B(t)|^{\beta-\alpha} dt \qquad (2.19)$$

Where,K_1 which is obtained by solving equation 2.19 for sinusoidal excitation and equating the result to equation 2.16 is given by

$$K_1 = \frac{K}{(2\pi)^{\alpha-1}\int_0^{2\pi}|\cos\theta|^{\alpha}\,|\sin\theta|^{\beta-\alpha}d\theta} \qquad (2.20)$$

The GSE neglects the excitation time history of material for the estimation of the power loss density; and yields inaccurate result for materials having minor hysteresis loops [59]. To cope up this limitation, an Improved Generalized Steinmetz Equation (iGSE) was proposed. In this equation, the instantaneous values of the flux density in the GSE are substituted by peak-to-peak values of the flux density ΔB so as to consider both major and minor hysteresis loops (J. Li , et'al., 2001).

$$P_V\,(iGSE) = \frac{1}{T}\int_0^T K_i \left|\frac{dB(t)}{dt}\right|^{\alpha} |\Delta B(t)|^{\beta-\alpha} dt \qquad (2.21)$$

$$K_i = \frac{K}{(2\pi)^{\alpha-1}\int_0^{2\pi}|\cos\theta|^{\alpha}\,(2)^{\beta-\alpha}d\theta} \qquad (2.22)$$

Neglecting of core loss under DC bias condition and relaxation process that occur when having waveforms with zero-voltage conditions are the drawbacks of this approach. Even though it is supposed that for constant magnetic flux density the losses in aforementioned approaches are zero, experimental results demonstrate that losses can occur even for this condition due to magnetic relaxation (J. Mühlethaler , et'al., 2012)

Despite its inaccuracies for very small duty cycles (wider zero voltage condition), the iGSE approach is used widely in loss characterization of magnetic cores. Since the core-loss density can be calculated for arbitrary waveforms, minor hysteresis loops are accounted for, and only material coefficients obtained from datasheet of manufacturer are needed [59]. Moreover, for cases where the duty cycle (D) in PSPWM is anticipated to be 50%, it yields highly accurate results (K. Venkatachalam, et'al., 2002).

2.4.3 Effects of high-frequency in Transformer Winding

The effects which are induced in the magnetic core of transformer due to high-frequency were treated in section 2.4.1. High frequency has also effects in windings of transformer such as proximity and skin effects which are illustrated in Fig.2.15. For a wire which carries DC current or AC current having low frequency, the DC resistance (RDC) can be given by:

$$R_{DC} = \frac{N \rho \ell_{eff}}{A_W} \qquad (2.23)$$

where, N stands for number of turns in the winding, ρ is conductor resistivity, ℓ_{eff} is effective length of turns and A_W is wire cross-sectional area.

If only the DC resistance (R_{DC}) is considered for winding loss calculation, it can be found by product of the square of current and R_{DC}. However, in areas where system frequency is high, there is a slight increase in resistance of a conductor because the current prefers to flow only in the circumference, tending to cover only some area of conductor area. The reduction in the effective area of the conductor causes an increase in the AC resistance -R_{AC} (C. Meyer, 2007)

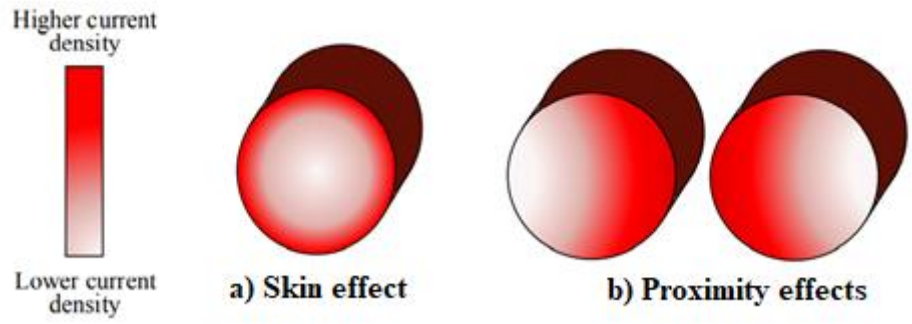


Fig2. 15 Skin and proximity effects in transformer winding

The phenomenon of slight increase in AC resistance due to high frequency is known as the skin effect and is illustrated in Fig. 2.15(a). The conductor having resistance equals that of a solid conductor under skin effect has equivalent thickness called skin depth (δ) and is calculated as follows (C. Meyer, 2007)

$$\delta = \frac{1}{\sqrt{\pi f \mu_0 \sigma}} \qquad (2.24)$$

Where, μ_0 is permeability of the free space, f is working frequency and σ is specific conductivity of conductor.

The approximate AC resistance (R_{AC}) of cylindrical conductor of radius r_o can be obtained with help of equation 2.24 as follows (W. G. Hurley, et'al., 2013).

$$R_{AC} = R_{DC}\left[1 + \frac{\left(r_o/\delta\right)^4}{48 + 0.8\left(r_o/\delta\right)^4}\right] \quad (2.25)$$

Skin effect is associated to single conductor carrying high frequency AC current. For intertwined multiple conductors, high frequency AC current causes another phenomenon known as proximity effect. The opposing magnetic fields of current carrying conductors close to each interacts in a way to cause current to concentrate on smaller area, and hence gives a rise to AC resistance (R_{AC}).

Minimization of skin and proximity effects in the windings can be achieved by using a Litz wire, which is made from insulated strands. Use of foil plates could also reduce these effects, but it is not convenient for high power application (C. William, et'al., 2011).

2.4.4 MFT Isolation Requirements

An ST should be in compliance with accepted international standards such as the ANSI/IEEE C57.12.01 related to distribution and power transformer requirements because its basic goal is to replace the conventional low frequency transformer. The transformer excitation voltage is a factor to decide the isolation level which is one of the requirements. The isolation level has significant impact on the transformer power density and hence it must be included among other design considerations. The minimum isolation distance to be included between windings during transformer design is given by the following formula (M. A. Bahmani, et'al., 2015):

$$d_{m,iso} = \frac{V_{iso}}{K_{iso}E_{ins}} \quad (2.26)$$

Where, V_{iso} is isolation voltage level, K_{iso} is safety margin based on design criteria or given by manufacturer and E_{ins} is dielectric strength of insulation material. Characteristics of some dry-type di-electric materials used in transformer are listed in Table2.3 below.

Table2. 3 Properties of dielectric material

Type of di-electrics	Property		
	heat Conductivity (W/m.K)	Strength of di-electrics (kV/mm)	Factor of dissipation -tan(δ)
Air	0.03 (@70°C)	3 0	0
Mica	0.71	11-43	-
EPOXI	0.25	15	0.02 (@100 kHz)
NOMEX	0.175 (@150°C)	27	0.005 (@60 Hz)

2.4.5 Leakage Inductance Requirement

The leakage inductance Lk of high/medium frequency transformer is additional key component to determine the amount of transferred power, as illustrated in Fig. 2.9. For transfer of maximum power, the value of leakage inductance (Lk) required to be integrated is calculated as shown in equation (2.23) below (R. W. De Doncker, et'al., 1991; F. Krismer,et'al., 2012).

$$L_K = \frac{V1V2'}{8fP_O} \qquad (2.27)$$

The structure of the MFT design will greatly influence the value of leakage inductance (B. Cougo, ,et'al., 2012).. As illustrated in Fig. 2.18, core-type and shell-type are the most commonly used transformer structures that could be used in medium frequency high power transformer applications. HV and LV side winding is placed on separate leg of the core in a core-type structure, as shown in Fig. 2.16(a) and because of the apparent separation of the windings, high leakage inductance and better isolation between windings may be achieved (W. Shen , 2006). However, estimation of its leakage inductance is not easy with analytical methods as most of the leakage flux does not remain inside the core window area.

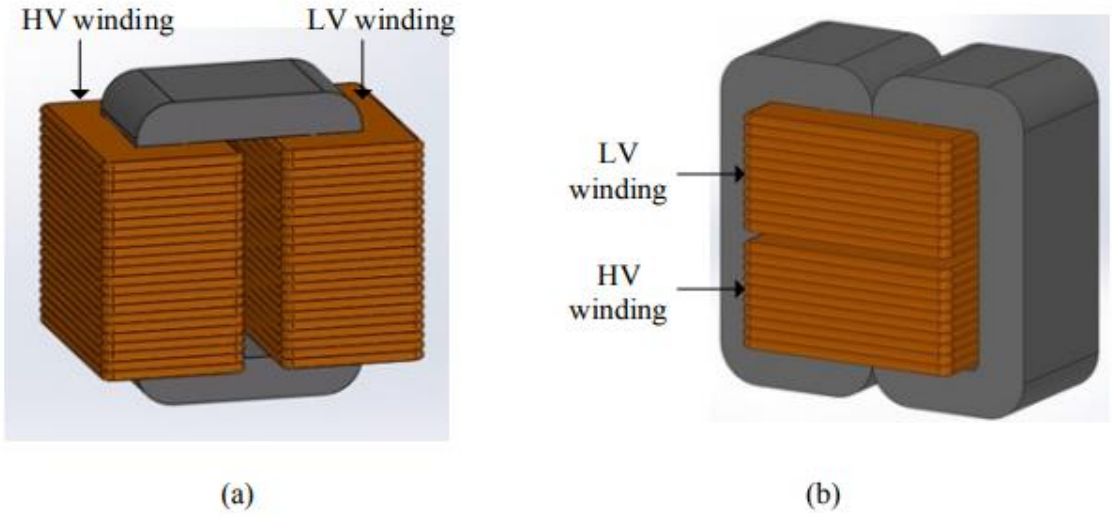


Fig2. 16 Typical MFT structures

Hence, a 2-dimensional or 3-dimensional finite element simulation is chosen for estimating the leakage inductance in core type structure (W. Shen , 2006). Both primary and secondary windings are placed in the same center leg in shell-type structure, as shown in Fig. 2.16(b). Hence, leakage inductance in this case might be lower since the leakage flux remains within the window area. This makes the calculation of leakage inductance easier and more precise. Moreover, the shell type structure has important advantage of better heat dissipation as the most of the core surface area is exposed to the air. By considering the transformer geometric parameters as shown in Fig. 2.17, the leakage inductance can be calculated as follows (C. William, et'al., 2011).

$$L_K = \mu_0 N^2 MLT\left(\frac{a+b+3c}{3w}\right) \qquad (2.28)$$

Where, μ_0 is permeability of air, N is number of turns where leakage inductance is incorporated, MLT is mean length of turns, a is width of primary winding, b is width of secondary winding, c is isolation distance and w is width of core window.

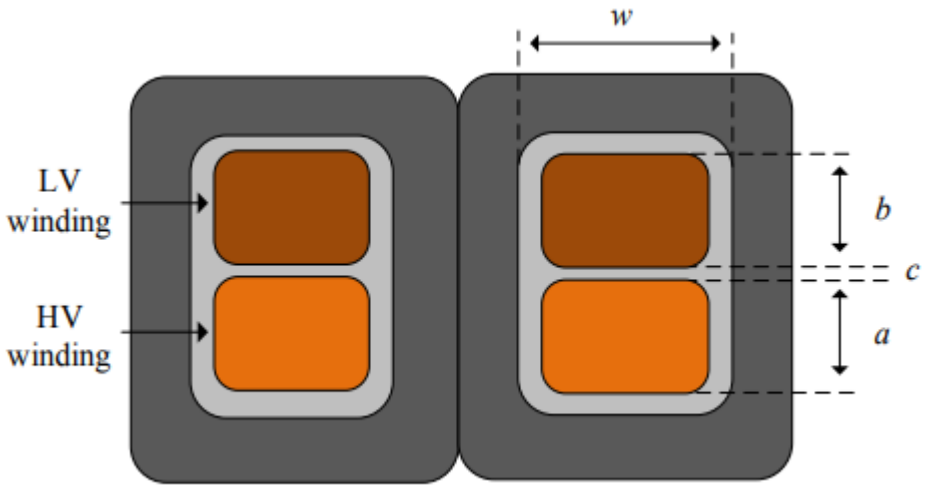


Fig2. 17 Geometrical parameters of MFT

2.4.6 Core-Loss Measurement Selection Methods

It has been explained in earlier sections that multiple factors such as excitation waveform, DC bias conditions and relaxation effects affect the core losses Hence, comparison made between results obtained by calculations using empirical equations with that from measurement is the best method for properly estimating the core losses. Many core-loss measurement methods have been suggested in an attempt to increase the accuracy of the measurements (M. Mu, et'al., 2014; J. Mühlethaler, et'al., 2012; Y. Han,et'al., 2008). In (M. Mu , 2013), a comparative evaluation of various core-loss measurement methods was reported, and the following desired features of effective measurements can be obtained:: separation of winding loss from core-loss, easy and fast implementation for measurement, applicability to any waveforms, minimum error as a result of phase discrepancy. Among many methods, the two winding method illustrated in Fig. 2.20 is the known one. The following steps are to be followed to obtain the core loss as explained in (R. Garcia, et'al., 2014).

a) Measure the current flowing in primary winding (ip) by open circuiting the secondary winding. Direct measurement by using current probe or indirect measurement by using sensor to detect the voltage (Vref) across resistor (Rref) and then applying Ohm's Law can be used to measure the current

b) Measure the secondary winding voltage (Vs).

c) Take integral of the product of the secondary voltage waveform and primary current waveform as shown below (2.29):

$$P = \frac{1}{T}\int_0^T \frac{N_P}{N_S} V_S(t).I_P(t)dt \qquad (2.29)$$

where Np and Ns are the number of turns in primary winding and secondary-winding .These two parameters are made equal for convenience (Np = Ns).

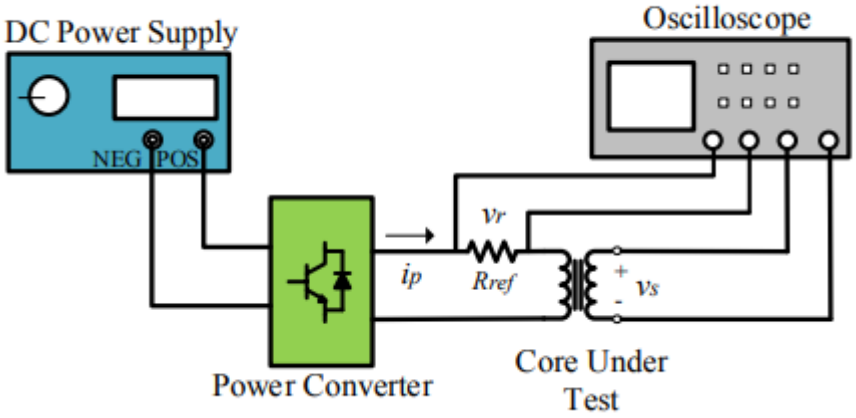


Fig2. 18 A two winding measurement schematic

Although this method has advantages such as exclusion of the winding losses from the measurements, applicability to two- or three levels or any square waveforms and simplicity due to few steps to implement, it is not suitable for high frequencies (> 1 MHz) at which phase discrepancies is significant. Newly proposed measurement methods include the capacitive cancellation for sinusoidal waveforms and the inductive cancellation for non-sinusoidal waveforms rectify the above inaccuracy (M. Mu ,2013).

2.5 Integration Level of Modular Smart Transformer (MST)

2.5.1 Power Semiconductor Switches

In order to use ST for distribution grid interfacing application, it should be able to handle the medium voltages between 2.5 to 35 kV. To achieve efficient and reliable ST in this area, the power electronic devices should have high voltage and high frequency operation**.** Readily available power switches made from silicon such as IGBTs and power MOSFETs have operating voltage of up to 6.5kV and operating frequency less than 1 kHz. The solution to realize the smart transformer by using readily available and cheaper power switches is using a series connection in the converter to share the problem of high voltage and power. However, this approach will make the used ST lose the most important idea, volume and weight

reduction. Using next generation power switches made from Silicon Carbide (SiC) and Gallium Nitride (GaN), having wide band gap (WBG) can leverage handling of high voltage up to 15kV and frequency range between 10 to 100 kHz because their critical electrical field withstand is about 300V/µm which is very large in comparison with 2V/µm field strength of Silicon based devices. Silicon Carbide GTO can be the best choice for system of (>1kA, >20kV) with 10 kHz-100 kHz. For voltages between 15kV and 20 kV, IGBT is the best whereas SiC MOSFET will be used for voltage lower than 15 kV. Use of hybrid modules that integrates Silicon power switches with wide band gap power switches can also be used to reduce cost and complexity issues (J. W. Kolar , et'al., 2018; Mahmoud Mazhar Samad ,2019; Huang, A.Q , 2019).

2.4.2 Power Electronic Building Block (PEBB)

The overall composition of an ST contains various integration levels from the smallest level to biggest level. These can be module level integration, converter level integration and system level integration. The power electronic building block is an integrated power module (IPM) which contains switching devices, gate driving circuit, sensing element, protecting element, power supplies, communication ports, passive elements, and the circuit needed to make one module. One leg of a power converter can be considered as a characteristic example of an IPM. It could be a half bridge sub-module, matrix converter sub-module, a cascaded H-bridge (CHB) or modular multilevel converter (MMC) phase leg as illustrated in Fig.2. 19. (Meynard, T, et'al., 1992; Lee, F.C, et'al, 2000; Szczesniak, P, 2013)

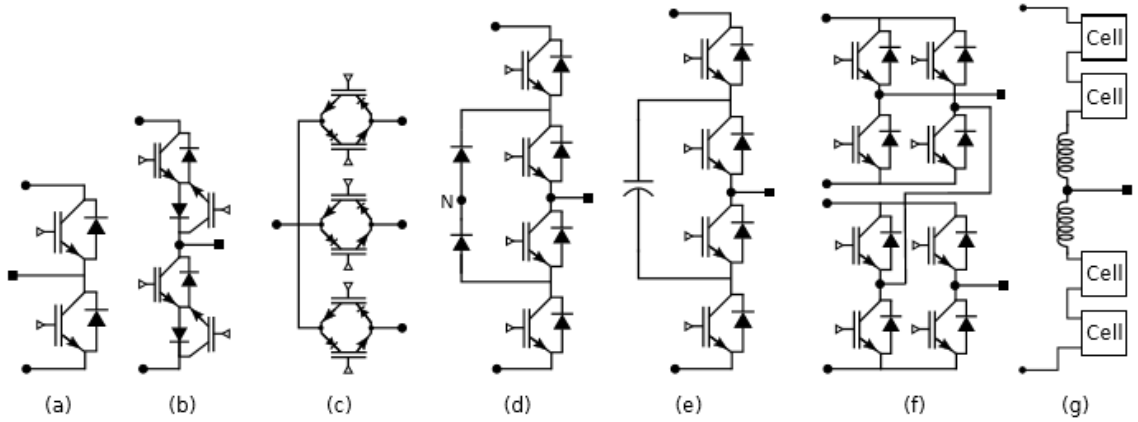


Fig2. 19 Topological variants at module-level: (a) Half bridge phase leg (b) Matrix converter phase leg, (c) Matrix converter phase leg using reversed blocking-IGBT, (d) Neutral point clamped converter phase leg, (e) Flying capacitor phase leg, (f) Cascaded H-bridge phase leg, and (g) Modular multilevel converter phase leg.

2.4.3 Converter integration level

In the converter level integration, many standard and non-standard power electronics converters could be used. This integration level is used in construction of ST blocks made from a single power converter (cell) or multiple power converters (cells) with or without HFT. An integration containing only multiple power converters is referred as ST_{block}, whereas the one containing MFT is referred as $ST_{i\text{-}block}$ as described in Fig.2.20.

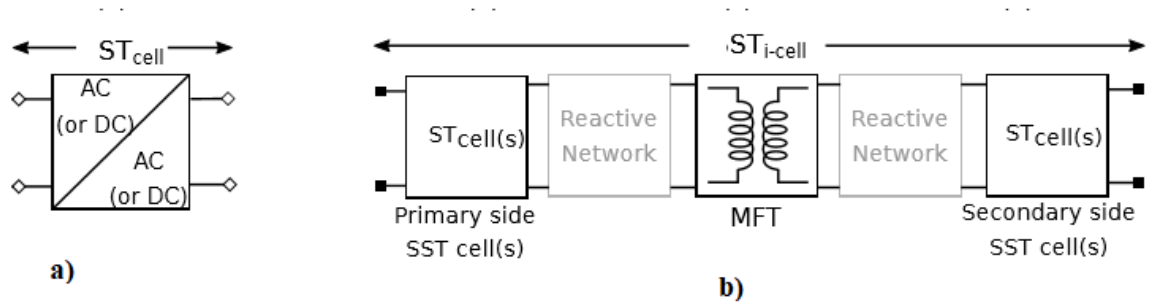


Fig2. 20 Basic converter blocks for converter level integration

In order to carry a high voltage or current levels present at the terminals of an ST, many ST_{cells} are interconnected. While series combinations are required to achieve high voltage levels with LV semiconductors, parallel combinations are suitable for carrying high current levels. Accordingly, three different interconnections such as input series output series (ISOS), input series output parallel (ISOP), and input parallel output parallel (IPOP) connection can be used to implement converter, as described in Figure 2.22a–d. (Mohammed Azharuddin Shamshuddin ,et'al., 2020; Feyzullah Ertrk, 2015; Zhang J,et'al 2017).

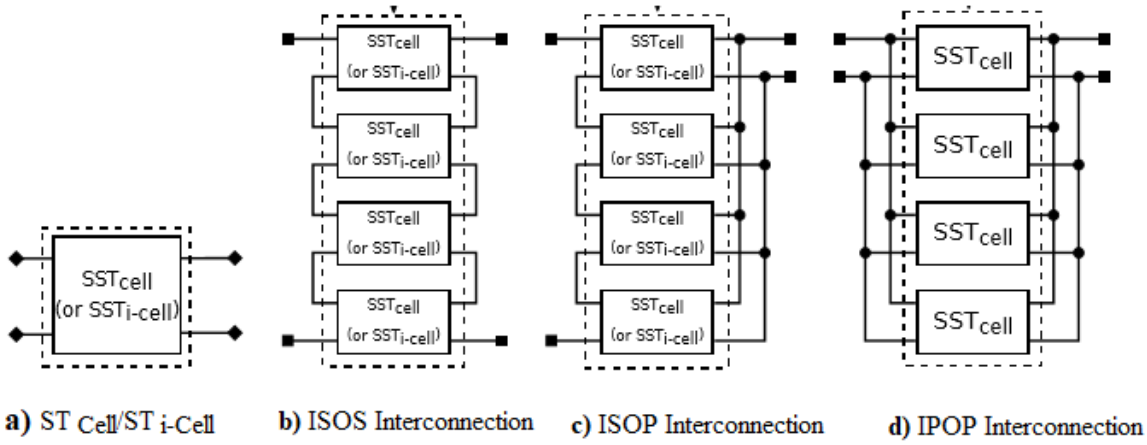


Fig2. 21 Types of converter interconnection

2.4.4 System level integration

The interconnection of many power converter levels, which can be of STcell or $ST_{i\text{-}cell}$ forms an ST_{block} or $ST_{i\text{-}block}$. The complexity of a ST_{block} or $ST_{i\text{-}block}$ is determined by the number of ST_{IPM} in each STcell or STi-cell and the number of STcell or $ST_{i\text{-}cell}$ in each of the ST_{block} or $ST_{i\text{-}block}$. When many ST_{block} or $ST_{i\text{-}block}$ integrated in phase interconnection using input series-output parallel (ISOP), input series-output series (ISOS), multiple input-multiple output (MIMO) or single input single output (SISO), it yields system level ST integration as illustrated in Fig.2.22 and Fig.2.23 (Tarisciotti,et'al., 2015; Besselmann,et'al., 2013).

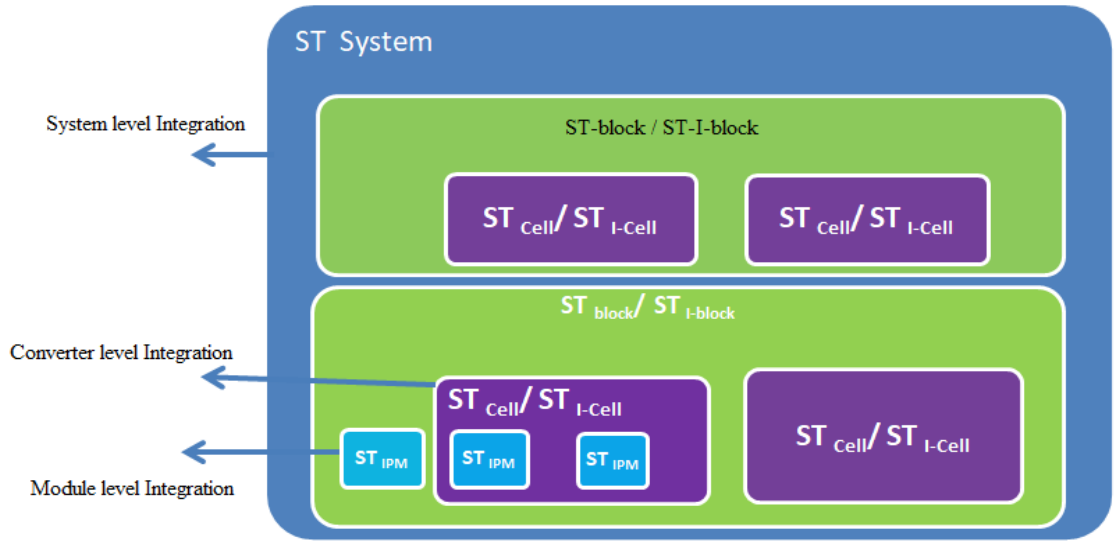


Fig2. 22 Integration levels of ST composition

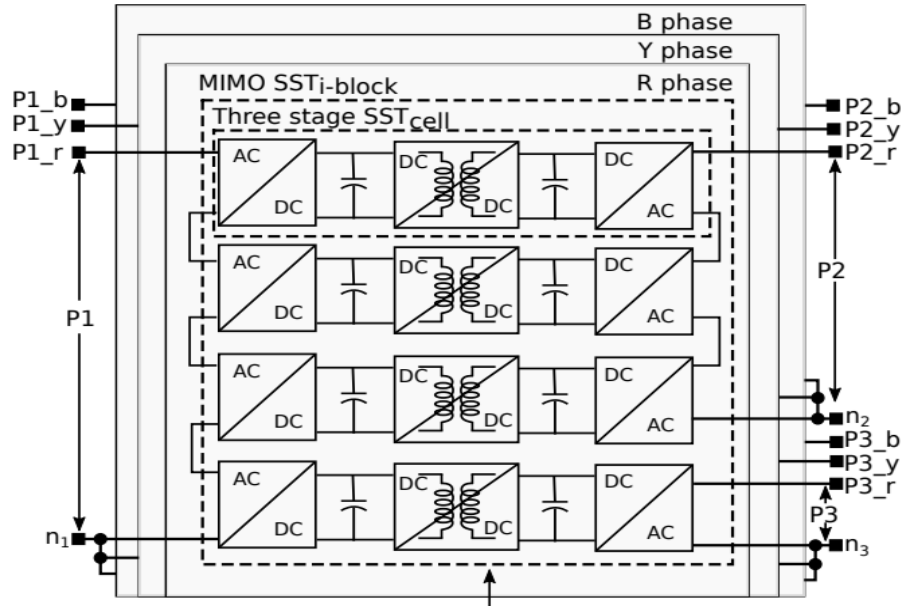


Fig2. 23 ST System integration using MIMO ST $_{i\text{-}block}$

2.6 Control and Modulation Techniques of Smart Transformer (ST)

Unlike conventional low frequency transformer (CLFT), external control is needed to operate the smart transformer (ST). There are different controllers, which operate independently on each stage of the multilevel modular converter based smart transformer (ST). Most often, closed-loop control with proportional and integral (PI) controller is used because it is simple and effective for linear system. But for complex and nonlinear systems, its performance degrades as a result of inaccuracy of mathematical plant model (Ajay B Patil, 2008). The advent of soft computing methods such as fuzzy inference system (FIS) and adaptive neuro fuzzy inference system (ANFIS) has realized better and efficient control of complex and nonlinear systems. Due to their flexibility, robustness and generalization capability, use of FIS and ANFIS to replace the conventional PI controller attracts much attention in control systems ranging from small home application to complex industrial application (Jafar Tavoosi , et'al, 1991].

Different types of modulation techniques are used to generate a gating signal for power switches. They can be categorized broadly as low frequency based modulation and multiple carrier frequency based modulation. Low frequency based modulation includes fundamental frequency modulation, nearest level control modulation and selective harmonic modulation. Multi-Carrier Pulse Width Modulation strategies are widely used for MMC because its implementation in low voltage modules is comparatively easy. Multi-carrier frequency modulation includes space vector PWM, level shifted PWM and phase shifted PWM of which level shifted and phase shifted PWM are used in this dissertation work (M. Hagiwara, et'al., 2008).

2.6.1 Phase shifted PWM

Phase shift PWM (PS-PWM) contains N carrier waveforms per leg arm of MMC. The carriers cover the whole range of modulation indices with consecutive carriers phase-shifted by $2\pi/N$, as shown in Fig. 2.24. The number of SMs to be activated in the arm is determined by the number of carrier signals that are below the reference signal at any given time. Interleaving is achieved by phase-shifting 2N carriers by π/N and distributing them alternatively between the upper and the lower arm, again with N carriers defining the transitions of each arm. The carrier frequency for PS-PWM is selected based on switching loss of SMs and working temperature.

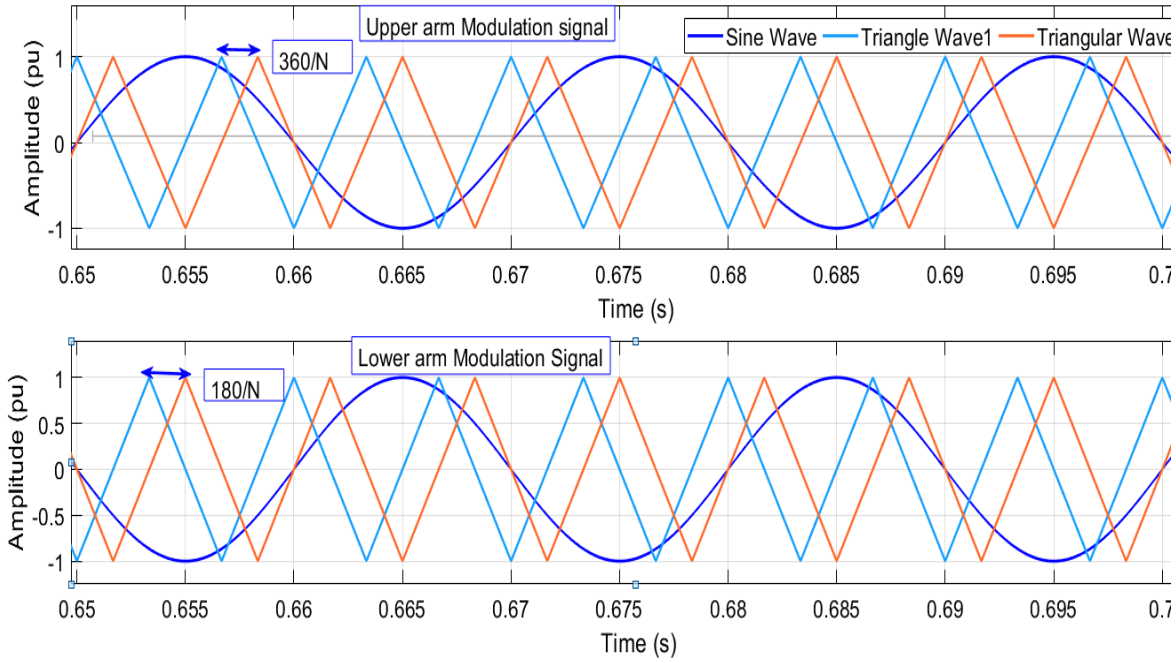


Fig2. 24 PS-PWM for two SMs per arm of MMC

2.6.2 Level shifted PWM

Level Shifted Carrier-Based PWM scheme involves several carriers that are level shifted from each other. For n voltage levels, (n-1) triangular carriers with the same frequency are arranged vertically one above the other in- phase (PD), Phase Opposition Disposition (POD), and Alternative Phase Opposition Disposition (APOD) manner ((M. Hagiwara, et'al.,2008; Giuseppe Carrara, et'al., 1992; K.Sharifabadi, et'al., 2016).

In PDPWM method, the upper and lower triangular waves are in same phase with respect to zero reference as illustrated in Fig.2.25. In PODPWM method, the triangular waves will have same frequency and amplitudes will be different. The upper triangular waves and lower triangular waves are 180 degree phase shifted as demonstrated in Fig.2.26. In APODPWM, the carriers are of same frequency and adjacent carrier amplitudes have a phase shift of 180 degrees between them as shown in Fig.2.27. Use of level shifted multi carrier PWM methods results in significant levels of THD both in the voltage and current waveforms and cause large currents to flow through the phase-legs because module capacitor voltage balancing is not easily achieved (M.S.Rajan,et'al.,2014; Feyzullah Ertrk,2015; Shoji Fukuda,et'al., 2009).

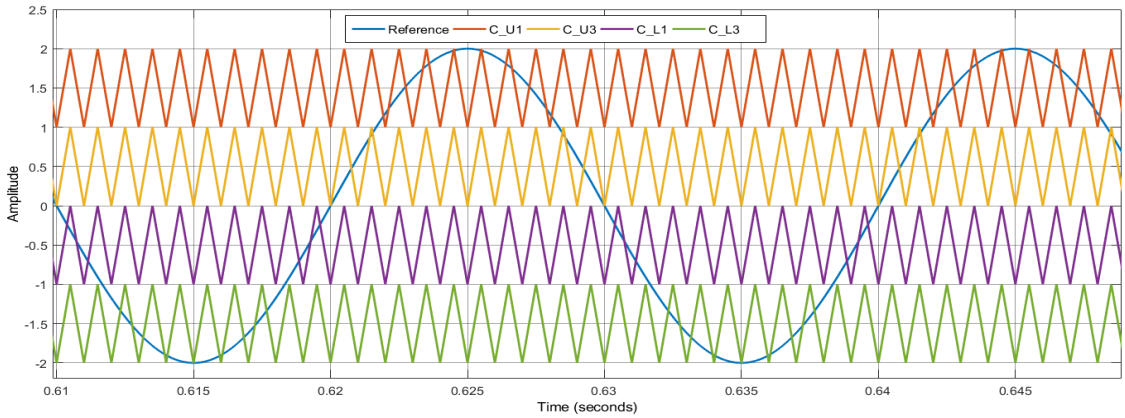


Fig2. 25 Level Shifted PWM with Phase Disposition Method

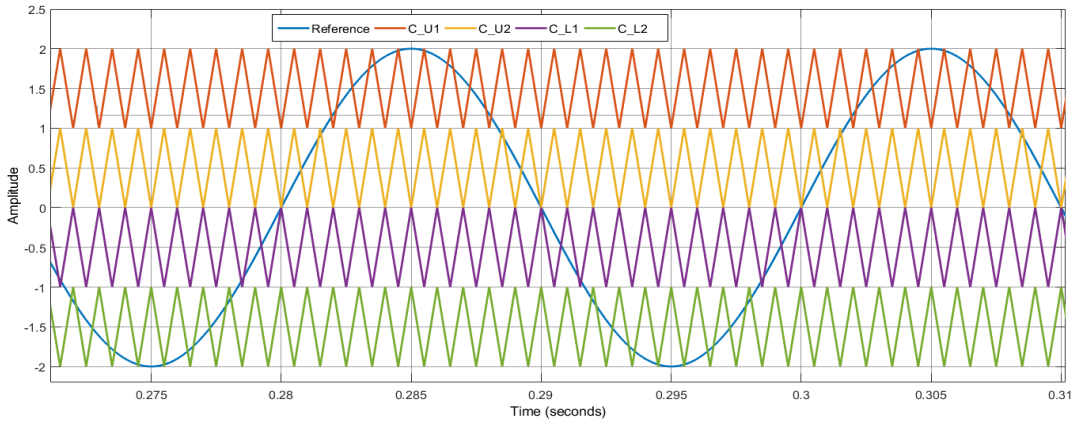


Fig2. 26 Phase Opposition Disposition (POD) PWM

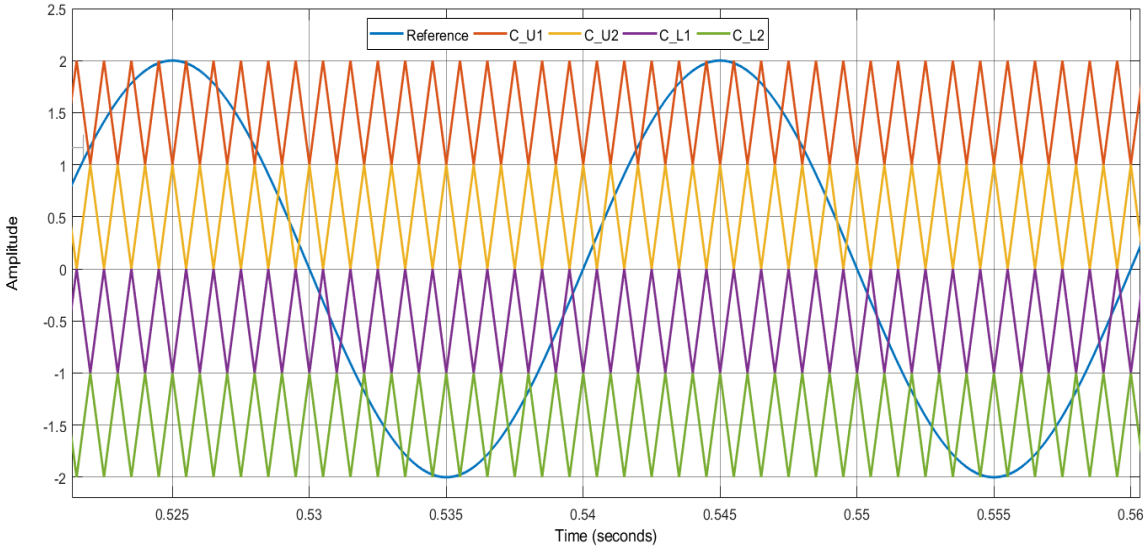


Fig2. 27 Alternate phase Opposition Disposition (APOD) PWM

Other multi-carrier such as carrier overlapping PWM (CO-PWM), variable frequency carrier PWM (VFC-PWM) and switching frequency optimal PWM (SFO-PWM) can also be used.

2.7. Evaluation of computer modeling Platforms

Computer based simulation platforms gives a reasonable and cost effective ways for evaluating performances of complex systems such as smart transformer (ST) integrated in smart distribution grid (SDG). Extensive evaluation of literature showed that a great variety of modeling and simulation platforms are being in use to evaluate the performances of three phase three stage ST. Application specific models such as switching model, average model and steady state models were developed in various simulation packages to analyze the main characteristics of the system.Table.2.4 below shows a review of simulation platforms used for modeling and performance analysis of three phase ST.

Table2. 4 Modeling platform of three phase ST

ST Configuration	Type of Switch model	No of ST stages	ST functionalities	Modeling Tool	Reference
Multilevel	switching model	Single	Bidirectional	MATLAB/ Simulink	[83]
Multilevel	Average Model	3-stage	Bidirectional	MATLAB/Simulink	[84]
2-Level	Average Model	3-stage	Bidirectional	MATLAB/ Simulink	[85]
Multilevel	switching model	3-stage	Bidirectional	MATLAB/ Simulink	[86]-[87]
2-Level	Average Model	3-stage	Bidirectional	MATLAB/ Simulink	[88]
2-Level	switching model	Single	Bidirectional	MATLAB/ Simulink	[89]
Multilevel	switching model	3-stage	-	MATLAB/PLECS	[90]
2-Level	switching model	Single	Bidirectional	PLECS	[91]
Multilevel	Phasor based	3-stage	Bidirectional	PLECS/SPICE	[92]
Multilevel	switching model	3-stage	Bidirectional	PSCAD/EMTD	[93]
2-Level	switching model	3-stage	Bidirectional	PSCAD/EMTD	[94]
Multilevel	switching model	3-stage	Bidirectional	PSCAD/EMTD	[95]
2-Level	Average Model	3-stage	Bidirectional	PSCAD/EMTD	[96]-[97]
Multilevel	switching model	3-stage	Bidirectional	EMTP/ATP	[98]
2-Level	switching model	3-stage	Bidirectional	EMTP/ATP	[99]-[100]
Multilevel	switching model	3-stage	Bidirectional	PSIM	[101-102]
2-Level	Average Model	3-stage	Bidirectional	DigSilent	[103]
Multilevel	switching model	3-stage	-	Simplorer	[104]
2-Level	Steady state model	3-stage	Bidirectional	OPENDSS	[105]

Cross evaluation of the options for power electronics building blocks (PEBB) parameters to be used in ST design shows that Simulink/PLECS platform enables us to include the thermal parameters and magnetic parameters which can be filled from device manufacturer data sheet. SIMULINK /PLECS simulation package was used in this project work

2.8 Semiconductor Losses

A power electronic system with high power densities and compact packaging demands critical thermal management. Semiconductor switches and ohmic resistors (stray resistance) are intrinsic components which dissipate thermal losses in power electronic system. Power semiconductors dissipate losses due to their non-ideal nature. These losses can be classified as conduction losses, switching losses and blocking losses. Blocking loss can be neglected as it is caused by very small leakage current. For Semiconductor switches with an integrated diode such as the IGBT/MOSFET with freewheeling diode model losses should be individually specified for both the semiconductor switch and diode. In this dissertation work, IGBT/MOSFET integrated with freewheeling diode is used as semiconductor switch to realize the PEBB and illustrations done refer to these devices. Various types of losses occurring in semiconductor switch are illustrated in Fig.2.28

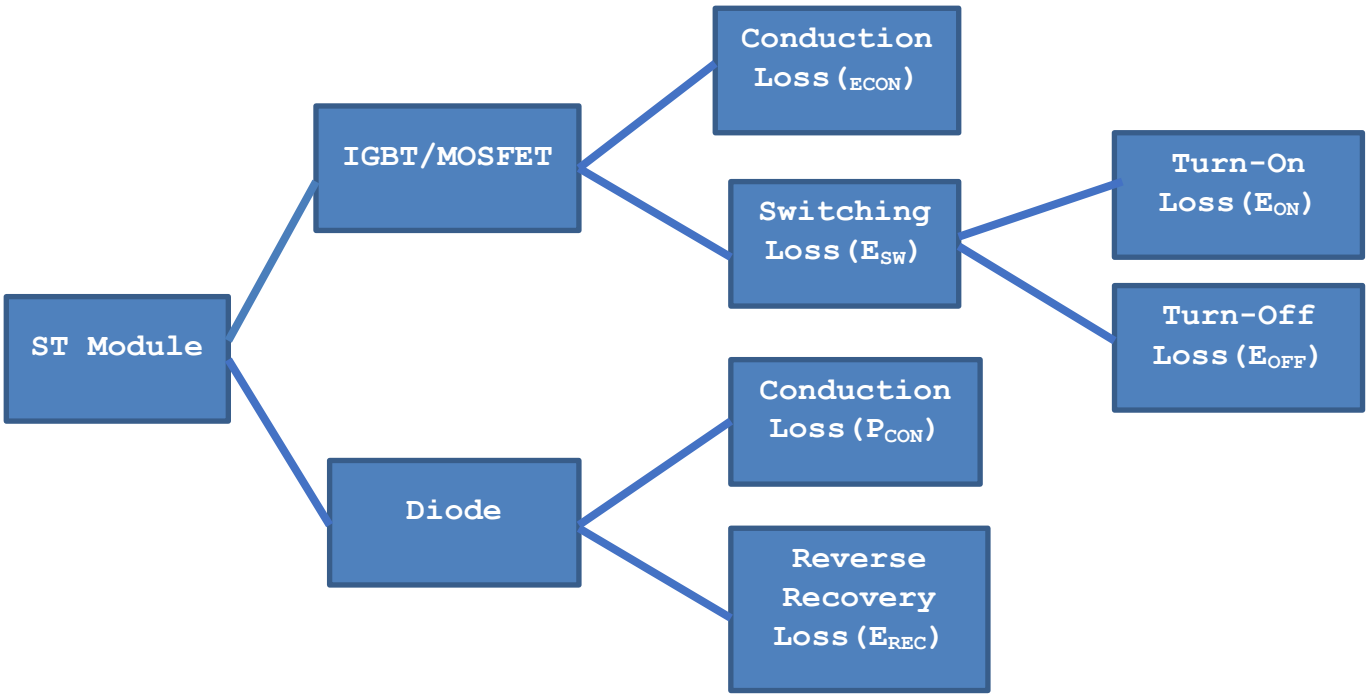


Fig2. 28 Loss hierarchy of semiconductor switch integrated with diode

Conduction losses are the losses that happen while the IGBT or fast recovery diode is on and conducting current. The product of the on-state voltage and the on-state current gives the total power dissipation during conduction. However, multiplication of the total dissipated power by the duty factor in PWM applications is a must to obtain average power dissipation.

The total conduction loss dissipated by the IGBT integrated with fast recovery diode is given by the following equation.

$$\mathrm{Pcond}(tot) = \mathrm{Pcond}(IGBT) + \mathrm{Pcond}(Diode) \quad (2.25)$$

$$\mathrm{Pcond}(IGBT) = \frac{1}{T}\int_0^T [V_{CE}(t) * I_C(t)]dt \quad (2.26)$$

Linearising equation (2.26) to connect the datashet values from the device manufaturer gives the following conduction loss equations as follow:

$$\mathrm{Pcond(IGBT)} = \mathrm{V_{CEO}} * \mathrm{i} + \mathrm{R_O} * \mathrm{i}^2 \quad (2.27)$$

$$\mathrm{Pcond(Diode)} = \mathrm{V_{DO}} * \mathrm{i} + \mathrm{R_{DO}} * \mathrm{i}^2 \quad (2.28)$$

Where, V_{CEO} and V_{DO} are on-state temperature dependent voltages and R_O and R_{DO} are temperature dependent on-state resistance

The best practice to obtain the on-state characteristic terms VCE0 and R0 is to utilize device output characteristic figure at maximum junction temperature -TJ (max), as shown in Fig.2.29 and Fig.2.30

Different values of gate-emitter voltage (V_{GE}) can be used to calculate the characteristic values, but in this work the DYNEX approach is followed for which the output curve for V_{GE} value of 15V is used.

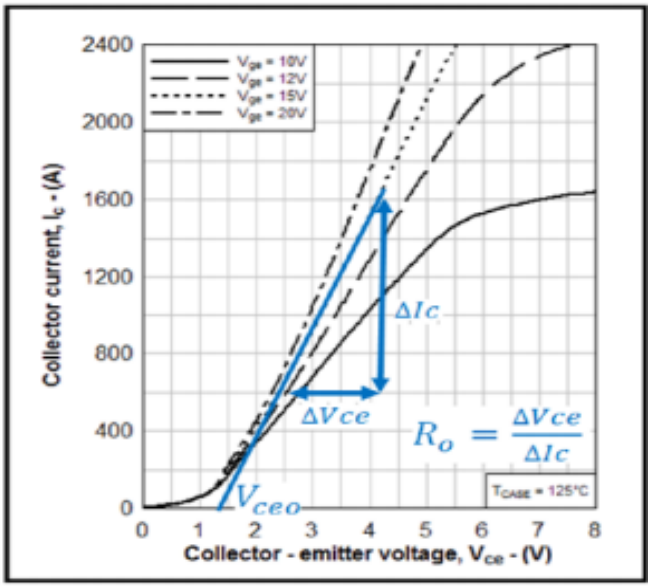


Fig2. 29 IGBT output characteristics

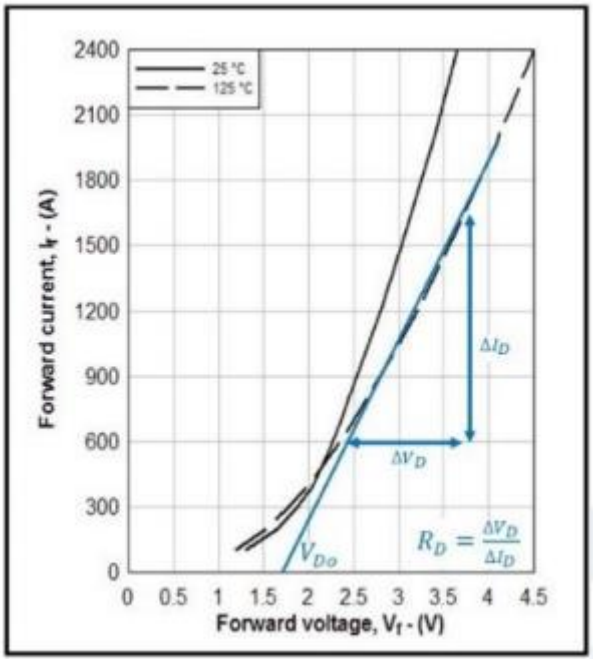


Fig2. 30 Diode R_O and V_{DO} derivation from output characteristics

VCE0 and VD0 are determined by establishing a line on the output characteristics figure (Fig. 29 and Fig. 30) and determining the X-intercept.

The average conduction loss of IGBT can be computed by the following equation:

$$\text{Pav}(cond) = V_{CE(S)} * I_C * \delta \qquad (2.29)$$

Where, δ refers to device duty cycle

The transitions from on-state to off-state and vice versa do not occur instantaneously and causes a loss known as switching losses During the on-to-off or off-to-on switching interval, both the current flowing through and the voltage across the device are substantially greater than zero which leads to large instantaneous power losses.

. The dynamic switching and conduction characteristic curve of IGBT for inductive loading during one cycle is illustrated in the Fig.2.31 below ((http://www.dynexsemi.com/)

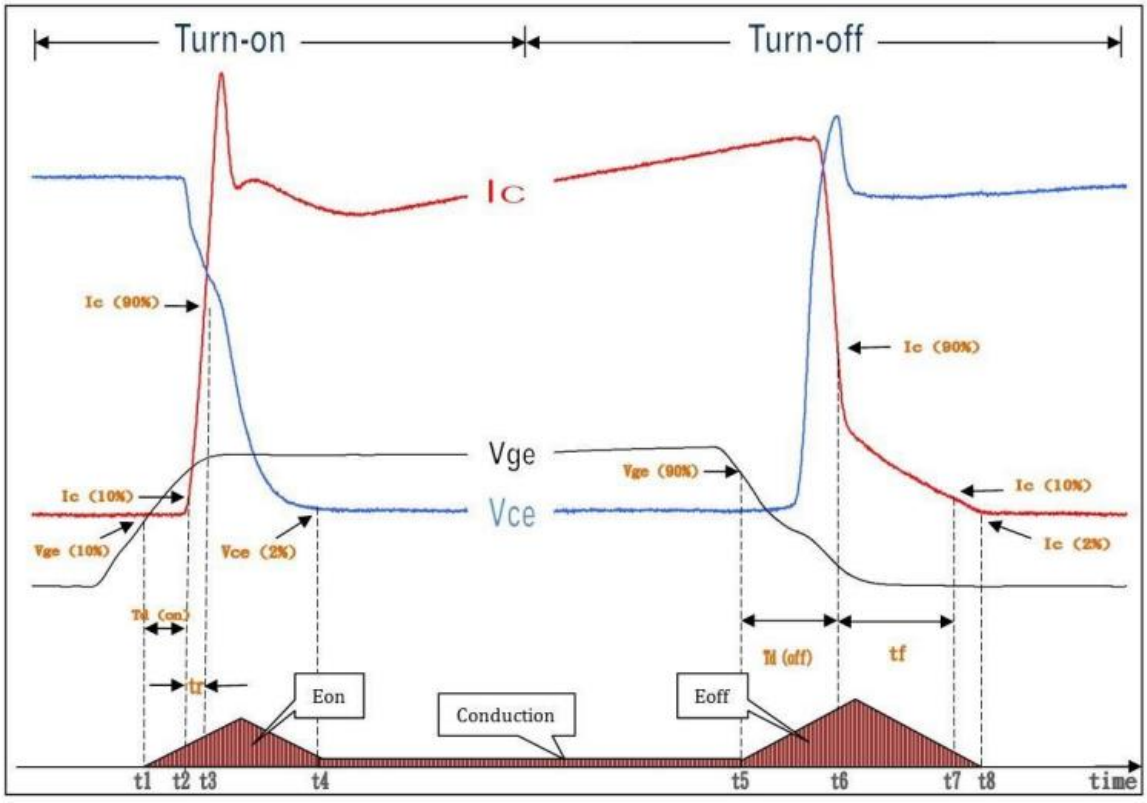


Fig2. 31 Semiconductor loss curve for inductive load

The instantaneous power integrated over one switching transition gives the switching energy for one transition at the applied collector current. In the datasheets of most IGBT, the switching energies are derived as a function of collector current. For fast recovery diodes (FRD), a reverse recovery losses which is a mechanism similar to IGBT happen during the turn off period of FRD, causing flow of temporary non-zero reverse current and voltage as shown in Fig.2.32

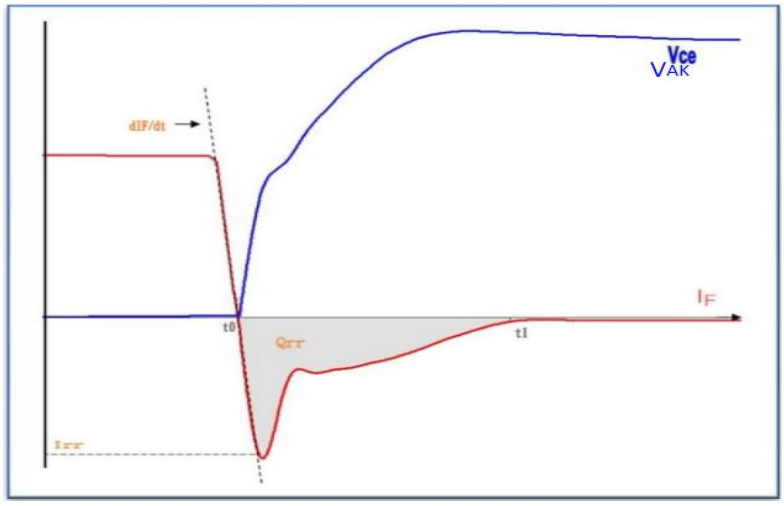


Fig2. 32 Fast recovery diode turn-off transition

The basic equations to determine the power losses due to switching of an IGBT and FRD are given bellow:

$$\text{Psw}(IGBT) = (E_{ON} + E_{OFF}) * \quad f_{SW} \tag{2.30}$$

$$\text{Psw}(FRD) = E_{rec} * \quad f_{SW} \tag{2.31}$$

The energy required for switching i.e. the turn-on energy (E_{on}), the turn-off energy (E_{off}) in the IGBT and the reverse recovery energy in the diode (E_{rec}) are dependent on collector current, collector voltage, gate resistance and junction temperature as shown below in Fig.2.33

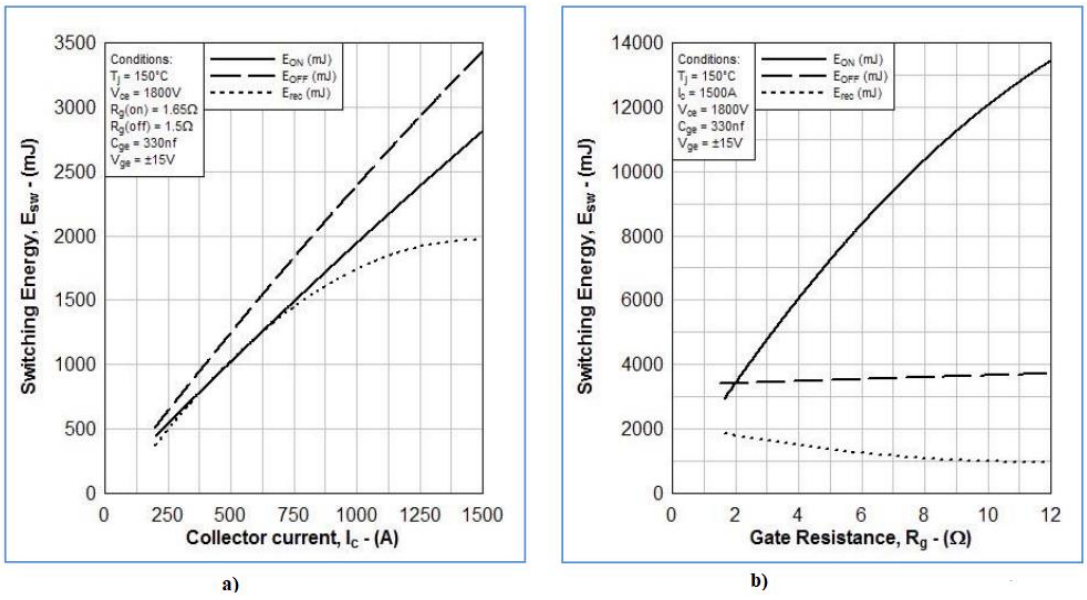


Fig2. 33 Switching energy Vs collector current and gate resistance graph

Ohmic losses are dissipated by resistance of components such as resistors, inductors and capacitors. It is calculated by

$$P(\text{ohmic}) = R_O * i^2 \quad = \quad V^2 / R \qquad (2.32)$$

From determination of the conduction losses and switching losses of IGBT and FRD, it is possible to obtain total loss for reasonably quantifying the efficiency of a system and junction temperature of the devices.

$$P(\text{tot}) = P_{\text{Cond}}(\text{IGBT}) + P_{\text{SW}}(\text{IGBT}) + P_{\text{Cond}}(\text{FRD}) + P_{\text{SW}}(\text{FRD}) \qquad (2.33)$$

A summary of the valid voltage and current regions for defining conduction and switching losses for the different types of semiconductors is given in Table.2.3 below:

Table2. 5 Valid current and voltage region for defining loss

	Diode		Switch		Switch with Diode			
					Switch		Diode	
	V	I	V	I	V	I	V	I
Conduction Loss	+	+	+	+	+	+	-	-
Switching Loss	-	+	+	+	+	+	+	-

2.9 Thermal Modeling of Power Semiconductor Switch

With increasing demands for compact packaging and high power density for power electronic systems, thermal management becomes more critical in system design. The heat produced by power semi-conductors losses affects the junction temperature, whose value will affect semiconductor losses in turn. Therefore, estimation of junction temperature and power losses that occurs in IGBTs and diodes is based on thermal models (Z. Luo, 2002; K. Ma, et'al., 2015). For safety reasons, the junction temperature during operation should be always under a maximum value, usually specified by the manufacturer. The main components of semiconductor thermal model are heat sink (hs), thermal resistance (Rth) thermal capacitance (Cth), controlled current source and ambient temperature (http://www.plexim.com, user Manual). A heat sink absorbs the thermal losses dissipated by the components within its boundaries. At the same time, a heat sink defines an isotherm environment and propagates its temperature to the components which it encloses. Heat conduction from one heat sink to

another or to an ambient temperature is modeled with lumped thermal resistances and capacitances that are connected to the heat sink. The thermal equivalent circuit of a component describes its physical structure in terms of thermal transitions from the junction to the case. Each transition consists of a thermal resistance (k/W) and a thermal capacitance (J/k) from its junction-to-case which are analogous to electrical resistance (Ω) and capacitance (F). The heat flow from the component to its case is described by controlled current source. The thermal model of semiconductors can be done for a single component or group of many components sharing a common heat sink. The thermal model of single IGBT and group of many IGBT with integrated FWD sharing common heat sink is shown in Fig.2.34-Fig.2.35 below.

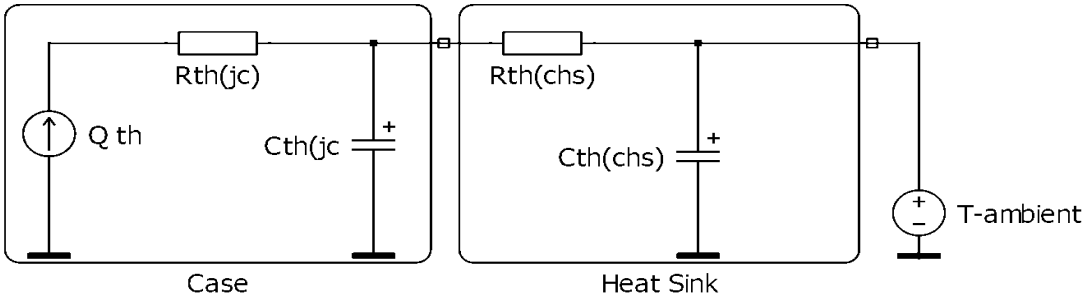


Fig2. 34 Thermal model of Single IGBT

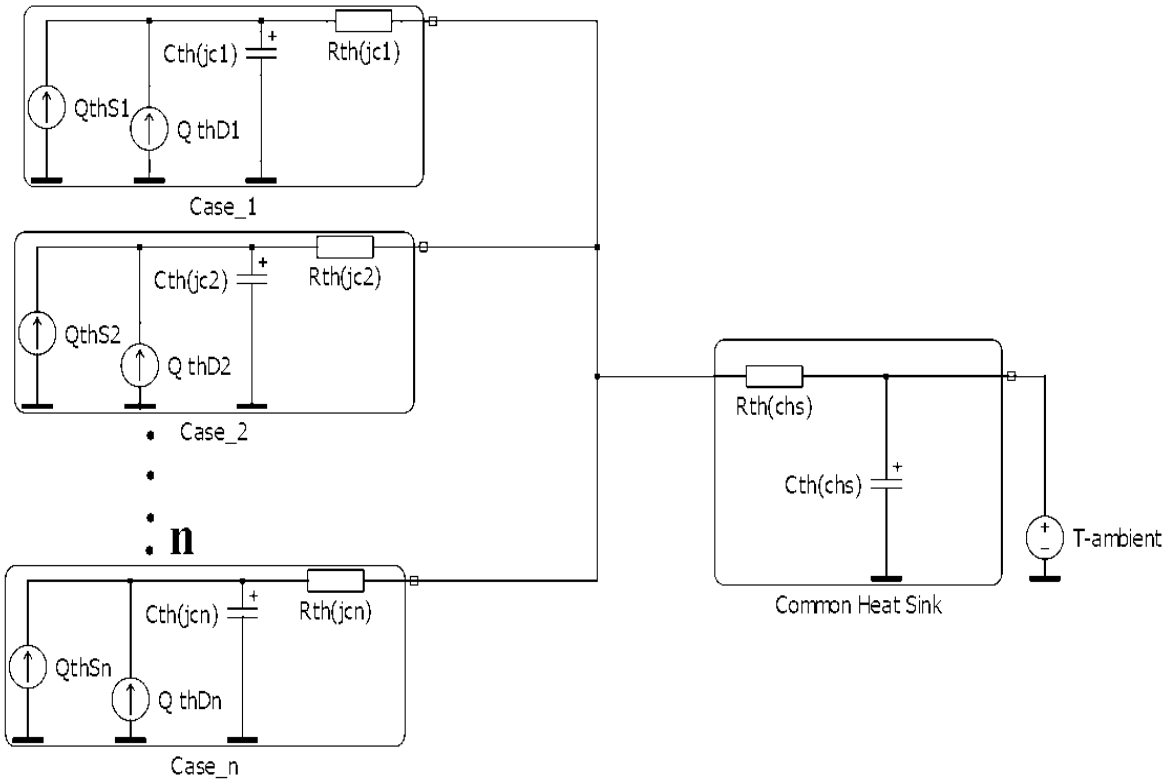


Fig2. 35 Thermal model of many IGBT with integrated FWD

As it is viewed from these figures, the thermal behavior of semiconductors is modeled by the RC circuits. In these figures, Rth (jca) and Cth (jc) are the thermal resistance and capacitance between semiconductor junction and semiconductor case, Rth(chs) and Cth(chs) are thermal resistance and capacitance between semiconductor case and heat sink.. The controlled current sources represent energy losses in each semiconductor device which can be obtained by analytical method as discussed earlier or using lookup table where thermal descriptions of devices is filled from manufacturer's datasheet.

Piecewise linear electronics circuit and system (PLECS) uses Look up table, formula or combination of lookup table and formula approach to determine conduction and switching losses. Lookup approach uses interpolation and extrapolation methods to find the device loss values based on the set of data points taken from datasheet. Thermal implementation model for single IGBT integrated with FRD is given in Fig.2.34. For power electronic system containing multiple switches, the same approach can be used with a common heat sink shared among all semiconductor switch packages.

CHAPTER THREE

DESIGN AND MODELING OF MODULAR ST STAGES

An ST aimed for electric power distribution application interfaces medium voltage (MV) grid with low voltage (LV) grid, providing a galvanic isolation between them in addition to its ancillary functionalities such as reactive power control and compensation, interfacing of distributed generations, improvement of reliability, and blocking of harmonic propagation. A typical design procedure of ST might begin with collection of relevant distribution system specifications (voltage and power level) followed by selection of suitable ST architecture, power converter topologies, power electronic building block (PEBB) configuration in consideration with the overall design requiremens such as reliability, efficiency, cost and functionalities. Fig.3.1 shows an overview of design procedures of ST for distribtion grid application

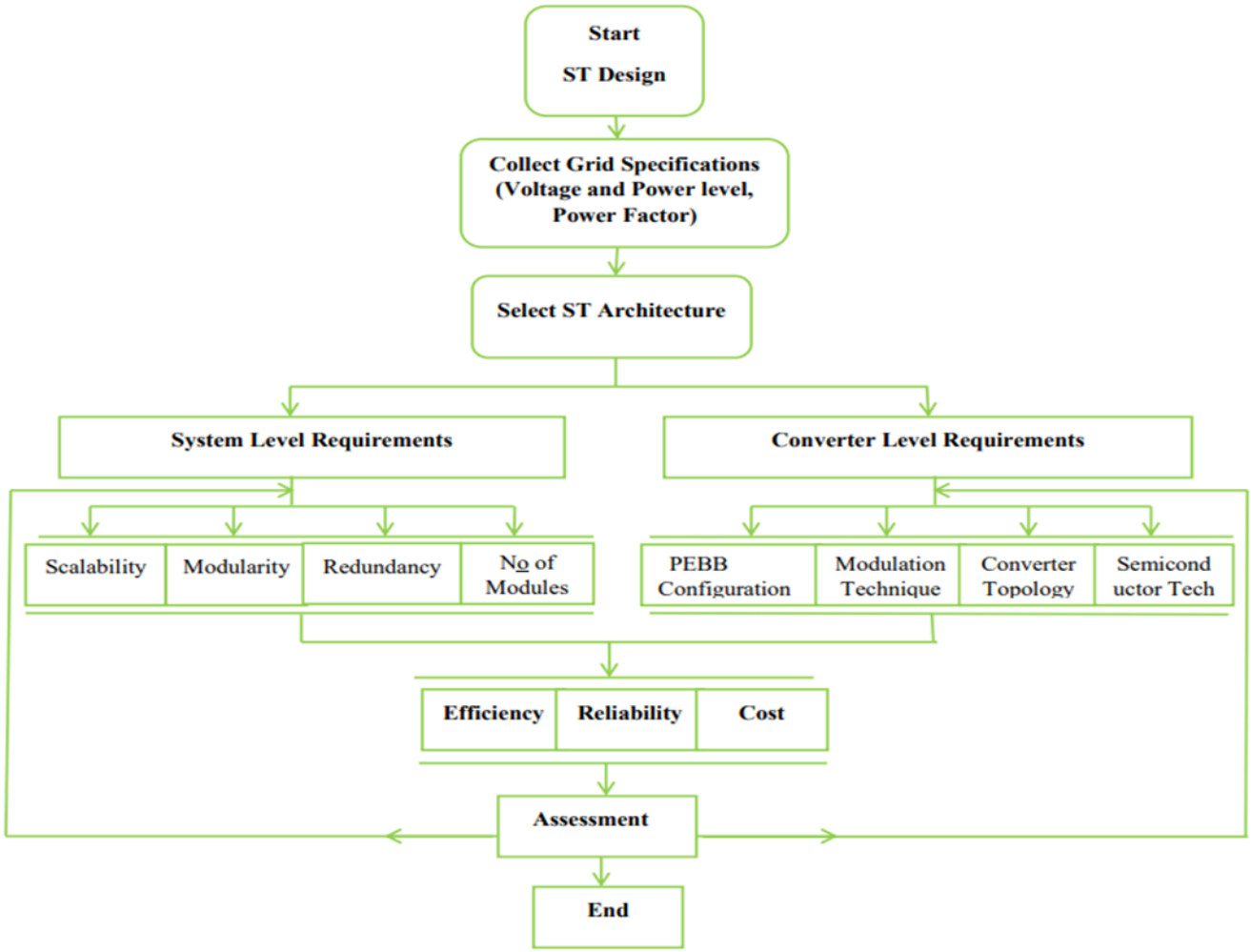


Fig3. 1 ST Design Procedure

3.1 Design and Modeling of Front-Side Stage of Modular ST

The MV side of a three stage modular ST is basically an AC-DC converter that controls the active and reactive power consumed from the grid, in addition to regulating the voltage for the next stage, i.e. the DC-DC stage (M. Liserre, et'al., 2016; X. She, et'al., 2013). Connection of this stage to a three phase AC source is done via RL filter. To handle the large voltage level of this stage, multilevel topologies are the most preferred and advantageous choice for constructing the front side MV stage (I. Villar, et'al., 2009; J. Reinert, et'al., 2001; J. Li,et'al.,2001; C. Meyer,2007). Since a three phase modular ST is going to be designed, the choices are confined to two converter topologies: the modular multilevel converter (MMC) and the Cascaded H-Bridge -CHB (Lesnicar, A , et'al.,2003). The MMC and CHB topologies are presented in Fig. 3.2 (a) and (b), respectively, together with their basic PEBB topology.

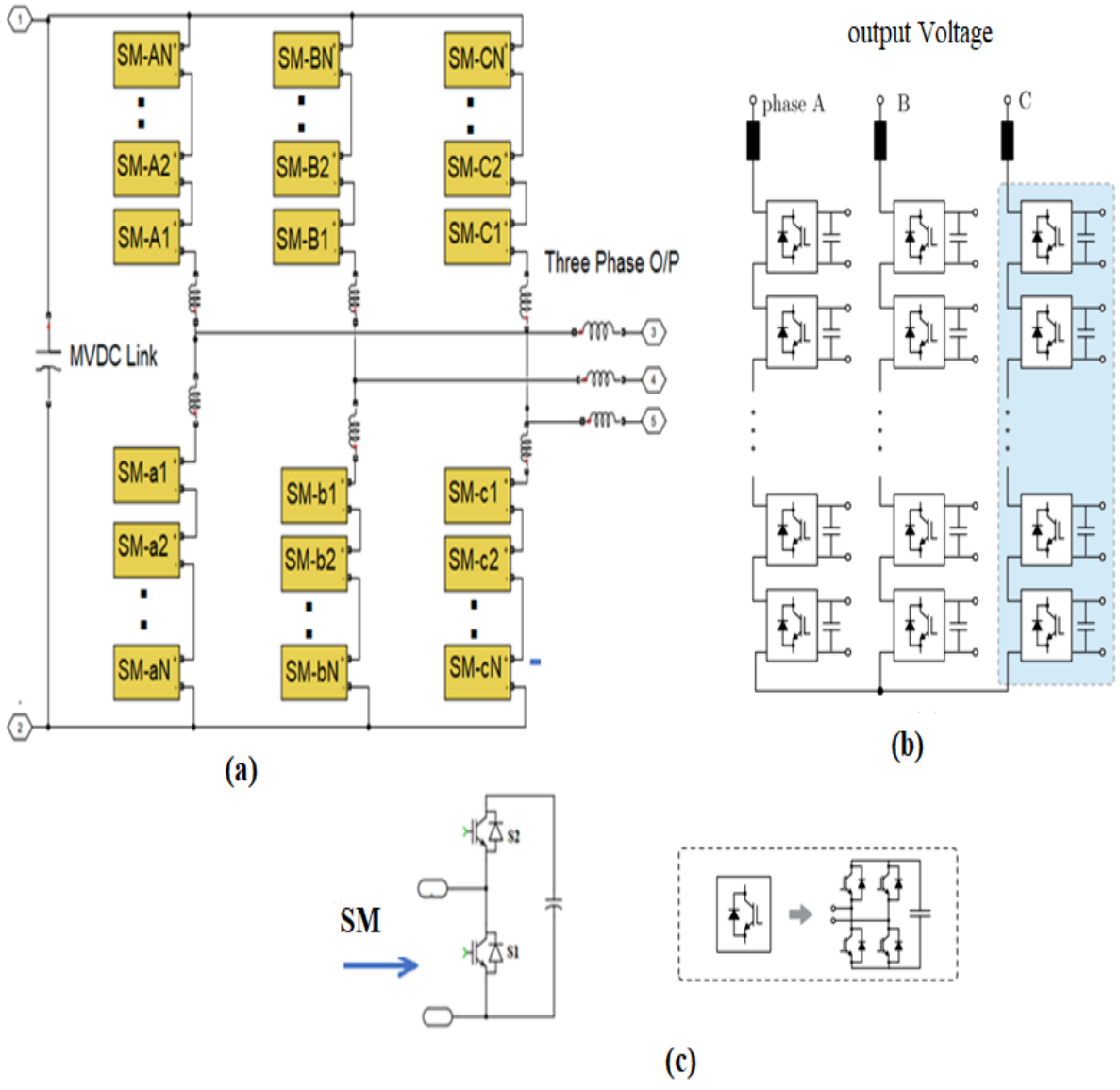


Fig3. 2.Front-side modular converter: a) MMC topology, b) CHB topology, c) Basic cell

These two modular converters share same features, such as reduced filter size, reduced blocking voltage over the semiconductors, modularity, as well as scalability in voltage and power. This star-connected quality enables their application in different places with different grid specifications without major alterations in the design of the basic module. To avoid confusions arising because of many similarities in the terminology, Akagi proposed a double star connected chopper cell for MMC and single star connected bridge cell for CHB in (H. Akagi,2011).

The CHB converter is realized by serial connection of several modules creating one phase, and the three phases are, as displayed in Fig. 3.2 (b). It is a well-known topology and widely used for MV applications in industrial sector. Even though other topologies can be employed as the basic cell, the H-bridge is widely used as the basic cell for CHB converter. The major drawbacks of the CHB converter are lack of MVDC link for connection of MV loads/ distributed generation sources, the need of separate sources connected to each module and need of several modules to implement the next stage i.e DC-DC stage of ST (J. Huber ,et'al.,2016; R. H. Baker ,1971; L. G. Franquelo ,et'al., 2008; L. M. Tolbert ,et'al.,1999; M. Malinowski ,et'al., 2010; F. Wang,et'al.,2014). These drawbacks are avoided by using an MMC.

Glinka and Marquardt introduced the first MMC in 2003 as a solution for high voltage application (J. Huber,et'al.,2017). It is made by series connection of cells forming upper and lower arms, which are connected through two inductors (Larm) to the AC grid, as illustrated in Fig. 3.2 (a). Many topologies at cell level can be used, but the half-bridge topology is the mostly utilized one. It provides few count parts, as well as few semiconductors on the current path, reducing the conduction losses, when compared to other possible topologies. This modular converter possess a striking features of MVDC link, which favors its high degree of freedom in connecting distributed generations and storage devices. Moreover, use of MMC gives a greater flexibility to decide the number of modules in DC-DC stage of ST. In this project work, MMC is used in design and modeling of front stage converter of ST with a freedom to utilize the MVDC link and dual active bridge converter in the DC-DC stage.

The half bridge IGBT power module which builds an MMC can have four states during operation, which is shown by Fig.3.3

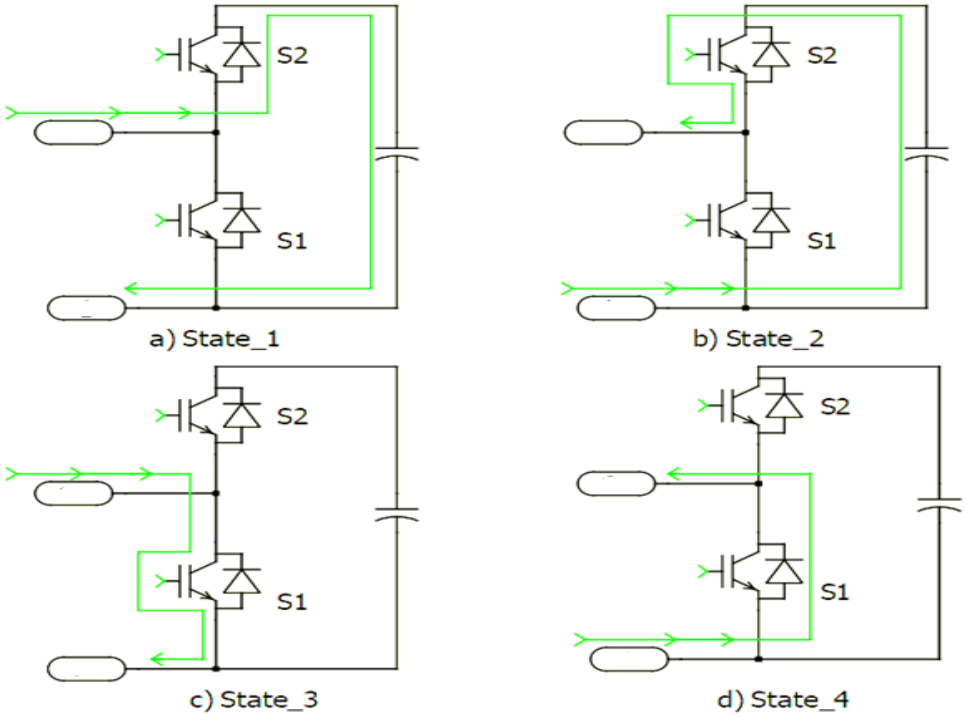


Fig3. 3 Operating states of half bridge sub-module

The half-bridge sub-module (Fig 3.3) is made of two switches ($S1$ and $S2$) and a capacitor. The switches can be of IGBT/MOSFET and an antiparallel diode. To avoid short circuiting of the capacitor voltage, one switch operates at a given instant of time. The direction of current in the sub-module decides whether the capacitor is in charging or discharging mode. During conduction of the only one valve, either the IGBT or the fast recovery diode will conduct, depending on the current direction.

Conduction of upper valve (S2) in Fig3.3), the SM enters in to either state-1 or state-2 based on the corresponding arm current. When the SM is in state-1, the current charges the capacitor and it discharges the capacitor when the SM is in state-2. The SM has output voltage equal to its capacitor voltage when it is in either satae-1 or state-2 and the SM is said to be in "on" or inserted state. In the same manner, turning on of S1 derives the SM to either in state 3 or 4 where the capacitor voltage remains unchanged and the SM output voltage becomes zero. When the SM is in either state 3 or 4, it is said to be in the "off" state, or "bypassed".

3.1.1 Mathematical Analysis of MMC

An MMC generally contains N number of series connected sub-modules in one phase arm, both in upper and lower arms resulting in total of 2N sub-modules in one leg (Fig.3.2a). For filtering out harmonics and limiting the phase leg currents, inductance and resistances are used at grid side and phase arms of the converter.. Each leg of the three phases operates so that the total voltage of the DC link is applied across its terminals. Its equivalent circuit is shown in Fig.3.4 below. In the single phase equivalent circuit of MMC i_a and U_a represent phase 'a' current and voltage, U_{UM} represents upper sub-module voltage, U_{LM} represents lower sub-module voltage, U_{dc} represents DC link voltage, L_g and R_g represent grid side inductance and resistance, L and R represent phase arm inductance and resistance, i_{UM} and i_{LM} are upper and lower arm sub-module currents and i_{Cir} is circulating current.

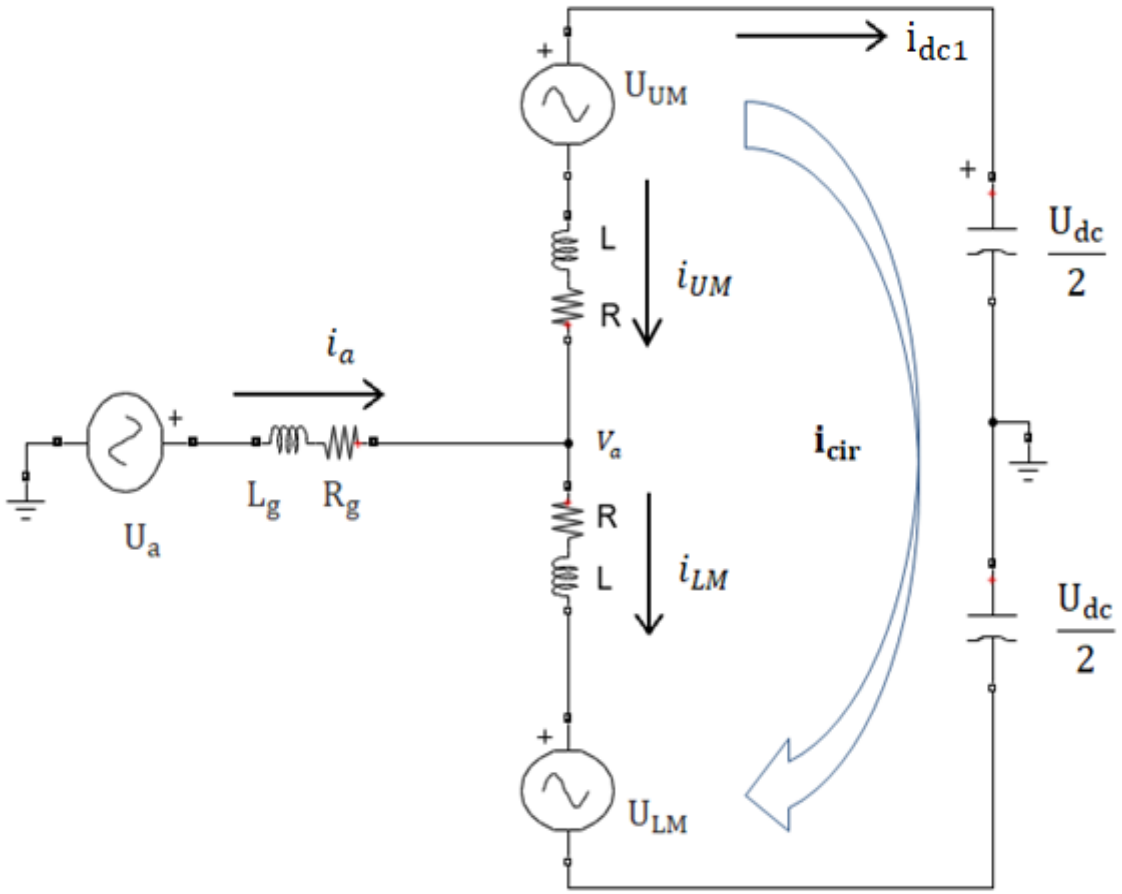


Fig3. 4 Single phase circuit of MMC

In its basic operation, the number of sub-modules in the phase leg which are in ON state at one instant of time should be equal to N (number of sub-modules in the arm). Two independent modes of operations are possible in the analysis of phase leg of MMC. These are the common mode operation and differential mode operation. In common mode of operation, the common current which flows through the upper and lower sub-module is half of sum of upper arm and lower arm currents, which equals half of phase current. In the differential mode of operation, the differential or circulating current, having a value equals half of the difference between the upper sub-module current and lower sub-module current circulates within the modules . It consists of a dc and ac components. The dc component is essential to keep the phase-leg energized but the ac components can be eliminated to reduce the losses and increase the efficiency of the MMC.

The current through upper sub-modules and lower sub-modules when considering differential mode operation are given by:

$$\mathrm{i_{UM}} = \frac{\mathrm{i_a}}{2} + \mathrm{i_{Cir}} \tag{3.1}$$

$$\mathrm{i_{LM}} = \mathrm{i_{Cir}} - \frac{\mathrm{i_a}}{2} \tag{3.2}$$

Addition of (3.1) and (3.2) gives the expression for circulating current as follows:

$$\mathrm{i_{Cir}} = \frac{\mathrm{i_{UM}} + \mathrm{i_{LM}}}{2} \tag{3.3}$$

Using KVL to the upper loop of Fig.3.4, the following voltage equation can be obtained:

$$V_a - V_{mU1} - V_{mU2} - \cdots - V_{mUN} - L\frac{d\mathrm{i_{UM}}(t)}{dt} - R\mathrm{i_{UM}} - \frac{Vd}{2} = 0 \tag{3.4}$$

, where $V_{mU1}\ldots\ldots V_{mUN}$ are sub-module voltages from first sub-module to N^{th} sub-module.

In compact form, equation (3.4) is written as:

$$\sum_{j=1}^{N} V_{mUj} = -V_a - L\frac{d\mathrm{i_{UM}}(t)}{dt} - R\mathrm{i_{UM}} + \frac{Vd}{2} \tag{3.5}$$

The voltage equation for lower leg can be obtained in the same manner by applying KVL

$$\sum_{j=1}^{N} V_{mLj} = V_a - L\frac{d\mathrm{i_{LM}}(t)}{dt} - R\mathrm{i_{LM}} + \frac{Vd}{2} \tag{3.6}$$

Letting $\sum_j^N V_{mUj}$ be U_{MU} and $\sum_j^N V_{mLj}$ be U_{ML}, subtracting equations (3.6) from (3.5) and using equations (3.1) to (3.2) gives the following expression of V_a

:

$$V_a = \frac{U_{LM} - U_{UM}}{2} + \frac{L}{2}\left(\frac{d\mathbf{i_a}}{dt}\right) + \frac{R}{2}(\mathbf{i_a}) \qquad (3.7)$$

The grid side voltage V_g can be given by the following expressions

$$V_g = U_a + R_g(\mathrm{i_a}) + L_g\frac{di_a}{dt} \qquad (3.8)$$

Substitution of equation (3.6) in in equation (3.7) gives the following equation:

$$V_g = \frac{U_{LM} - U_{UM}}{2} + \frac{L}{2}\left(\frac{d\mathrm{i_a}}{dt}\right) + \frac{R}{2}(\mathrm{i_a}) + R_g(\mathrm{i_a}) + L_g\frac{di_a}{dt} \qquad (3.9)$$

Rearrangement of equation (3.9) gives the following reduced form equation:

$$\mathrm{V_g} = \mathrm{U_{eq}} + \mathrm{R_{eq}}(\mathrm{i_a}) + \mathrm{L_{eq}}\frac{\mathrm{di_a}}{\mathrm{dt}} \qquad (3.10)$$

Where $\mathrm{U_{eq}} = \frac{\mathrm{U_{LM} - U_{UM}}}{2}$

$$\mathrm{R_{eq}} = \mathrm{R_g} + \frac{\mathrm{R}}{2}$$

$$\mathrm{L_{eq}} = \mathrm{L_g} + \frac{\mathrm{L}}{2}$$

By using equation (3.9) the most simplified circuit of single phase MMC shown in Fig.3.4 is shown below in Fig.3.5

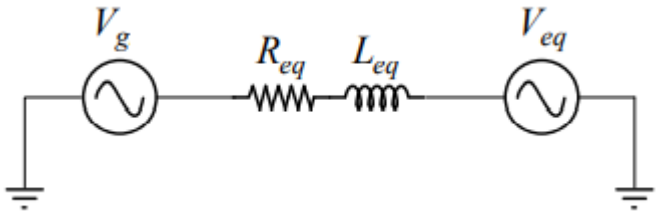


Fig3. 5 Equivalent circuit of MMC

Addition of KVL equations for upper phase arm (3.5) and lower phase arm (3.6) gives the following expression:

$$Vd - \left(\sum_{j=1}^{N} V_{mUj} + \sum_{j=1}^{N} V_{mLj}\right) = L\frac{d(\boldsymbol{i_{UM}}(t) + \boldsymbol{i_{LM}})}{dt} + R(\mathbf{i_{UM}} + \mathbf{i_{LM}}) \qquad (3.12)$$

If the MMC is controlled to operate in rectifier mode, the sum of upper arm and lower arm voltages is greater than DC voltage; the addition of upper arm and lower arm currents equals total dc current (i_{dc}), power flow from AC side to DC link and the equation becomes:

$$\mathrm{Vd} - \left(\sum_{j=1}^{N} \mathrm{V_{mUj}} + \sum_{j=1}^{N} \mathrm{V_{mLj}}\right) = \mathrm{L}\frac{\mathrm{d}(\mathbf{i_{dc}}(t))}{\mathrm{dt}} + \mathrm{R}(\mathbf{i_{dc}}(t)) \qquad (3.13)$$

Alternatively, the MMC can be controlled to operate in inverter mode when the total sum of upper arm and lower arm module voltages is less than DC voltage, allowing power flow from DC link side to grid side.

3.1.2 Design Criteria and MATLAB/Simulink Model of FS-MMC

Procedures of MMC dimensioning include activities such as deciding the rated voltage of the sub-module, the capacitor size requirement in the cell, the arm choke inductance value and number of sub-modules in the phase arm as presented in (J. Kolb, et'al, 2012). By knowing the voltage rating of the distribution grid, the DC bus voltage level for an MMC can be determined. The MVDC bus voltage should be slightly higher than the peak value of the MVAC so as to prevent over-modulation. But, the value of voltage at DC bus should not be much higher than the peak value of the MVAC voltage, because doing so will reduce the modulation index, and thereby introducing a higher harmonic content in the converter's output voltage and current. Knowledge of the blocking voltage of an IGBT helps in deciding a safety factor to be used to determine the capacitor voltage. Device manufactures recommend that the highest voltage an IGBT should block does not exceed 80% of the rated collector-to-emitter voltage (V_{CES}) and the DC voltage should not exceed 50 to 60% of the V_{CES}. The standard voltage ratings of easily available IGBTs are 1.2kV, 1.4kV, 1.7kV, 3.3kV and 6.5kV. By taking the nominal voltage of the DC bus for MMC, the number of modules in each arm can be calculated by selecting one of the IGBT modules and applying the required safety factor.

As mentioned in [127], the formula for MV DC voltage is given by:

$$V_{dc} \geq \frac{2\sqrt{2}VL - L}{\sqrt{3}} \qquad (3.10)$$

Using 15kV AC grid voltage, the value of V_{DC} equals 24.5kV. The selected IGBTs voltage rating (V_{CES}) is 6.5kV (Appendix B.4) and the de-rating factor (η) to be used is 0.909.; the number of sub-modules per phase leg arm (N) is given by equation below:

$$N \geq \frac{V_{dc}}{\eta V_{CES}} \qquad (3.11)$$

If the parameter values for V_{dc}, V_{CES} and η are substituted in the above equation, the value of number of sub-modules per phase leg arm to be four (4)

In high power MMC application with high number of sub-modules, sizing and optimizing the sub-module capacitor is an important task. The sub-module capacitors are the only energy source during fault occurrence in MVDC link and hence they should be able to provide energy for at least one cycle. When the sub-module capacitors are inserted in the phase arm of MMC, capacitor voltage fluctuation happens due to the flow of the arm current. One criterion in selecting sub-module capacitors is to suppress these voltage fluctuations to a pre-defined value to meet required specifications. In modular multilevel converter using LS-PWM, sub-module capacitor voltages are not the same and this fact Therefore a sub-module capacitor balancing technique is usually added to the modulation technique to keep the capacitor voltages balanced. However, addition of capacitor balancing technique may not be required if PS_PWM is used.

The sub-module is in inserted mode, its capacitor is charged or discharged based on the direction of the arm current. The capacitor balancing techniques usually rotate the sub-module so that the amount of energy in all sub-modules becomes the same after a few cycles. Integrating the phase arm power between two zero crossings gives the energy value of the voltage source for every half period and sub-module capacitor is designed on the basis of calculated energy.

A sinusoidal arm current and balanced sub-module capacitor voltage is assumed to determine capacitance of the sub-module as a function of energy difference (ΔW_{SM}) stored over one cycle for acceptable ripple (ε) (Thouhidul Islam,2018).

$$C \geq \frac{\Delta W_{SM}}{2\varepsilon V_{C,av}^2} \qquad (3.12)$$

where $V_{C,av}$ is average sub-module capacitor voltage given by $\frac{Vd}{N}$ and ε is voltage ripple and the change in SM energy (ΔW_{SM}) is given by

$$\Delta W_{SM} = \frac{2}{3}\frac{S}{Nm\omega}\left[1 - \left(\frac{mCos\varphi}{2}\right)^2\right]^{\frac{3}{2}} \qquad (3.13)$$

Substitution of (3.13) in (3.12) gives the following new expression for sub-module capacitor:

$$C_{SM} \geq \frac{S}{3NmV_C^2\varepsilon\omega}\left[1-\left(\frac{mCos\varphi}{2}\right)^2\right]^{\frac{3}{2}} \quad (3.14)$$

The arm inductance has a function of filtering out circulating current and limiting arm current in the event of fault. On the basis of resonant frequency formed between sub-module capacitor and arm inductance, the value of arm inductance that enable the MMC to work above resonant frequency is given by the following formula as discussed in (Fazal Muhammad,et'al.,2022; Johannes Kolb,et'al.,2012).

$$L_{arm} \geq \frac{5N}{\omega^2 * C_{SM}} \quad (3.15)$$

, where C_{SM} is the capacitance of an SM; N is the maximum number of sub-modules per arm, ω is the reference frequency. The parameter values suggested above may be tuned after iterative simulation.

Table 3.1 shows the basic distribution system specification and the design value of the passive components and number of sub-modules in phase arm of front side MMC

Table3.1 Front stage system basic specification

Parameters	Value
AC grid Line Voltage(Vg)	15kV
Grid side Inductance (Lg)	10μH
Grid side resistance (Rg)	0.01 Ω
Grid frequency(f_g)	50Hz
Power Factor (PF)	0.9
Converter Switching frequency (fc)	4kHz
CT Maximum Capacity (S)	50kVA
Sub-module arm inductance (Larm)	12mH
Sub-module arm resistance (Rarm)	0.1 Ω
Sub-module arm capacitance (C_SM)	0.1mF
No of Sub-module (SM)	4
Proportional gain (KP)	10
Integral Gain (KI)	100

The MATLAB/Simulink model of FS-MMC of ST sis shown in Fig.3.6 below

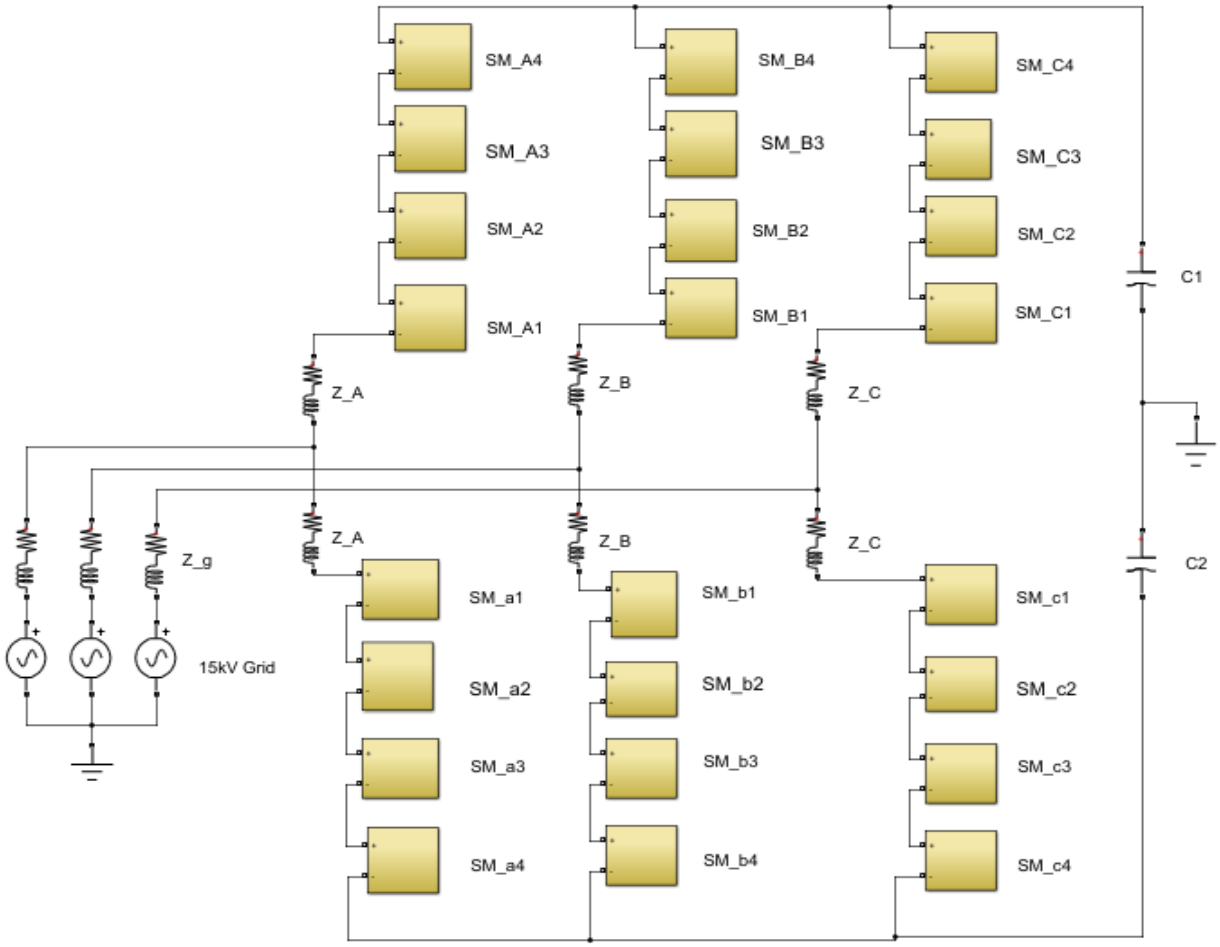


Fig3. 6 FS_MMC Developed in MATLAB/SIMULINK

3.1.3 Modulation and Control of FS-MMC

This section addresses the widely used controllers along with carrier based PWM for MMC operation. In addition, it also treats the application of Fuzzy Inference System (FIS) and Adaptive-Neuro-Fuzzy inference system (ANFIS) as a potential solution to the classical PI controllers. Design of controller and modulation for MMC system is very important for its stable operation The controller design process is complicated because several controllers such as SM capacitor voltage controller, circulating current controller and arm voltage balancing controller are needed in a synchronized manner to achieve a stable operation. In addition to above controllers, rectification and inversion operations also require controllers. On conventional approach, a sending-end MMC terminal controls the dc-link voltage and reactive power for rectification process and a receiving-end terminal controls the active and reactive powers for inversion process

Multi-carrier PWM techniques such PS-PWM and LS-PWM require controller outputs for generating the reference voltage signal to be used in gate triggering circuit. As discussed in section (2.5), PS-PWM need N carriers to produce N+1 voltage levels while LS-PWM requires 2N carriers per arm. Figure 3.7 below describes a typical block diagram of PSC-PWM modulation scheme.

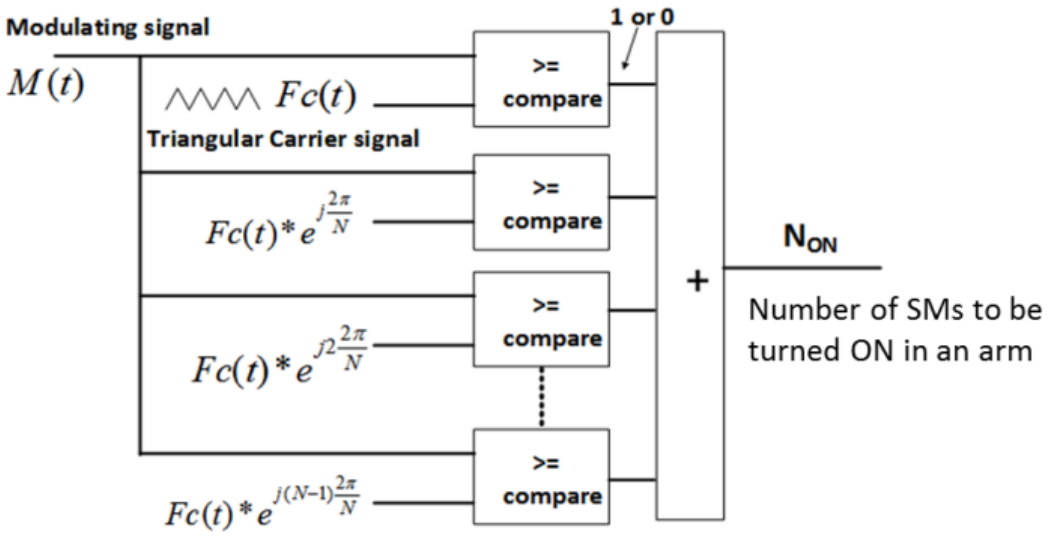


Fig3. 7 PS-PWM technique block diagram (Rostan Rodrigues, 2015).

In the structure, a low frequency modulating signal (usually sinusoidal) obtained from modulating reference generator is continuously compared with a high frequency triangular wave signal (also called as a carrier signal). Due to nature of multiple levels in the converter more sine-triangle comparison blocks are required. The total number of compare blocks is equal to the number of sub-module in an arm of MMC in the case of PS_PWM and twice the number of sub-modules in the case of LS-PWM. The structure for LS_PWM differs from PS-PWM in that consecutive carrier amplitude is level shifted in phase disposition manner, phase opposition manner or alternate phase opposition manner.

The phase angle between consecutive sub-modules in the case of non-interleaved PS-PWM is given by:

$$\theta = 360/\mathrm{N} \qquad (3.16)$$

Interleaved PS-PWM is used to increase the voltage level by 2N without changing the number of carriers but a phase shift of π/N is introduced between the upper and lower leg arms

MATLAB/Simulink model of LS-PWM and PS_PWM are shown below:

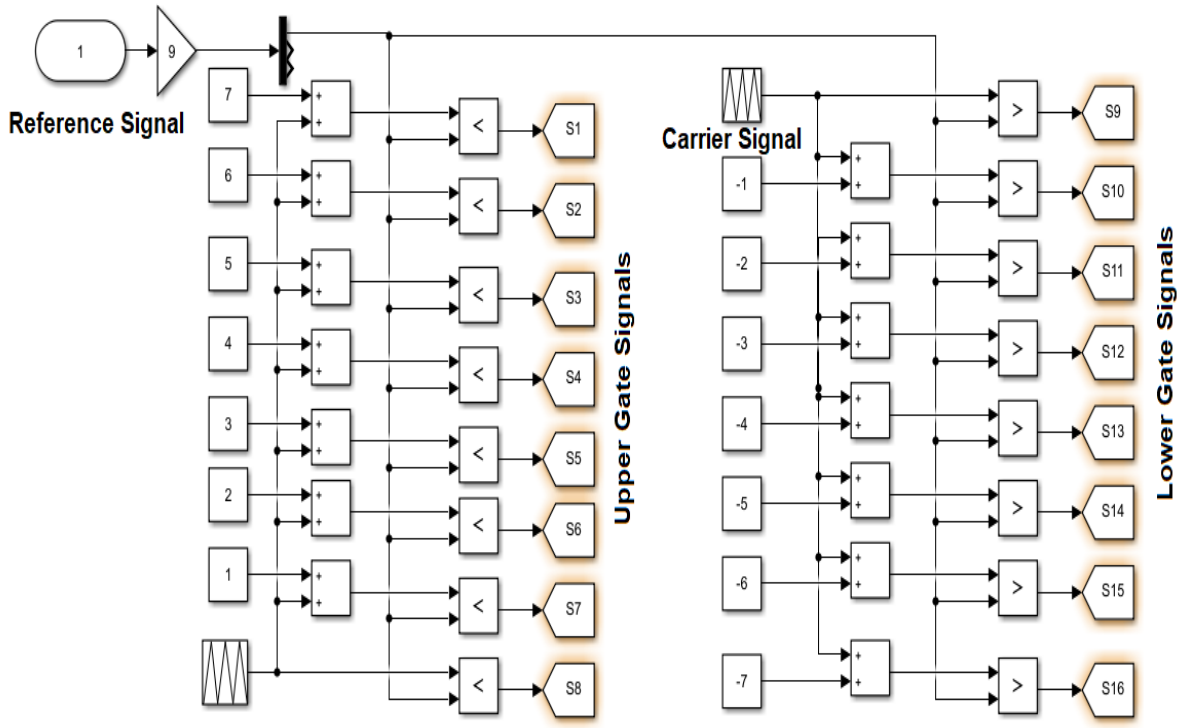


Fig3. 8 MATLAB/Simulink model of LS-PWM for Phase arm

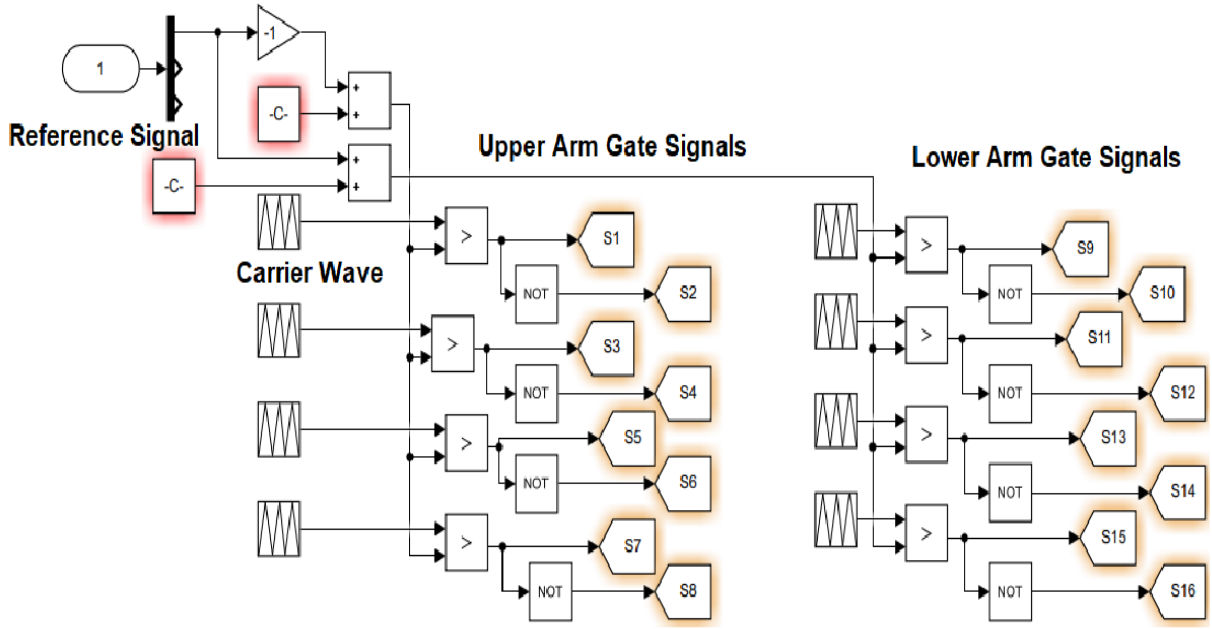


Fig3. 9 MATLAB/Simulink model of PS-PWM for Phase arm

The reference wave or modulating signal of the PWM is generated from the controller circuit. Each MMC phase is modulated with its respective Vref. There is a phase displacement of 120° between the modulating signals. The upper arm modules have negative orientation and hence, the −Vref is taken as the reference while the lower modules are provided with Vref as the reference. Triangular carrier signals having the

same frequency , symmetry and amplitude Ac are used. The carrier frequency (fc) is an integer multiple of the reference signal frequency (fm), which is the same as the grid frequency f_{grid}. Comparisons of carrier waves and the modulating signals are carried out in comparator and the output of the comparator defines the output signal state. The comparator yields a high (digital one) value in the positive half cycle when the value of reference signal is larger than the carrier signal and low (digital zero) otherwise. In the same manner, for the negative half cycle, it yields high output if the reference signal is less than the carrier signal and low (zero) otherwise. Between consecutive carrier signals of each sub-module, there is a phase shift of 2π/N, where "N' stands for the number of sub-modules in each arm. The carrier signals have frequency equal to 12 to 15 times that of the reference signal. In a 9-level MMC modeled in section (3.5) four sub-modules on each arm exist, having total of eight sub-modules exist on each phase leg. The upper and lower arm sub-modules operate in complimentary manner. If $+V_{DC}$ is needed, all the four modules on the upper arm are switched on by activating the switch S2 in each of the sub-modules and the sub-modules in the lower arm are turned off by triggering the switch S1 in each of them. Similarly, if $-V_{DC}$ is needed, all corresponding switches in the sub-modules on the lower arm are enabled and corresponding switches in the sub-modules on the upper arm are disabled. If zero (0) voltage is required, all switches in the modules are turned off, creating a blocking state. When + V_{DC}/2 is required, two sub-modules in the upper and two on the lower arm are enabled. At any instant, the number of sub-modules inserted in each phase leg is equal to the number of SM in an arm (four in our case). For generalized N level converter, N modules are turned on at any given time in each phase leg (L. Wu, etal.,2015).

A Voltage Oriented Control (VOC) strategy is implemented to generate proper reference signals for the modulation technique implemented in this work. Transformation of a stationary 'abc' frame in to rotating 'dq' frame is required in VOC. The positive-sequence grid voltage is used to obtain the grid angle for synchronization purposes by means of a phase-locked loop (PLL). The PLL (3ph) block is closed-loop control system, which tracks the frequency and phase of a sinusoidal three-phase signal by using an internal frequency oscillator. The control system adjusts the internal oscillator frequency to keep the phase difference to 0.

Conversion from 'dq0' frame to abc' frame is carried out by the inverse Park transformation (D. A. Guzman, 2013). The description and MATLAB/Simulink model of

the Park and inverse Park transformations are provided in Appendix A.1. The VOC scheme provides the reference input phase voltage V_K* and upper and lower arm voltages, V_{KU}^* V_{KL}^* respectively.

The widely used conventional closed loop control system is used in VOC. The control structure in VOC is composed of three control loops. The outer power control loop which is on the top level has two controllers, an active power controller and a reactive power controller. The system target specification dictates the references for power. The inner phase current control loop is in the second level of control loop. The inner current controller is used for producing phase currents of desired amplitude (usually symmetric and sinusoidal). The three-phase sinusoidal variables are transformed into two-phase DC components using Park transformation which operates in synchronous "dq" frame domain. The advantage of using this method is that when the dc components are controlled by proportional-integral controllers, zero steady-state error is achieved. The references for inner current controller are obtained from outer power controllers. The output of active power controller is treated as d-axis current controller reference while reactive power controller output is taken as reference for q-axis current controller. Together with the inner current controller, another current controller known as the circulating current controller is required some times. This current controller is used for minimizing the 2nd harmonic circulating current that flows through phase legs. The phase current controller and circulating current controller outputs are summed to form complete modulating signal. The current controllers output is called inner emf (emf_{ref}) or reference phase voltage V_K* (k representing phase a, b or c.). Using equations (3.5) and (3.6), the upper and lower arm reference voltages are calculated. The design and implementation of the aforementioned three controllers is discussed in the following section.

3.1.4. Outer control loop

Controlling the active power (P_{AC}) and the reactive power (Q_{AC}) of the converter is the task of outer control loop. The converter's passive component (impedances) induces in a reactive power in the system. The AC side active and reactive power calculation is done first by transforming the abc parameter in to their dq0 form by using Park transformation (explained in Appendix-A1). The Vq component of the input AC voltage is essentially brought to zero by synchronizing the q-axis with the grid voltage using a Phase Locked Loop (PLL) to generate the reference converter voltage. Hence, the power equations in dq0

frame can be written as:

$$P_{AC} = V_d * i_d \quad (3.17)$$

$$Q_{AC} = V_d * i_q \quad (3.18)$$

In the above equations of P_{AC} and Q_{AC}, Vd is considered as constant because the grid reference is always constant. Measurement of mismatch between the reference Q_{AC}* and the measured Q_{AC}, the d-axis reference controller current can be determined. The q-axis controller current (icq) is minimized or increased depending on the need by bringing the bringing the controller direct axis current (icd) to the reference direct axis current value. The Qac of the converter is ideally brought back to zero using the error between the measured value Qac and the reference value $Qac*$ as the input to the PI controller. This bias value between Qac and Qac* is used to generate the controller output bias which is used as the reference value for the direct axis current ($icd*$) of the current to be controlled.

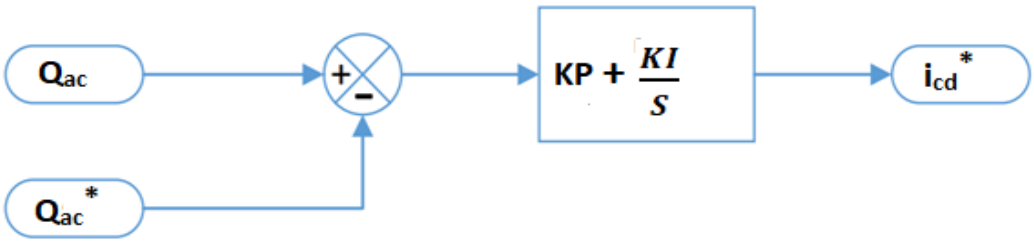


Fig3. 10 Control of reactive power using PI controller

The quadrature axis reference value control current ($icq*$) is produced by bringing the reference active power from the grid ($Pac*$) that is to be synchronized with the inverter's active power Pac, and feeding the error between these parameters to the PI controller as shown below (Deepan Chakravarthy Balakrishnan,2016].

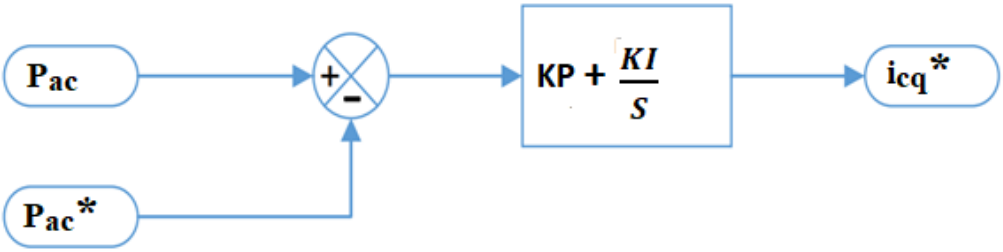


Fig3. 11 PI controller block representation for active power control

During rectification mode, the q-axis control current ($icq*$) is generated by using the output bias of the PI controller after comparing the output DC voltage (V_D) with the required reference output DC voltage ($V_{DC}{}^*$). A quicker and closer control over this constant voltage output is achieved by comparing the square of the reference and actual DC voltages

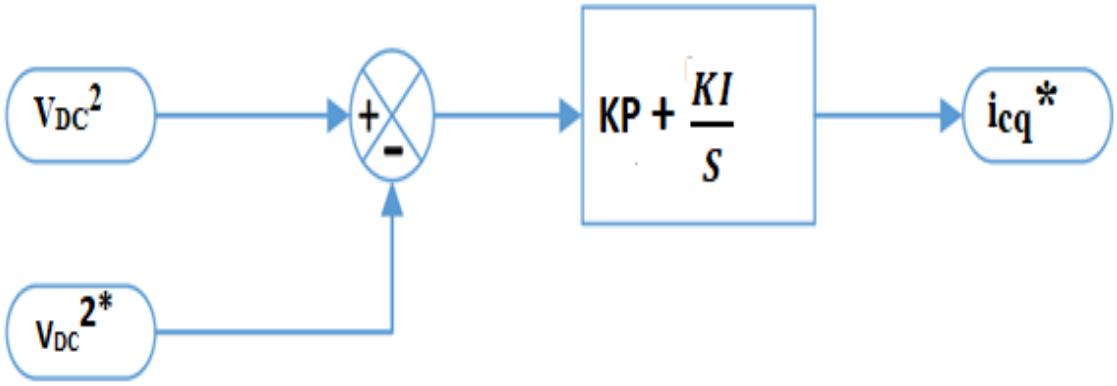


Fig3. 12 DC Voltage control using PI controller

The controller gains of the outer control loop (voltage and power controllers) can be obtained from the converter's DC side equation (3.12) in the section3. 2 and explained in Appendix-A2

3.1.5. Inner Current Control

The goal of inner current control loop is to generate a modulating signal (reference signal) to modulate the converter switches and its control structure is illustrated in Fig3.13. The reference converter current in the form of dq0 scale is obtained from the outer control loop. Comparison of the reference current is made with the AC current output of the converter to be controlled after being transformed to the dq0 scale using Park transform (A. Yazdani, et'al., 2010].

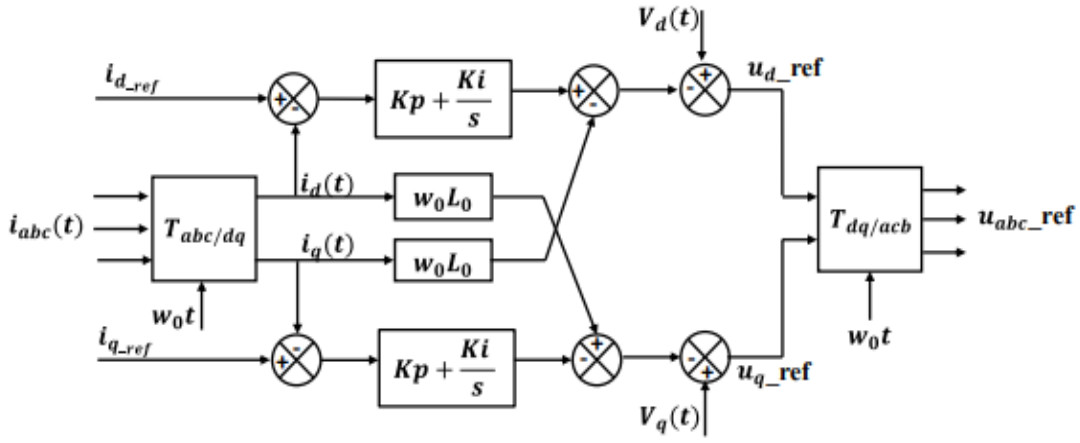


Fig3. 13 Inner current Control loop structure**.**

For derivation of the control equation of the controller current and establish a relationship between the converter current and the voltage of the sub-module, we treat each sub-module to be a voltage source. To further simplify, all sub-modules on each phase arm are bunched up to represent a single voltage generator because series connected voltage sources are summed up according to KVL The charge on the capacitors is controlled by regulating the arm voltage generators so as to impose the required current through the arm inductor. The phase currents on each phase leg need to be equal.

The inner current control loop is described in Fig.3.14 below:

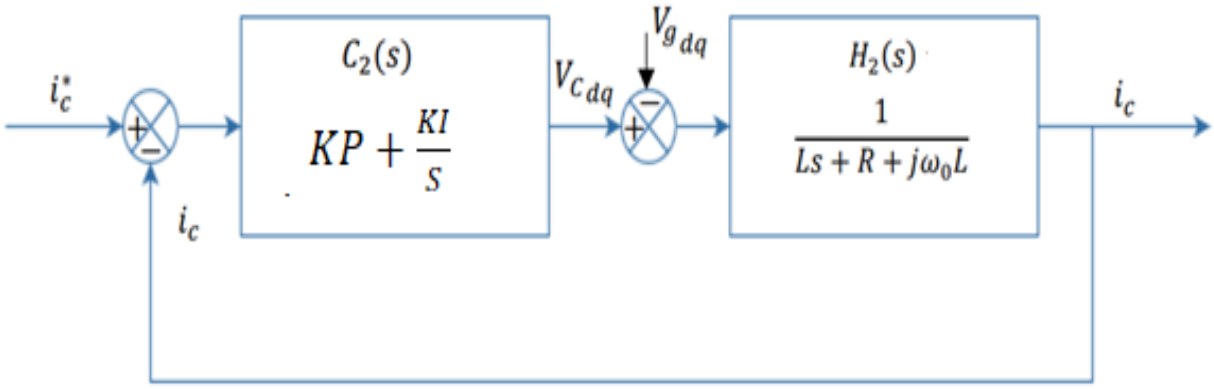


Fig3. 14 Inner current controller transfer function

Using Fig.3.13: and Fig.3.14: controller gains based on desired phase margins at desired crossover frequency can be calculated (explained in Appendix A)

The overall VOC strategy implemented in MATLAB/Simulink is shown in Fig.3.15 below.

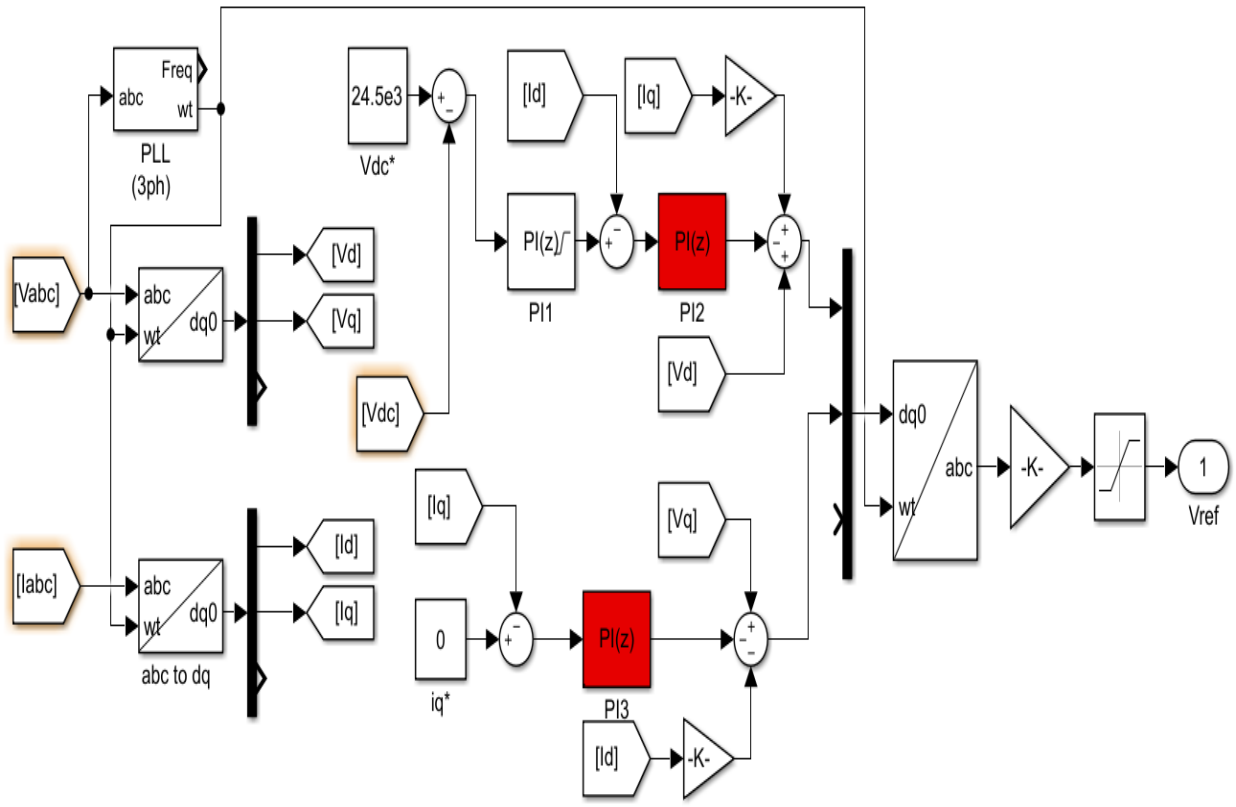


Fig3. 15 MATLAB/SIMULINK model of voltage oriented Control (VOC)

Comparison of a classical controller based on inner loop and outer loop PI controller with fuzzy inference system (FIS) and adaptive neuro-fuzzy inference system (ANFIS) controller is carried out in this dissertation to see their effectiveness.

. The classical PI controller used in the above VOC can be replaced by a fuzzy logic control and ANFIS with two inputs and one output. The error signals (E) and the change in error signal (CE) between the reference DC voltage and the measured DC voltage are the two inputs to the system. When the signal is processed, it generates the desired DC voltage. On the basis of the variable value limit, seven membership functions (MSF) have been developed and labeled as big positive (BP), medium positive (MP), small positive (SP), Zero (ZE), small negative (SN), medium negative (MN), and big negative (BN). Adaptive-neuro fuzzy inference system (ANFIS) is hybrid of artificial neural network (ANN) and fuzzy logic control, which yields a good control response. A one input-one output with seven rules and five layers based ANFIS is used to replace PI in this dissertation. The proposed controller employs the Sugeno fuzzy model with five layers. The first layer (Layer 1) has a function of mapping the input variable relative to every membership function (MF). It is also in charge of effectively conveying the external crisp signal to the other layers.

The second layer (Layer 2) either performs the fuzzification process or receives crisp inputs and determines which inputs belong to the fuzzy set's neuron. The third hidden layer is a fuzzy rule layer that normalizes the previous layer. The fourth layer is used to calculate a normalized firing strength of rules. The last fifth layer performs defuzzification process to produce global output through summation of all inputs that comes to this layer. A hybrid learning rule with 100 iterations and Gaussian membership function are used. The basic ANFIS architecture is given in Fig.3.11 below.

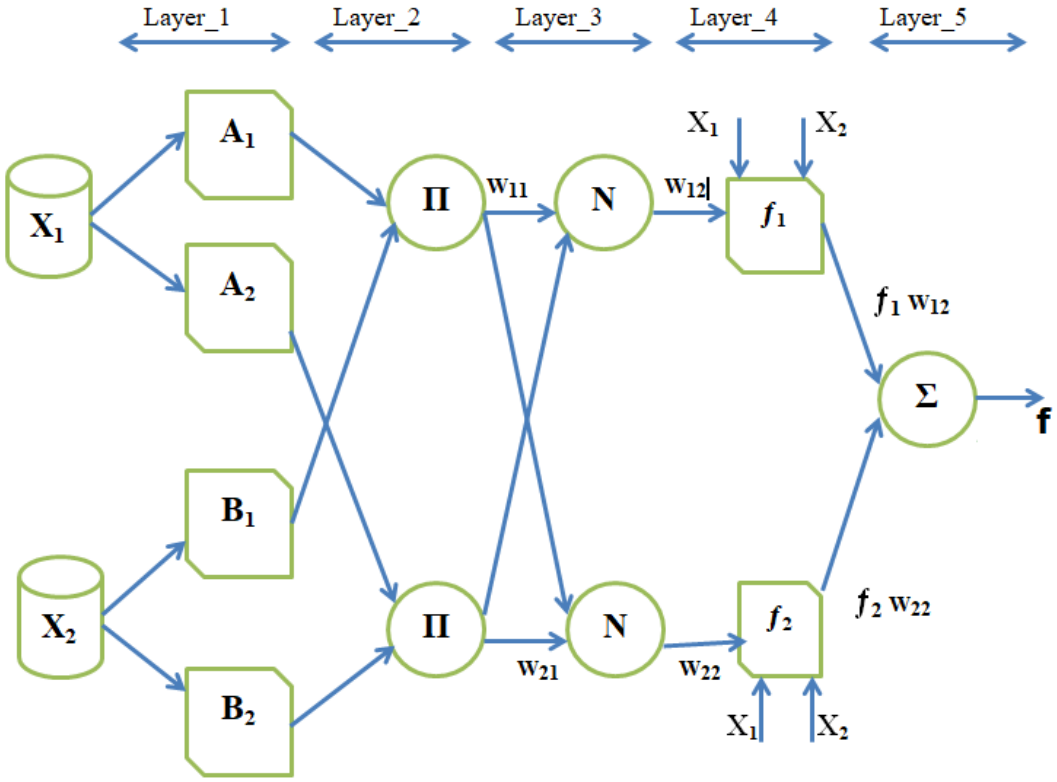


Fig3. 16 Five layer ANFIS architecture

To get the output variable value, the input variables are combined in an AND logical operation. A one-input- one output ANFIS having seven rules is used to substitute PI controller in this dissertation. A Gaussian membership functions are used for input variables and triangular functions are used for output variable. The required data to design fuzzy inference system (FIS) and adaptive neuro-fuzzy inference system (ANFIS) is obtained from PI controller. The error signal between the desired DC link voltage and the actual DC voltage (e) are fuzzified and labeled as shown in Fig.17

		e						
		BN	MN	SM	ZE	SP	MP	BP
Δe	BP	ZE	SP	MP	BP	BP	BP	BP
	MP	SN	ZE	SP	MP	BP	BP	BP
	SP	MN	SN	ZE	SP	MP	BP	BP
	ZE	BN	MN	SN	ZE	SP	MP	BP
	SN	BN	BN	MN	SN	ZE	SP	MP
	MN	BN	BN	BN	MN	SN	ZE	SP
	BN	BN	BN	BN	BN	MN	SP	ZE

Fig3. 17 .Membership function of ANFIS

3.1.6 Simulation and result descustion of FS of ST

A) PI controller with Level Shifted PWM

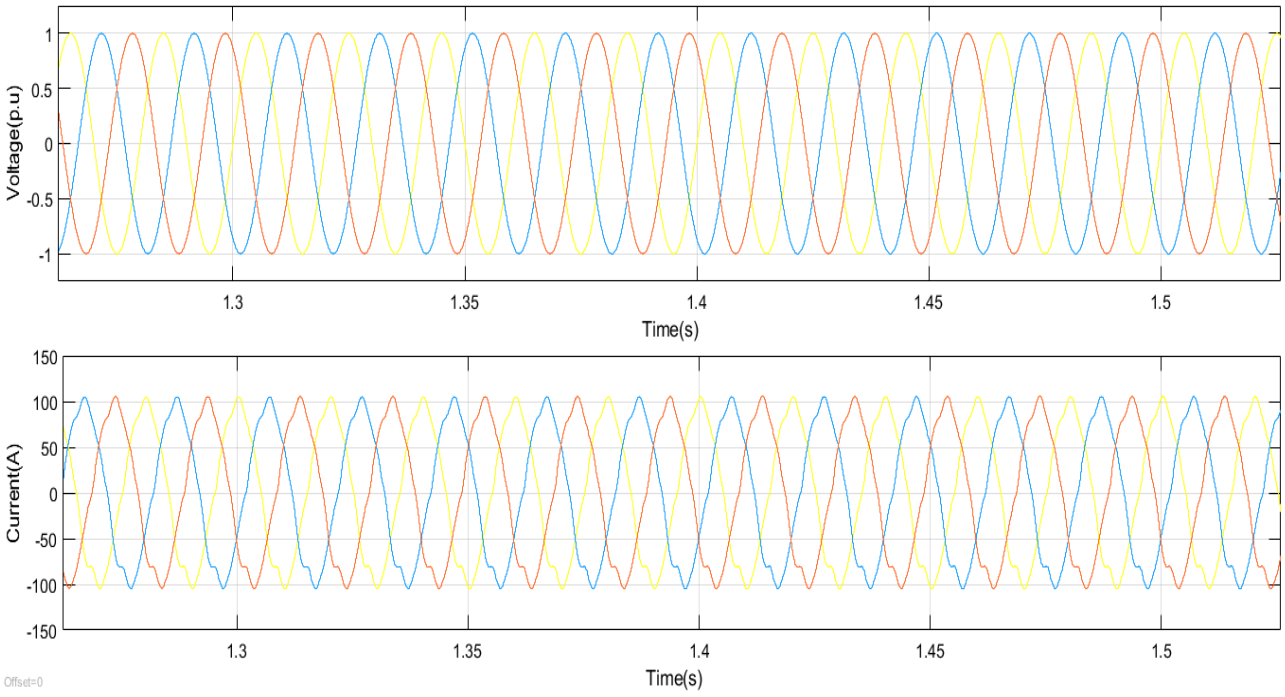


Fig3. 18 Input voltage and current wave forms at grid side for PI with level shifted PWM

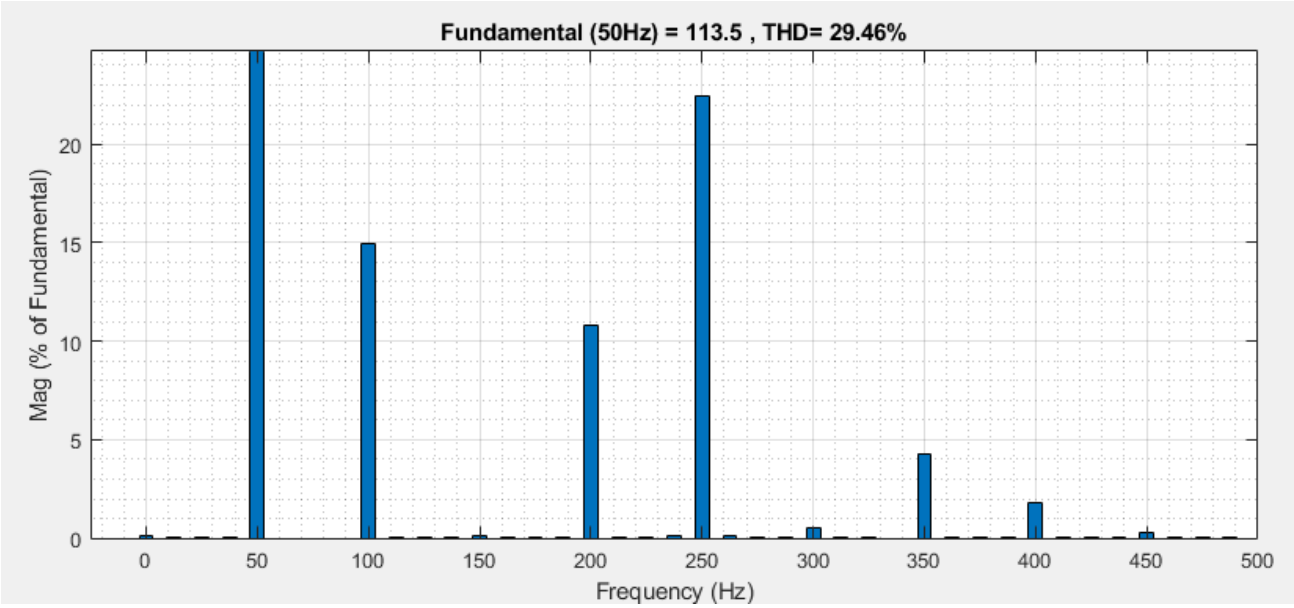


Fig3. 19 Input Current THD for PI with level shifted PWM

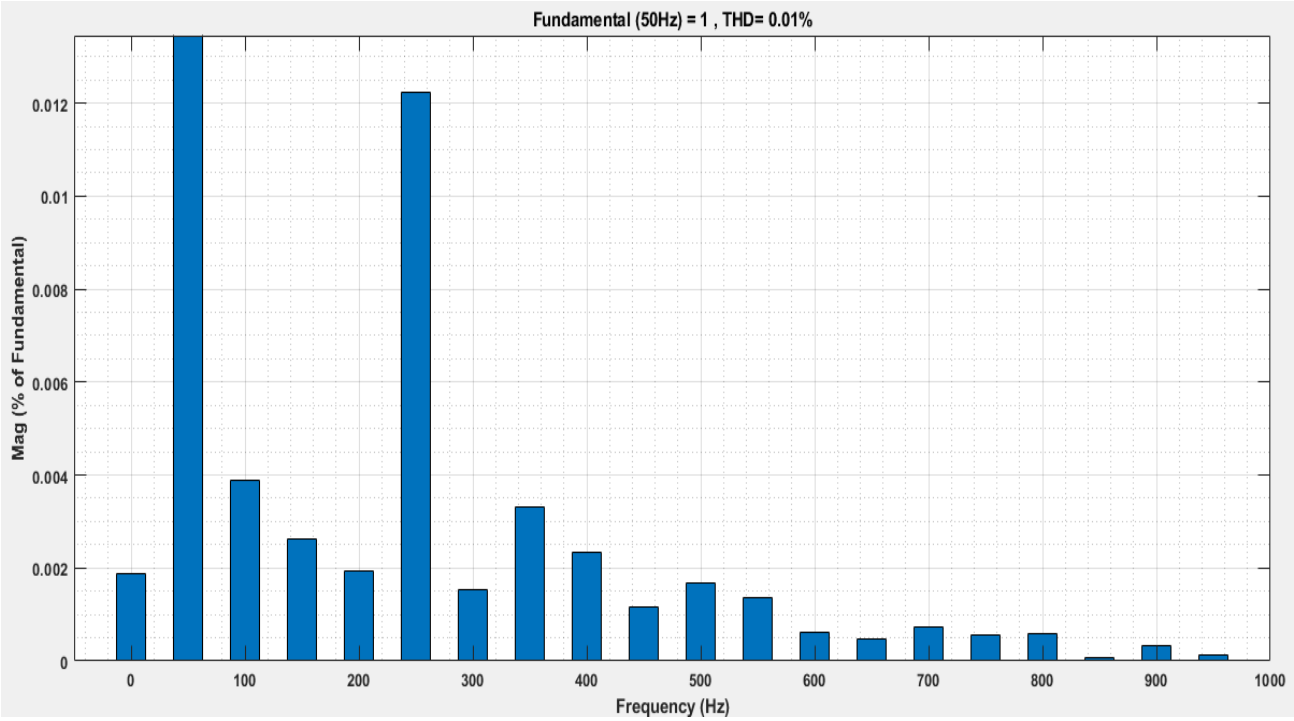


Fig3. 20 Input AC Voltage THD for PI with level shifted PWM

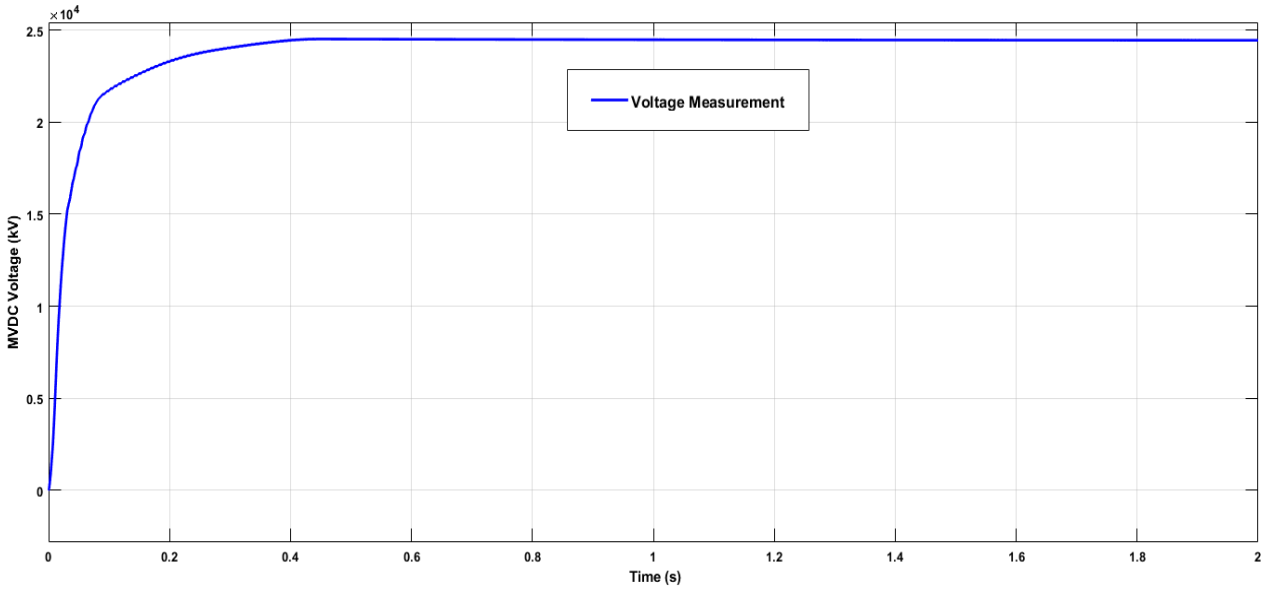


Fig3. 21 MVDC Voltage wave form plot for PI with Level shifted PWM

The grid side current and voltage wave forms are shown in Fig.3.18. The total harmonic distortion (THD) of current and voltage for level shifted modulation technique with PI controller are 29.46 percent and 0.01 percent, respectively, as shown in Fig.3.19 and Fig3.20 in the result section under "A". The RMS voltage is 24170 volts, while the MV DC voltage is 24470 volts. Ripple values can reach a maximum of 1.2%. The DC link voltage rises to its maximum value in less than 0.5 seconds, as shown in Fig.3.21.

B) **PI controller with Phase Shifted PWM**

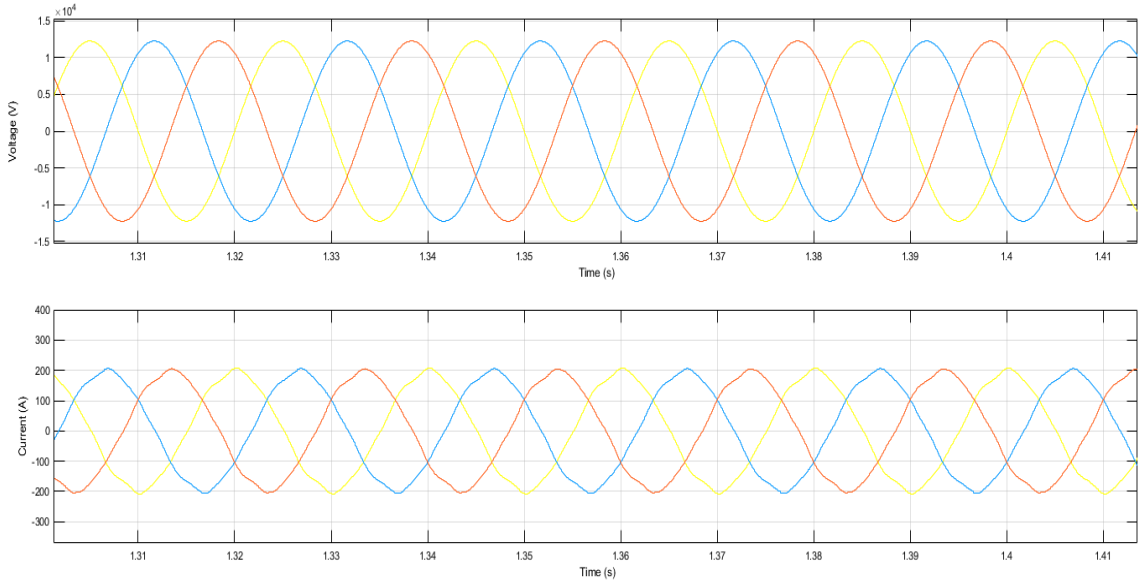


Fig3. 22 Voltage and Current wave form at grid side for PI with Phase shifted PWM

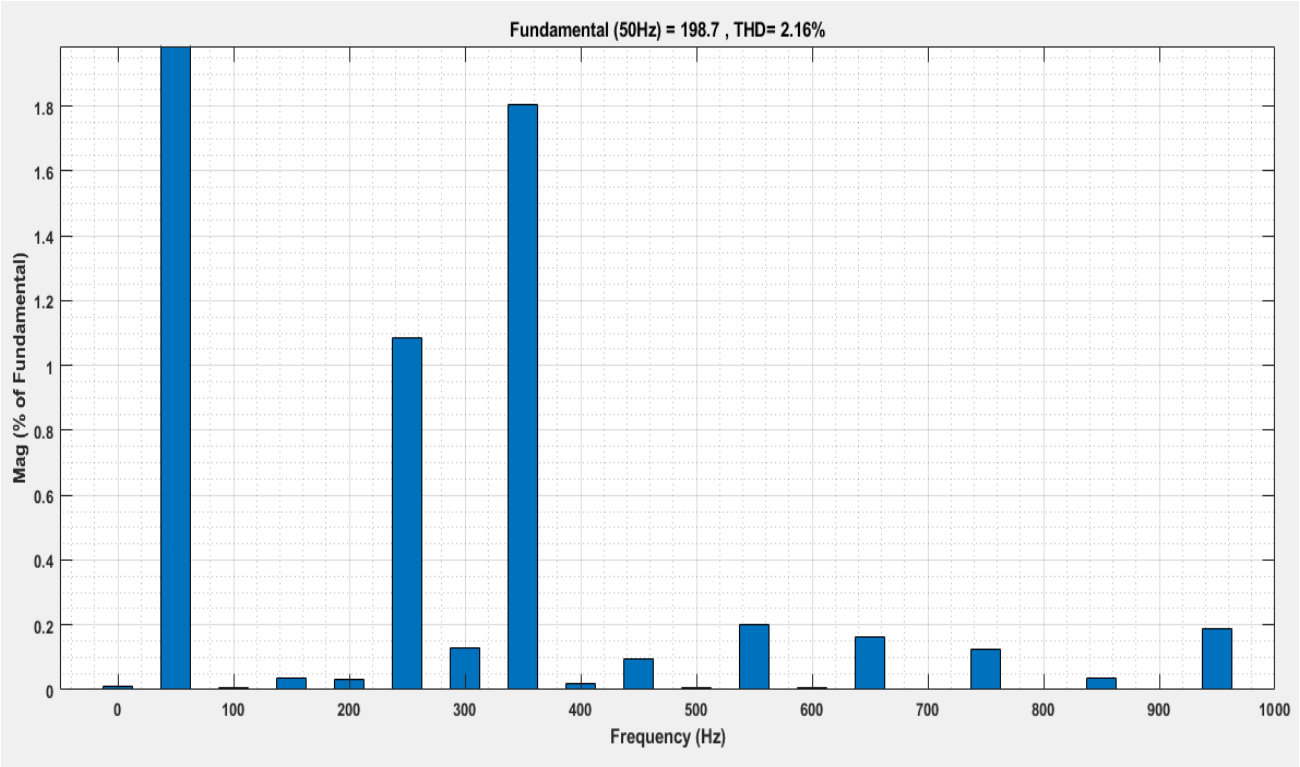


Fig3. 23 Grid side Current THD for PI with phase shifted technique

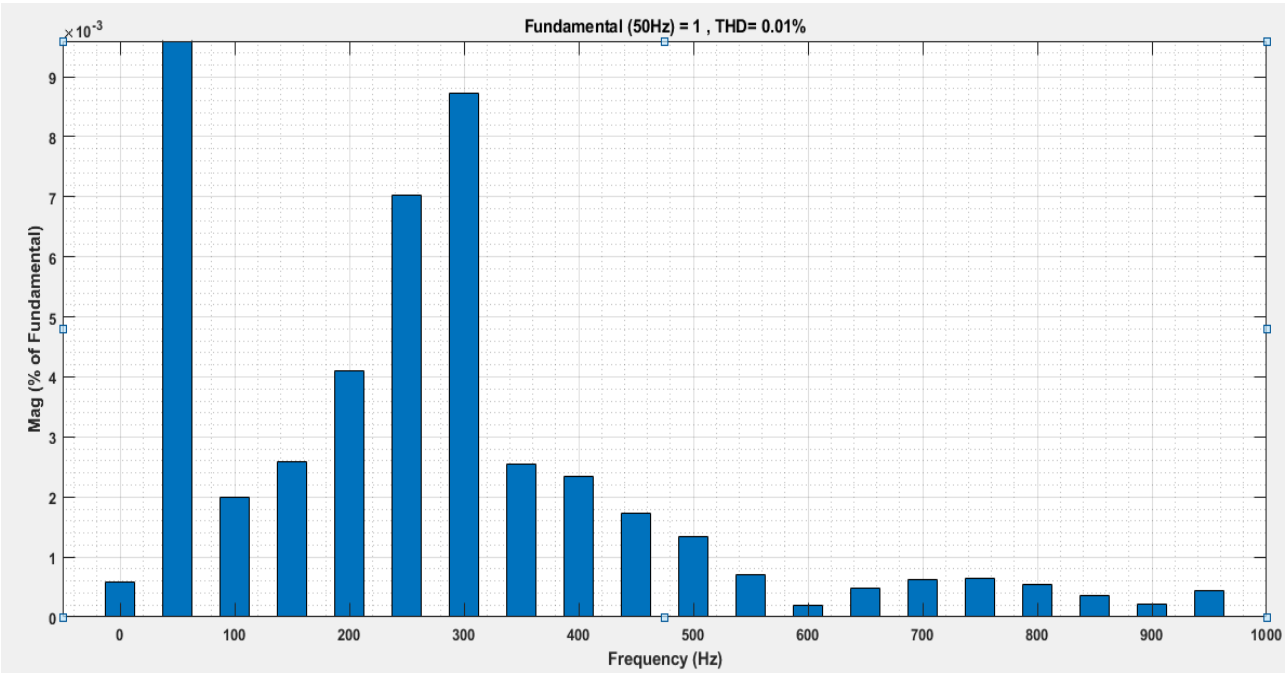


Fig3. 24 Grid side voltage THD for PI with phase shifted PWM

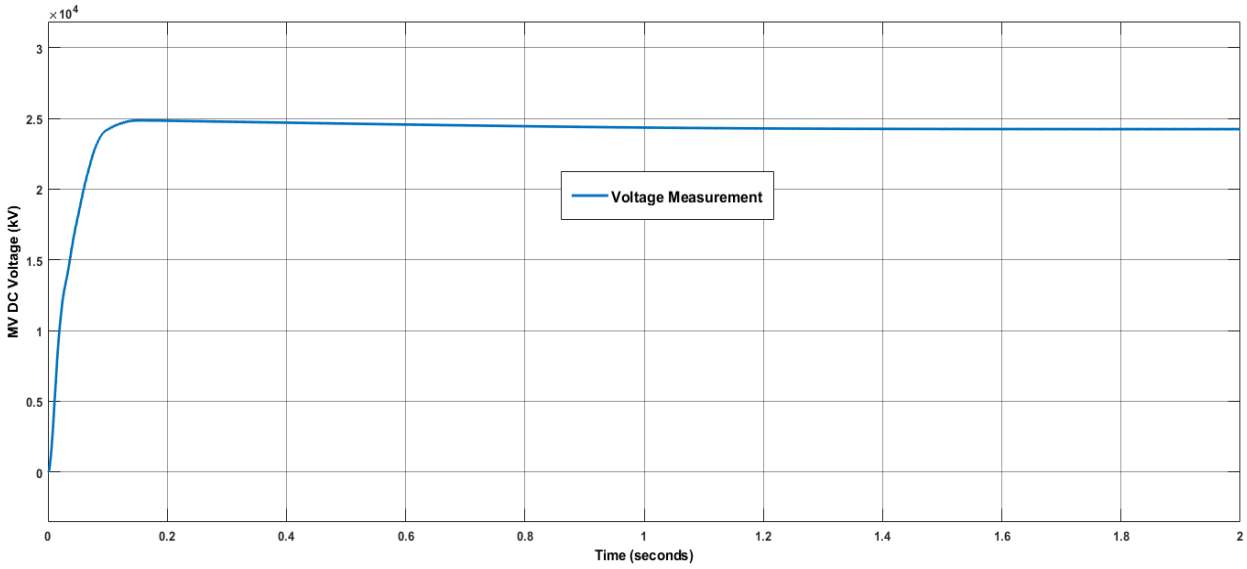


Fig3. 25 FS-MMC output voltage plot for PI with phase shift PWM

The grid side current and voltage wave forms for PI controller with phase shifted PWM is shown in Fig.3.22. Current and Voltage THD for phase shifted modulation with PI controller are 2.16 percent and 0.01 percent, respectively, as shown in Fig.3.23 and 3.24 in the result section under 'B'. It is indicated in Fig. 3.25, that the maximum MV DC voltage obtained is 24530V and its RMS value is 24300V with a ripple of 0.9%. It is also shown that the rise time to reach maximum DC link voltage less than 0.2sec.

C) Result with Fuzzy Logic and ANFIS controller for Level Shifted PWM

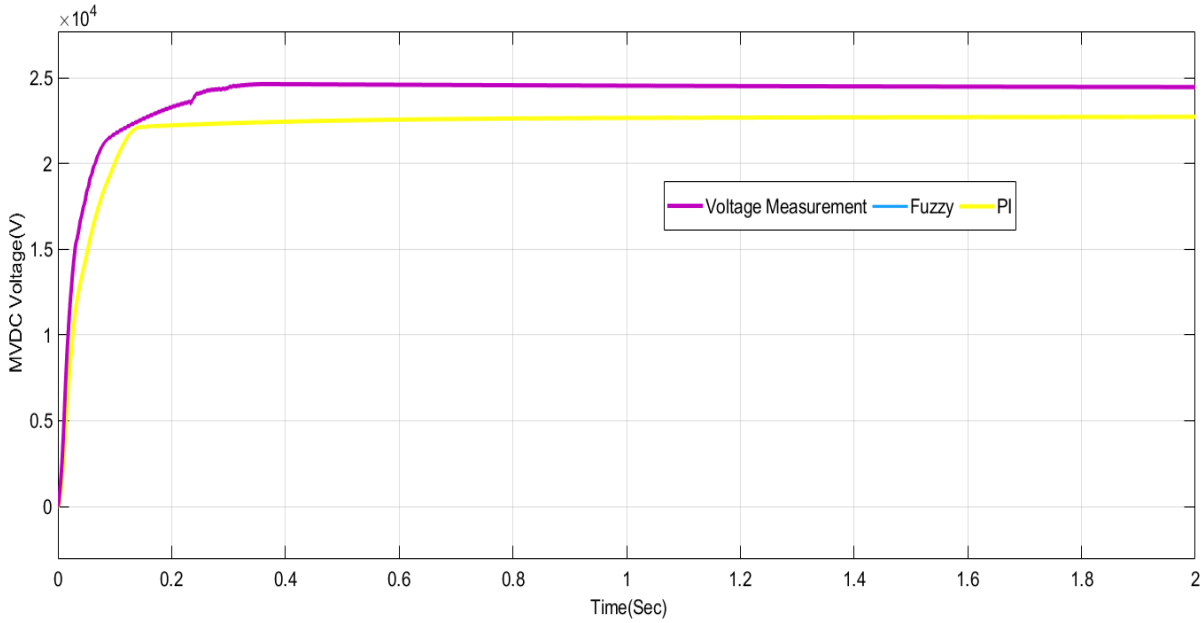


Fig3. 26 FS-MMC output voltage plot for different controllers

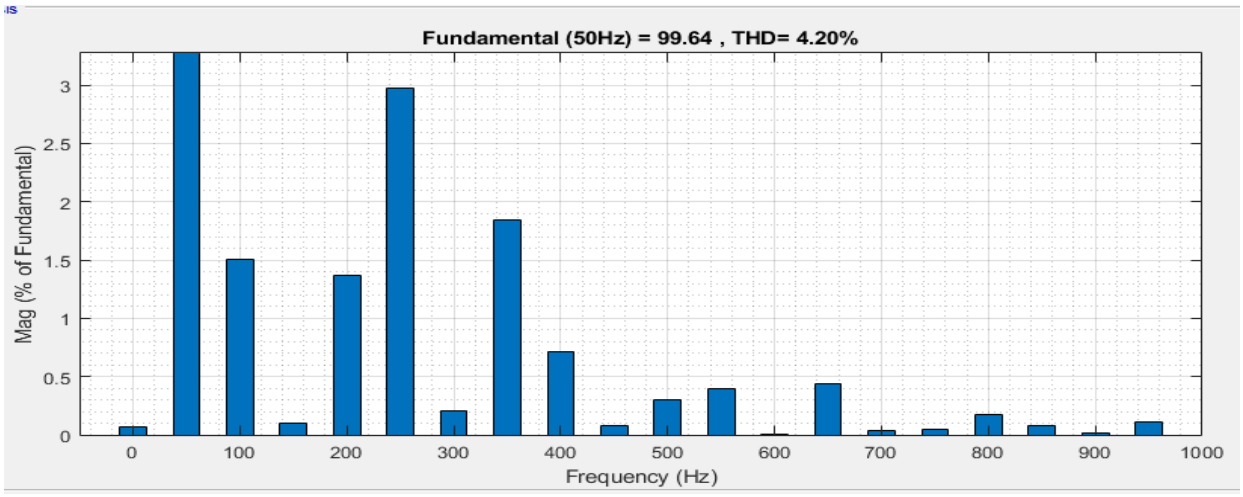


Fig3. 27 Current THD for FIS with Level shift PWM

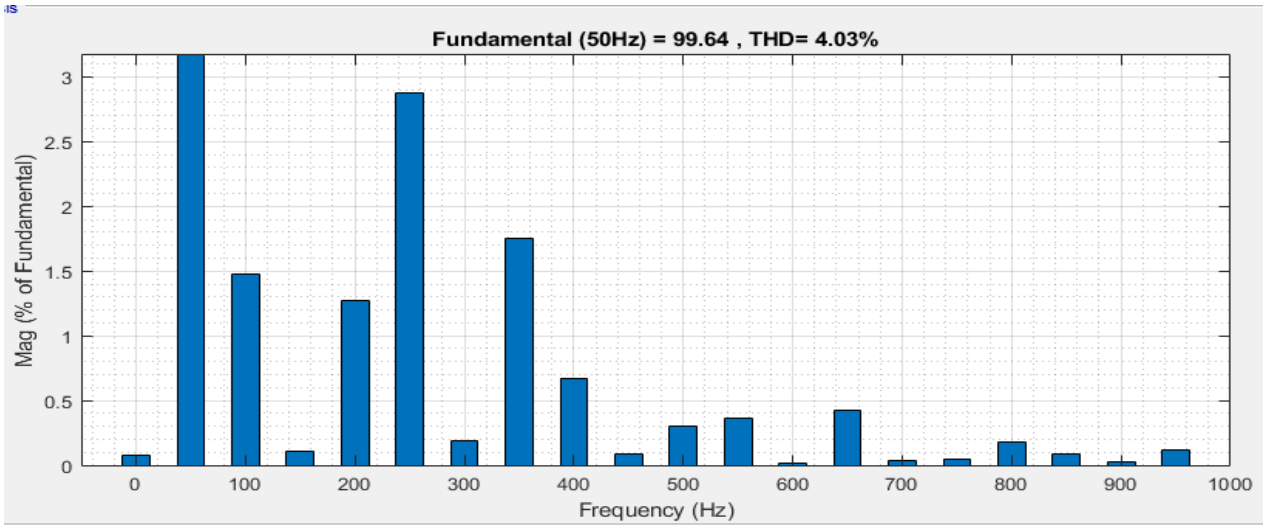


Fig3. 28 Current THD for ANFIS with Level shift PWM

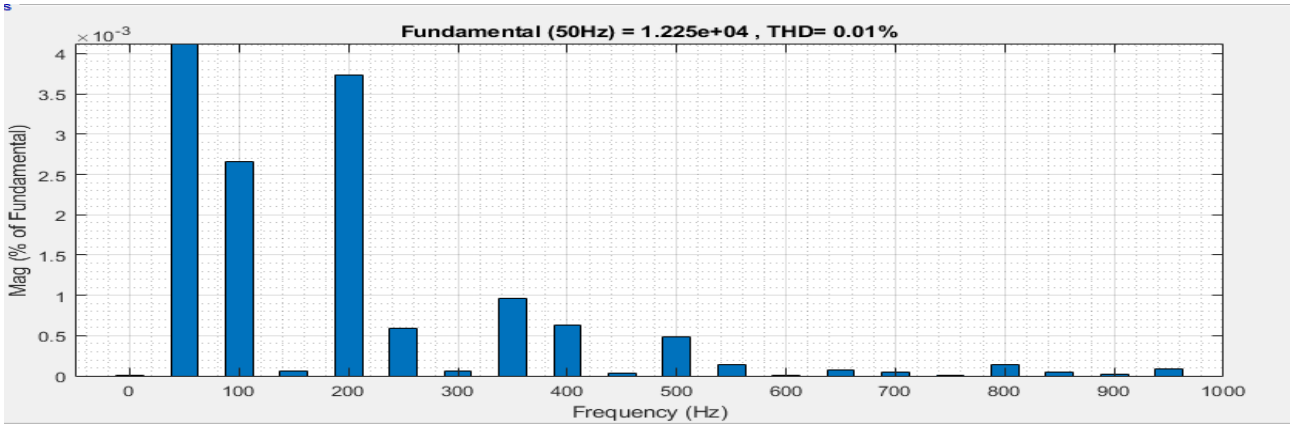


Fig3. 29 Voltage THD for FIS and ANFIS with Level shift PWM

According to observation of simulation results, the level shifted PWM using ANFIS has shown better performance as compared with PI with level shift PWM techniques. The ANFIS current and voltage THD were 4.03% and 0.01% respectively, at the time of this simulation. Analysis of MVDC link voltage, displayed in the Fig.3.26 showed that the rise time is less than 0.3 seconds, and the ripple at level shifted using ANFIS is about 1.3%. Performance of the system with FIS produces a current THD value of 4.20%, nearly equal to ANFIS.

3.2 Design and Modeling of DC//DC Stage of Modular ST

The DC-DC stage is recognized as the heart of the ST architecture as its function is connecting the MV side to the LV side, providing galvanic separation in medium frequency which results in space and volume reduction.

The model implemented in MATLAB/Simulink for representing the DC-DC stage consists of three major parts (see Fig.3.30 to 3.32) irrespective of its topological variants. The first one is a high frequency converter at primary stage. This stage takes the MVDC link voltage of front end converter and converts it in to a high frequency AC voltage fed in to primary winding of medium frequency transformer. The second part is the medium frequency transformer (MFT), which is modeled as ideal transformer with single or multiple primary winding(s), single or multiple secondary winding(s) in series with its short-circuit impedance; and the third part is a single-phase full-bridge PWM converter that acts as a rectifier and provides the required LV dc link voltage to the next stage of the ST.

Independent of the adoption of various approaches i.e. modular or non-modular, this stage has summary of the following requirements as discussed in: (X. She, et'al., 2013; J.E. Huber, et'al., 2016; Levy Ferreira Costa 2019).

i. Capability to handle a high voltage in the MV side: Voltage level in the rage of 10 kV to 25 kV is handled by this stage.
ii. Capability to handle a high current in the LV side: Current value of 100A and above is expected
iii. High voltage isolation: The medium frequency (MF) transformer used in the HV side has an isolation requirement defined by voltage of the MVDC link, i.e. between 10 kV to 15 kV, irrespective of the solution adopted for this stage.
iv. Degree of decoupling between the MV DC side and the LV DC side: Capability to offer total decoupling between the MVAC grid and the LVAC grid, so that the MV

stage and LV stage converters operates in independent manner from each other. This means that the input side converter of ST can operate and provide the required ancillary services to the MV grid (e.g. provide reactive power), without disturbing its output stage or being disturbed by the output stage of ST. The same condition holds true for the LV DC-AC stage operation. This decoupling degree is achieved by maintaining a constant DC links voltage (both MV and LV) with minimal oscillation level (i.e. 5% of the LVDC) and the DC-DC converter should guarantee the voltage regulation.

v. Power flow controllability: A controlled power flows between the LVDC link and MVDC link and effective management of the connection of loads of both sides is possible.

vi. Bi-directionality: As pointed out in many publications, in addition to unidirectional power flow, this stage allows a bi-directional power flow.

vii. DC breaker function: overload and short-circuit protection (working as a DC breaker) during load/source/micro-grid connection to the LVDC link

3.2.1 MATLAB/Simulink Model of DC//DC Stage

The primary converter of DC-DC stage takes 24.5kV MV DC link voltage at the output terminal of front side stage. Many candidate topologies such as standard DAB and MAB in symmetrical and asymmetrical configuration can be used. Also, a three phase DAB can also be used in this stage, giving a reduced LV capacitor size. In this research work, DC-DC stage with QAD in asymmetrical circuit (Fig.3.31), DC-DC stage with symmetrical DAB in ISOP configuration (Fig.3.32) and QAB in symmetrical configuration are proposed to be used in this stage and performance evaluation is made for comparison purposes. The LV DC output voltage of this stage that is fed to the input of back-end converter (BEC) is 750V. Selection of transformer type as three phase or single phase, its shape, core materials, winding type are contributing factors to efficient operation of this stage among other factors. Detail core thermal design, winding design of MFT is not in the scope of this dissertation. This stage operates at high frequency which leads to the reduction of size of passive components and space requirement. However, high voltage isolation sets an upper limit on operating frequency of this stage. Due to this, a maximum switching frequency of 20 kHz is used (Mahammad A., et'al., 2019; Levy Ferreira Costa 2019).

Table3.2 Basic Specification of DC-DC Stage

Parameters	Value
Input (MVDC Link) Voltage	24.5kV
Output (LVDC Link) Voltage	700V
Total power(S)	50kVA
Switching frequency	20kHz

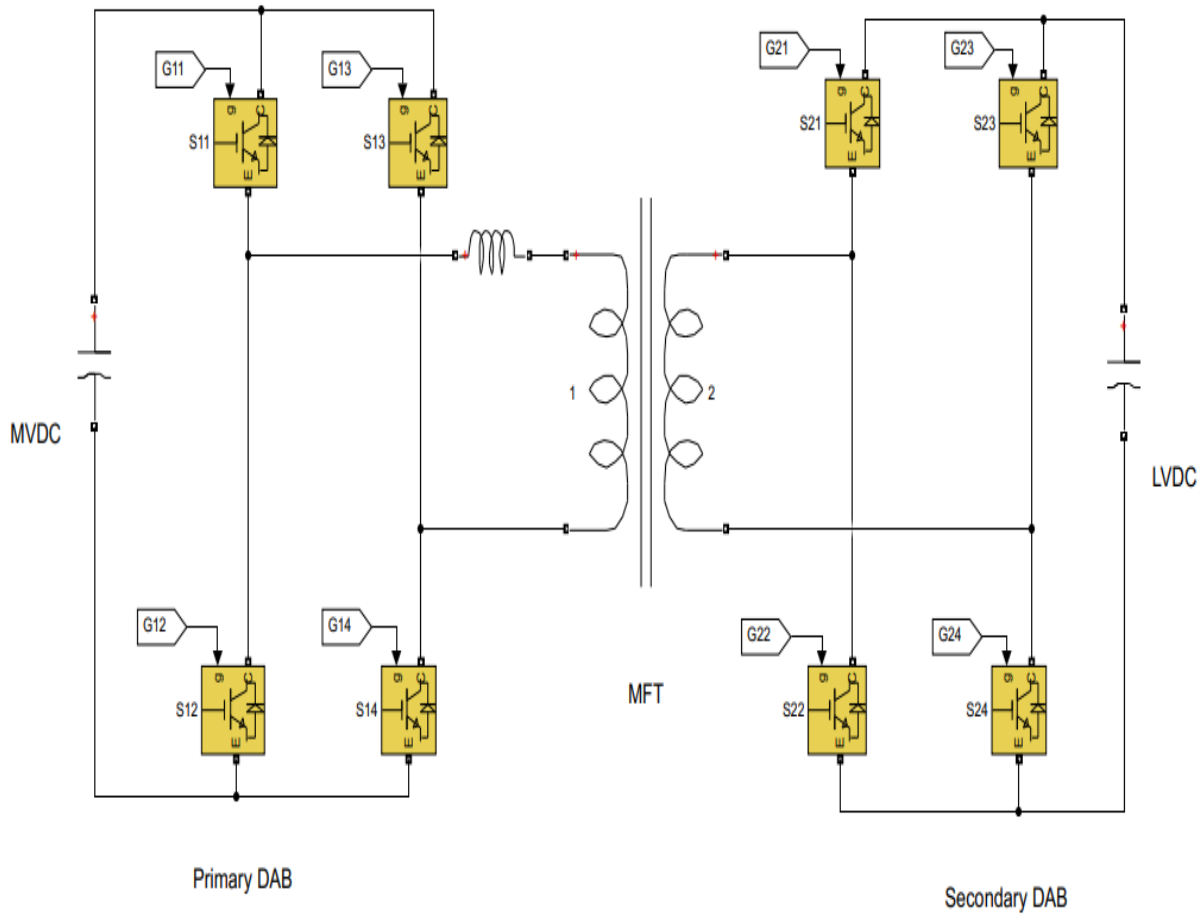


Fig3. 30 DC-DC Stage in standard DAB configuration

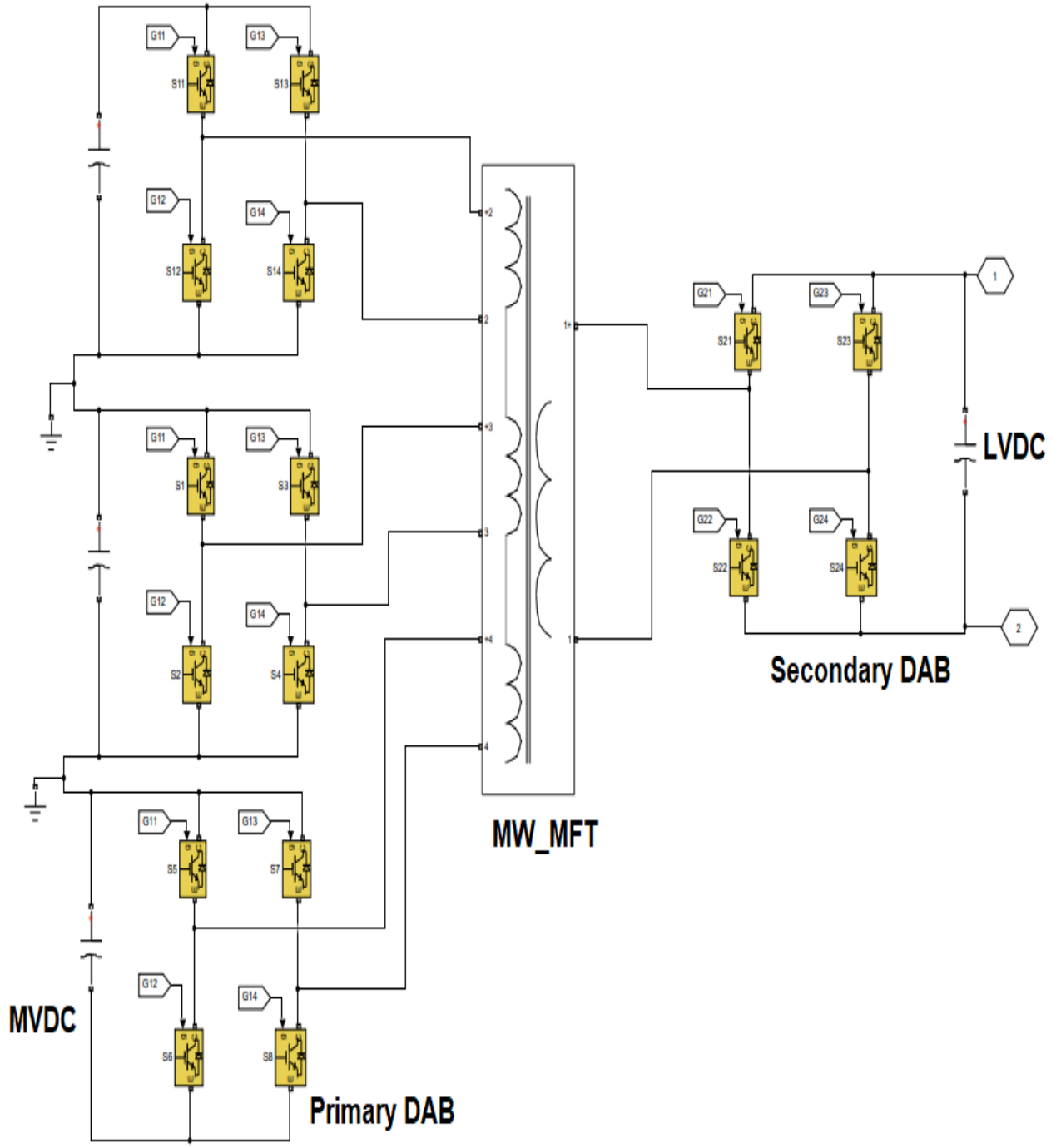


Fig3. 31 DC-DC Stage (QAB in Asymmetrical topology)

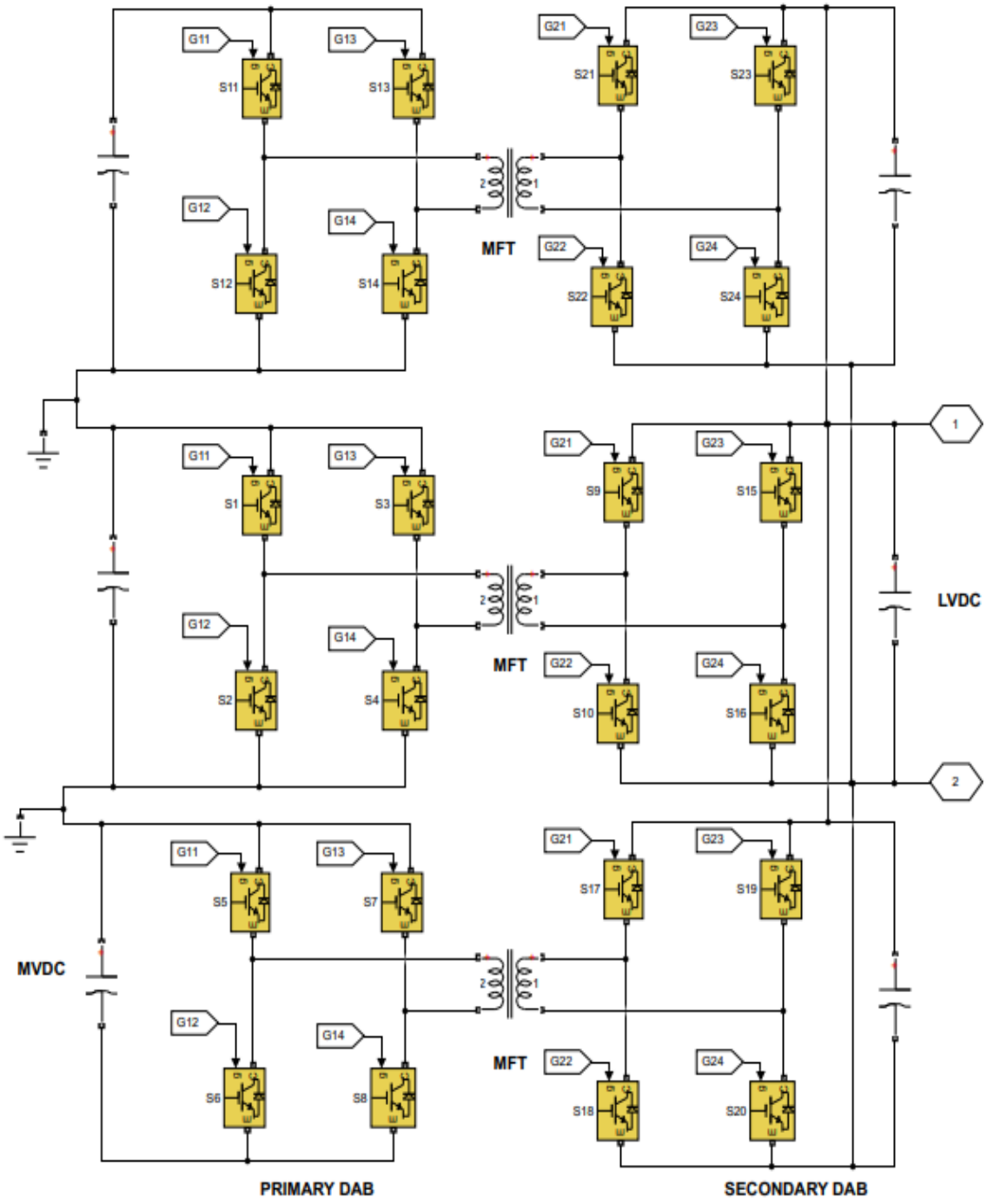


Fig3. 32 DC-DC stage (DAB in ISOP Configuration)

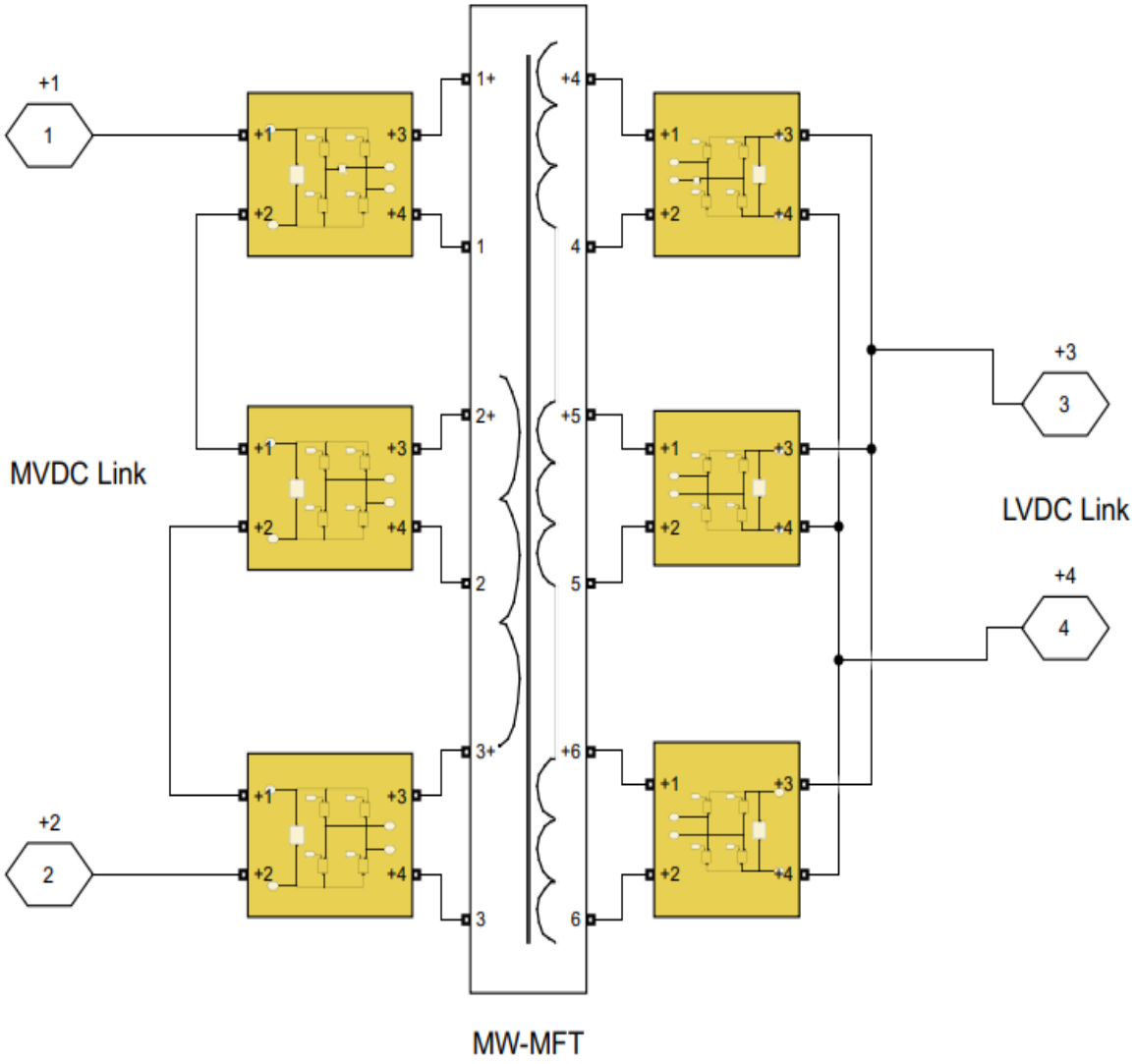


Fig3. 33 DC-DC stage (MAB in symmetrical configuration)

The standard DAB configuration shown in Fig.3.30 couldn't be directly used for the DC-DC stage of the proposed ST configuration as the MVDC voltage is large (24.5kV). The maximum blocking voltage of the switching devices to be used in this stage is limited to 6.5kV to 15kV. Hence, DAB having series connected primary converter is to be applied to share the high voltage and power. This can be achieved by use of QAB in asymmetrical configuration (Fig.3.31), DAB in input-series-output parallel (ISOP) configuration (Fig.3.32) and MAB in Symmetrical configuration (Fig.3.33). The QAB in asymmetrical configuration uses a common MVDC voltage and multi-winding medium frequency (MW-MFT) transformer to isolate the input side and output side converters.

Due to the fewer number of components (Cells and MFT), the QAB solution is more

economically advantageous, as presented in Fig.3.31. Adopting this solution instead of others considering the specification of the Table I, the system cost can be greatly reduced when Si-IGBT are employed. Regarding the efficiency, the QAB solution presented similar performance to the DAB, although the first one performs slightly better. As the QAB operates similarly to the DAB converter, when processing balanced power, then similar power dissipation is also expected. Of course, semiconductor with different electric characteristic are used in the LV cells for both cases, and also the quantity of semiconductors, resulting in different power dissipation between the solutions. Then, QAB converter is proposed as it is an economically viable solution in DC-DC isolation stage. The potential application of this configuration in ST has been demonstrated from the results obtained in (Levy Ferreira Costa, et'al.,2018). The multiple active bridges (MAB) in symmetrical configuration depicted in Fig.3.33 is also a candidate solution in the DC-DC isolation. This configuration allows use of low voltage semiconductor switches in MV stage and power sharing at the LV stage, giving a chance to use low value current rated semiconductor switches.

3.2.2 Selection of Si and SiC based IGBTS and MOSFETs

The switching devices themselves are a key component of the DC-DC stage. Selection of the power switching devices is less simple, in that it requires no mathematical analysis to select, but rather best judgment must be applied. Factors to be assessed to select switching device include on resistance, peak voltage and current ratings, and the stresses they must withstand, switching frequency and commutation loss. Basically, the converter terminal connected to the low voltage conducts higher peak currents and will therefore exhibit higher conduction losses through each device. Considering the voltage and power level of the converter, Silicon IGBT modules are often used in this stage. On the other hand, the new technology of Silicon-Carbide MOSFETs has emerged as a high performance and efficient solution. The SiC MOSFETs offer many advantages such as high frequency operation, reduced commutation loss and higher voltage blocking capacity as compared with Si based IGBT of the same rating. These devices have been used to implement the power converters of the ST architecture in (K. Mainali, et'al., 2015). In general, use of SiC MOSFET reduces commutation power dissipation by 25 times smaller and size reduction up to 50% when it replaces Si based IGBT (R. M. Burkart,et'al.,2016; Jeff Casady,2018). However, the energy saving throughout the system operation needs to be evaluated properly according to the application, to justify for its feasibility

Summary of benefits obtained at device level and converter level when using SiC MOSFET is illustrated by Fig.3.34

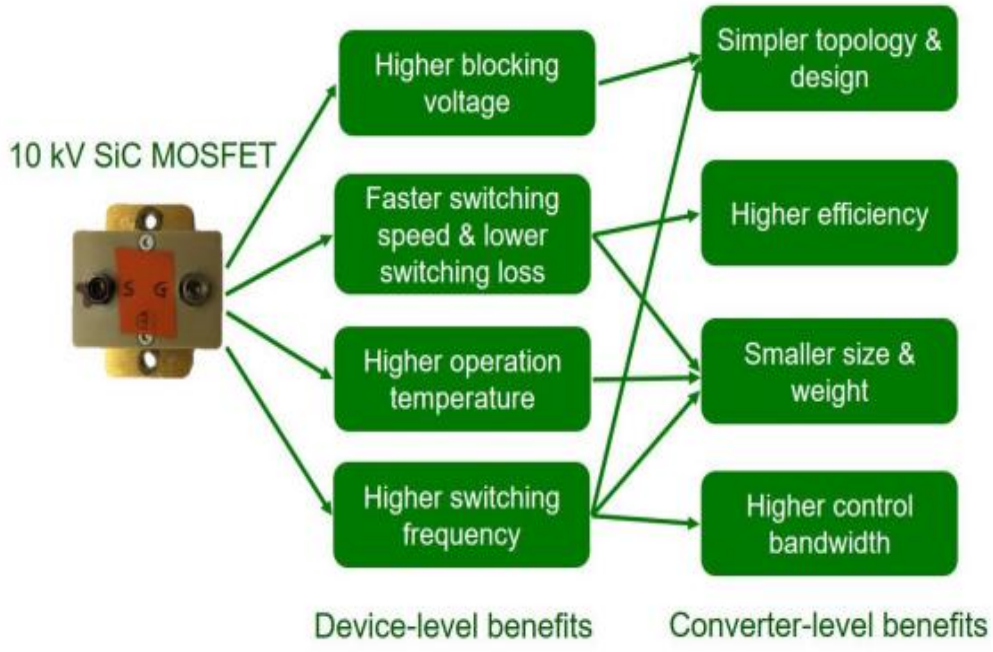


Fig3. 34 Benefits of SiC MOSFET [142]-[146] (J. Wang, et'al., 2008; E. Van Brunt, et'al., 2015)

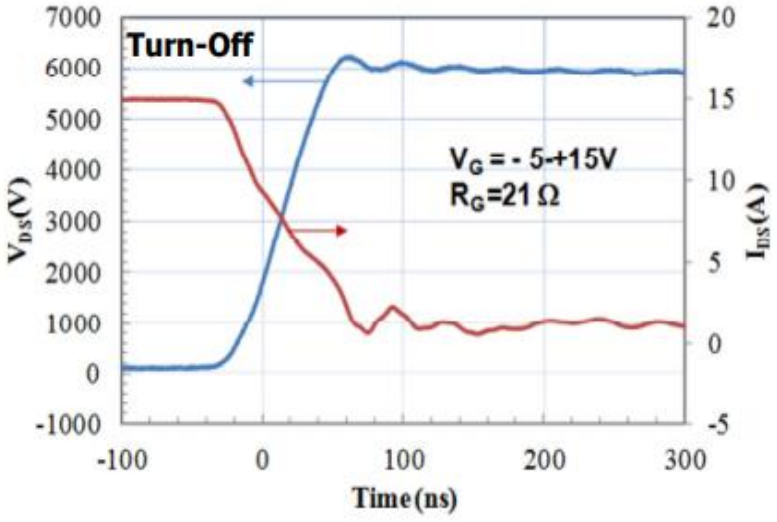


Fig3. 35 Turn-Off SiC MOSFET characteristics curve (10kV)

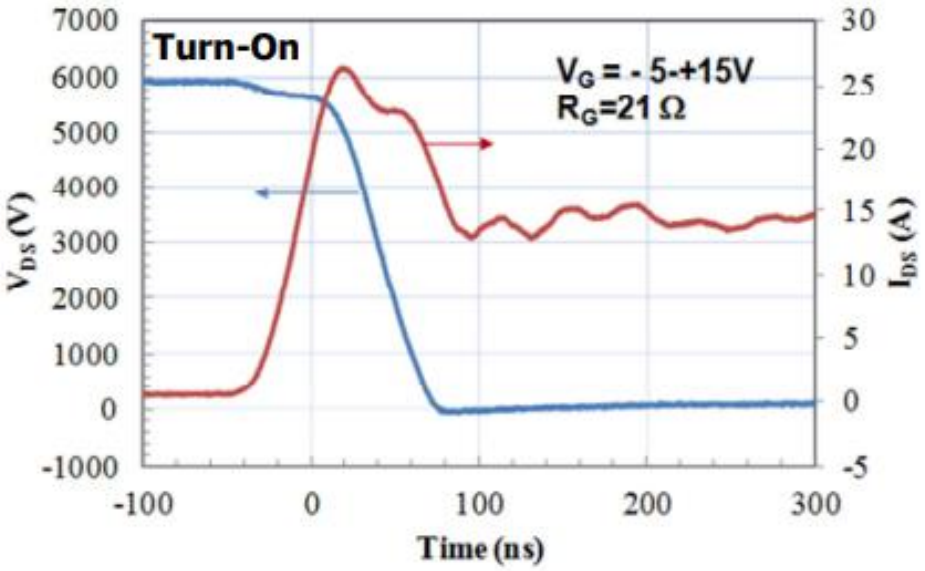


Fig3. 36 Turn-On MOSFET characteristics curve (10kV)

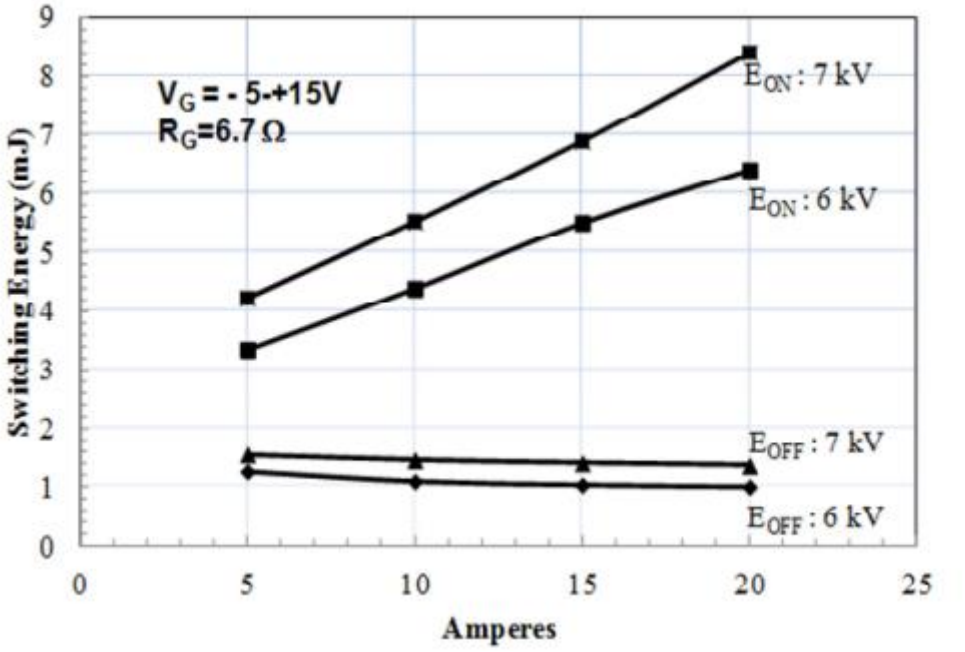


Fig3. 37 MOSFET commutation energy characteristics curve

3.2.3. Modulation Technique for DC-DC stage.

A number of modulation schemes for the dual active bridge have been studied. They include phase shift modulation, trapezoidal modulation and triangular modulation. From the aforementioned modulation methods, the most commonly used one is the phase shift modulation (PSM) method, which directs power flow by shifting the leading edges of each

complimentary pair of devices, both high- and low-side switches (Kheraluwala, et'al., 1992; Kheraluwala , et'al.,2000). The simplest type to implement is Single Phase shift Modulation (SPSM which follows exactly the power flow. Other methods, such as dual phase shift modulation, hybrid phase shift modulation, and triple phase shift modulation have been studied and compared. These variations on the PSM method offer many benefits, but their controller design and implementation are much more sophisticated. This project work will utilize the SPSM method, for both primary side bridge and secondary side bridge,

3.2.5. Primary and Secondary Side Converter parameter for proposed topologies

As shown in basic specification Table of DC-DC stage, the input to the PWM inverter or primary DAB is the medium DC link voltage of 24.5kV. For quadruple active bridge (QAB) asymmetric configuration shown in Fig. 3.31, the DC link voltage is shared equally in three primary DAB circuits. The peak rectangular AC voltage to each primary DAB should be slightly lower than the DC input so as to avoid over modulation. Therefore, a value of 24.5kV/3 = 8.2kV is chosen as peak AC rectangular voltage to each primary converters. The RMS value of primary DAB is calculated as:

$$\mathbf{V_{RMS(P)}} = \frac{\mathbf{8.2kV}}{\sqrt{\mathbf{2}}} = \mathbf{5.8kV} \approx \mathbf{6kV} \qquad (\mathbf{3.19})$$

This value can also be used for other two configurations i.e DAB symmetrical ISOP and MAB symmetrical configurations**.**

Assuming that the total power(S) is shared equally among the three primary DABs, the RMS primary currents for the three proposed configurations can be obtained as:

$$\mathbf{I_{RMS(P)}} = \frac{\mathbf{S/3}}{\mathbf{V_{RMS(P)}}} = \mathbf{2.77A} \approx \mathbf{3A} \qquad (\mathbf{3.20})$$

The LVDC requirement as given in basic specification Table3.2 is 700V. The MFT output (Secondary side) AC peak voltage should be slightly less than the output LVDC voltage. If we select a value of 700V, the MFT secondary RMS voltage is $700V/\sqrt{2}$ = 495 ≈500V.

For AQAB topology, the magnitude of secondary RMS current can be obtained as

$$\mathbf{I_{RMS(S)}} = \frac{\mathbf{S}}{\mathbf{V_{RMS(P)}}} = \frac{\mathbf{50KVA}}{\mathbf{500V}} = \mathbf{100A} \qquad (\mathbf{3.21})$$

The MFT turn's ratio is given by $\frac{V_P}{V_S}$ = 12:1

For MAB in symmetric configuration and DAB_ISOP configurations, the value of secondary side current is smaller than it is for QAB in asymmetric configuration as a result of power sharing among the three secondary side converters

$$\mathbf{I_{RMS(S)} = \frac{S/3}{V_{RMS(P)}} = 34A} \qquad (\mathbf{3.22})$$

Based on the above analysis, the semiconductor switch ratings of primary side and secondary side converters with sufficient consideration of safety factor are summarized in Table.3.3 below

Table3.3 Switching device parameter for DC-DC stage

Primary side Voltage = 10kV					
Device PN and Company	I(A)	Ron (mΩ)	Eon/E-off (mJ)	VG(V)	Configuration
CPM3-10000-0270 (CREE)	20	300	6/1	-	DAB_ISOP, SMAB, AQAB
Secondary side Voltage = 900V					
Device PN and Company	I(A)	Ron (mΩ)	Eon/Eoff (mJ)	Vf (V)	Configuration
SD11740 (Solitron)	100	8.6	3.5/0.7		AQAB
C3M0030090K (CREE)	73	30	0.15/0.09	2.5	DAB_ISOP, SMAB

3.2.6. Design of Medium frequency Transformer

The optimal design of a high-power medium-frequency(<1MHz) transformer include rigorous evaluation of factors such as selection of the smallest standard core shape relevant to the output power, frequency, and transformer operating temperature, calculation of the optimum flux density providing minimum transformer loss and calculation of the optimum wire diameters of the windings and leakage inductance (Petkov R ,et'al.,1992).The following design equations are given from which the area of the core, window spacing, primary and secondary turns are determine (M. A. Shamshuddin,et'al.,2020).

The core area is given from the area product A_P which is the product of window area and core area found in manufacturer's datasheet.

By using the total kVA capacity of the MFT, area product (A_P) can be expressed as follows:

$$A_P = \left[\frac{\sqrt{2}\sum VA}{B_O f_s K_V K_t K_f \sqrt{K_U \Delta T}}\right]^{\frac{8}{7}} \quad (3.23)$$

Where,

B_O is optimum flux density, f_S is switching frequency, K_V is wave form factor, K_f is stacking factor that correlates the effective cross-sectional area of the core with its actual area, K_U is window utilization factor and ΔT is change in temperature. The factor Kt is found from (M. A. Shamshuddin, et'al., 2020).

$$K_t = \sqrt{\frac{K_a h_C}{\rho_w K_w}} \quad (3.24)$$

Typical values of K_V can be 4 or 4.44 depending on wave shape, K_f is 0.9 to 0.95, ka = 40, kc = 5.6, and kw = 10 , K_U = 0.4 and are set as fixed parameters during design process (W.G. Hurley,et'al.,1998; M. A. Shamshuddin, et'al., 2020).

The optimum flux density is then found by using the equation given in section (2.4.1) in equation (2.15)

Alternatively, the total KVA rating of a transformer can also be given using the following equation:

$$KVA = 2.22 f_s K_W B_M J A_C A_W * 10^{-3} \quad (3.25)$$

Where, A_C is core area, A_W is window area, B_M is saturation magnetic flux density, J is current density and K_W is a factor obtained as given below (Kheraluwala , et'al.,2000).

$$K_W = 10/(30 + kV\ of\ HV\ winding) \quad (3.26):$$

Substitution of the value of HV winding in (3.20) gives the value of K_W to be 0.28

The maximum core area is obtained as follows:

$$A_C = \Phi_m/B_M = (E_T/4.44f)/\ B_M \quad (3.27):$$

Where E_T is voltage per turn of winding and obtained as follows (W.G. Hurley, et'al.,1998)

$$E_T = K_V K_f A_C \Delta B f_s \quad (3.28):$$

If the voltage per one turn of a winding is assumed to be 10V and other parameters as presented in Table3.4, then the cross sectional area of the core is 4.6cm^2

From the selected core area and voltage per turn, the number of turns in the primary winding is

$$N_P = V_P / E_T \quad (3.29)$$

Substitution of the value of primary side voltage obtained in section (3.5) gives the number of turns in the primary side of MFT for all configurations (QAB-ISOP, AQAB and SMAB) is 600

The number of turns in the secondary side of MFT is obtained by using basic transformer equation:

$$N_S = N_P / V_P * V_S \quad (3.30)$$

The value of secondary number of turns obtained is 50

From the calculated values of primary and secondary currents and selected current density, areas of primary and secondary windings are obtained.

$$A_{wng} = I_{rms} / J \quad (3.31)$$

For all stated three configurations, the primary side currents for normal operations are same and hence the winding area obtained is 0.5mm^2

The value of secondary side winding area differs for different topologies. For DAB-ISOP and SMAB topologies, the secondary winding areas are same and equal to 5.6mm^2. However, for ADAB, the secondary winding area is larger than it is for the others and equals to 16.7mm^2

Table3.4 MFT design Parameters

Parameters	Value
Total power(S) Switching frequency V_P(RMS) V_S(RMS) Current density(J) Voltage per turn (E_T)	50kVA 20kHz 6kV 500V 6A/mm^2 10V
Maximum Flux density(B_M)	1.5T
Window utilization factor (K_U)	0.4
Stacking factor (K_f)	0.9
Voltage form factor (K_V)	4
Flux density variation (ΔB)	0.3
Mean turn length of winding(L_{ET})	100mm
Density of Copper (d_{wng})	8.96 · 10−3 g/mm3
Change in temperature (ΔT)	50^{0}C

Values of selected winding (copper) area and core area can be multiplied with their effective winding length and core length to find the total volume requirement of MFT for cost comparison of the three topologies if needed. If we assume a constant volume of core for three topologies, then volume of MFT depends on the volume of winding (copper) used.

The volume of winding used in the MFT is obtained as follows:

$$V_{wng} = A_{wng}\,(NL_{ET}) \qquad (3.32)$$

Where L_{ET} is effective length of one turn

The weight of winding, which is related to cost of copper used is obtained by multiplying the winding volume by its density

$$W_{wng} = A_{wng}\,(NL_{ET}) * d_{wng} \qquad (3.33)$$

where, d_{wng} is density of winding (copper) used

In general, computer aided iterative design procedures shown in Fig.3.35 can be followed to arrive at the feasible MFT for a given application.

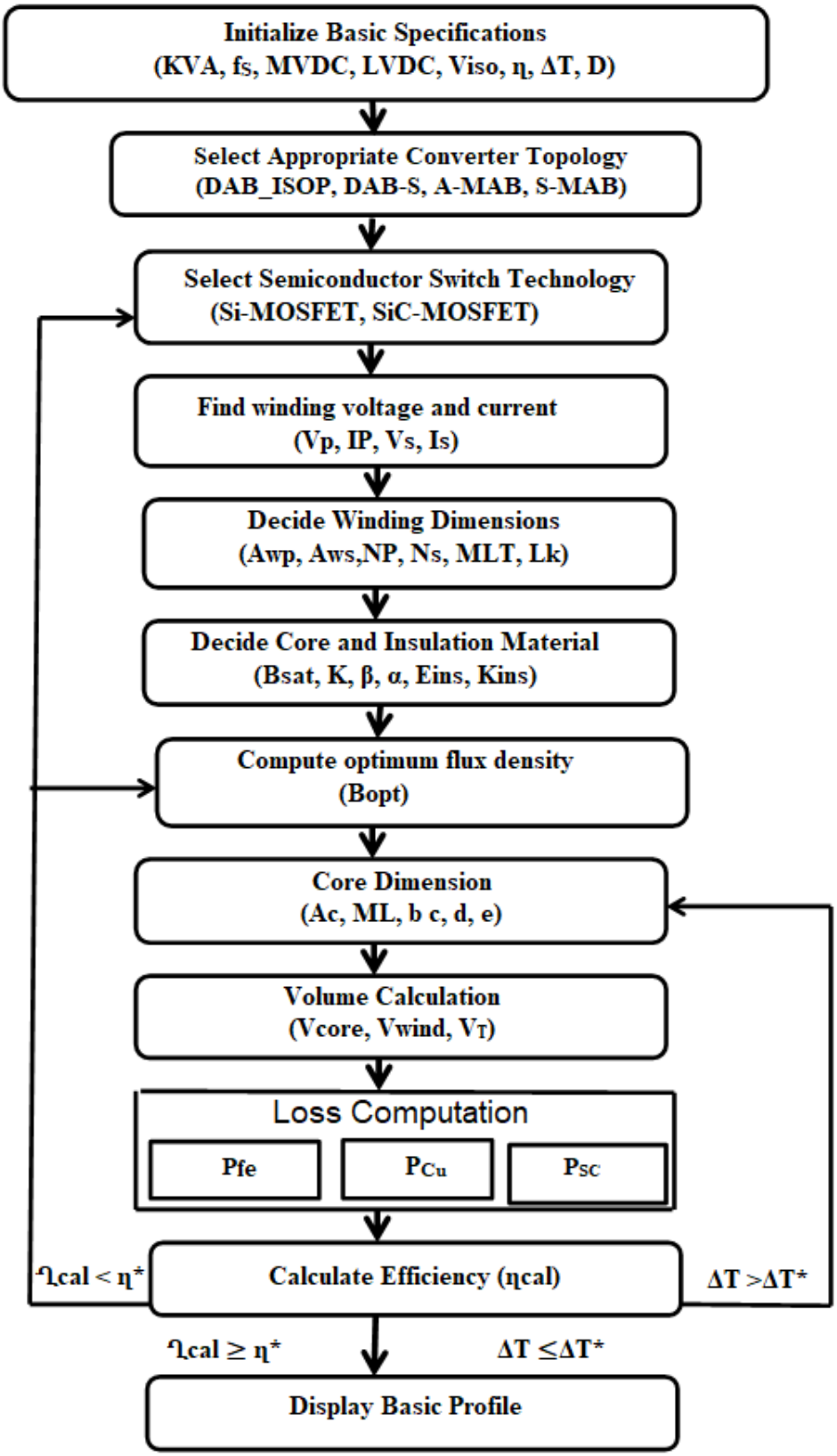


Fig3. 38 General design flow chart of DC-DC stage.

The volume of core used in the MFT is obtained as product of mean length of the core and its cross-sectional area follows:

$$V_{Core} = A_{Core} * L_M \quad (3.34)$$

The basic insulation level requirement determines the minimum separation distance between primary and secondary windings. If the isolation voltage of 95kV between primary and secondary side winding is assumed and epoxy insulation material having dielectric strength of 15kV/mm with safety factor of 40% is used, then the minimum isolation distance obtained as per equation(2.26) under section 2.4.4 is equal to 19mm

The core and winding volume obtained are multiplied with their respective densities to get the weight for finding the cost of winding and core materials. Cost of winding and core materials are obtained from market survey of manufacturer and are not included in this study. The cost analysis and detail magnetic modeling of core material of proposed system configuration are not the subject of this dissertation

3.2.7 Simulation Results of DC-DC Stage and Discussions

A) For DAB_ISOP Topology

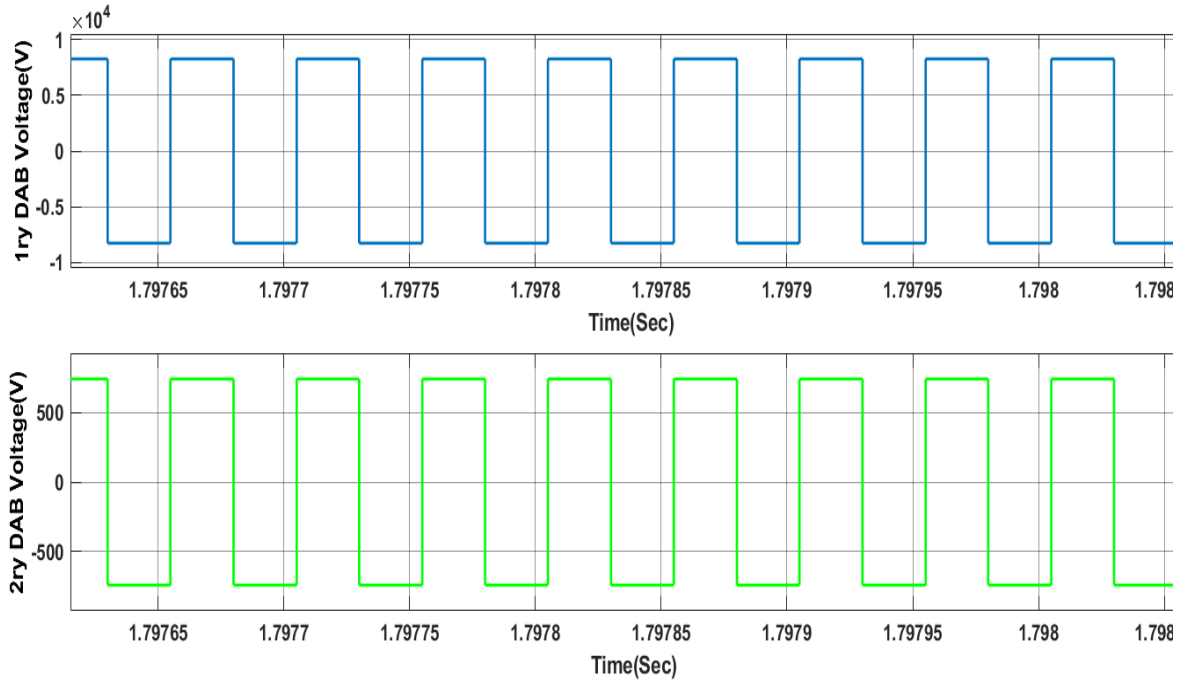


Fig3. 39 MFT primary and secondary output voltages for DAB-ISOP

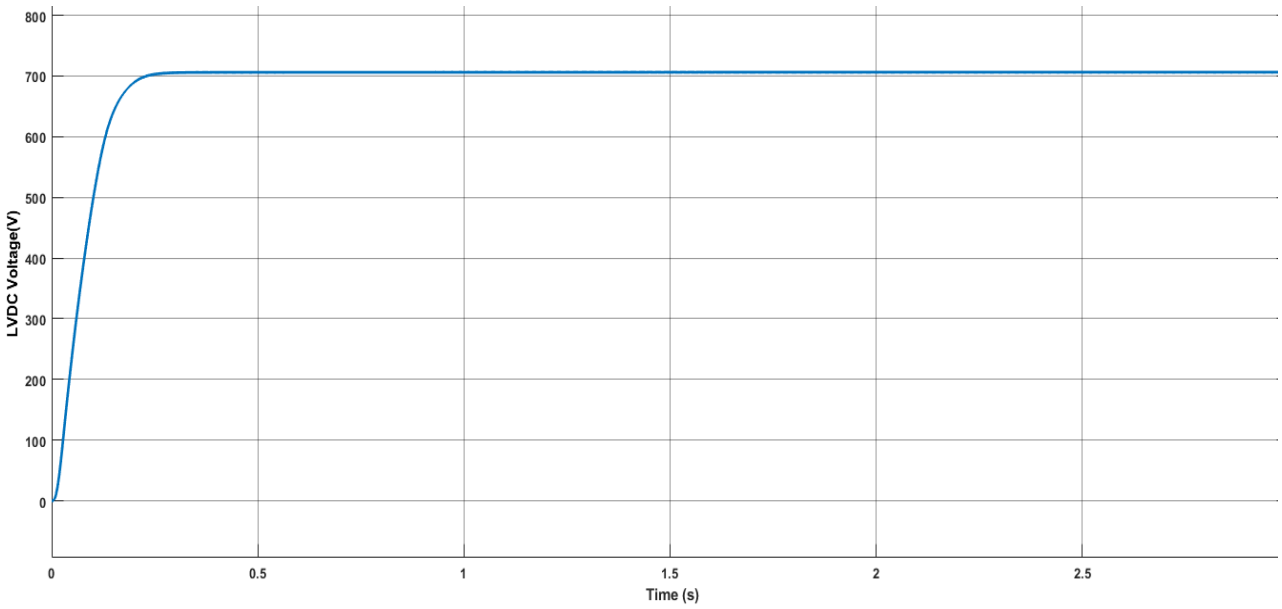


Fig3. 40 Low DC(LDC) link Voltage

Remark: As shown in Fig.3.39 and Fig.3.40, the primary DAB converters share the total input voltage of 24kV. Each DAB converter has a value equals to 8kV. Also the secondary DAB has a peak voltage of 666V and the LVDC output voltage is 700V

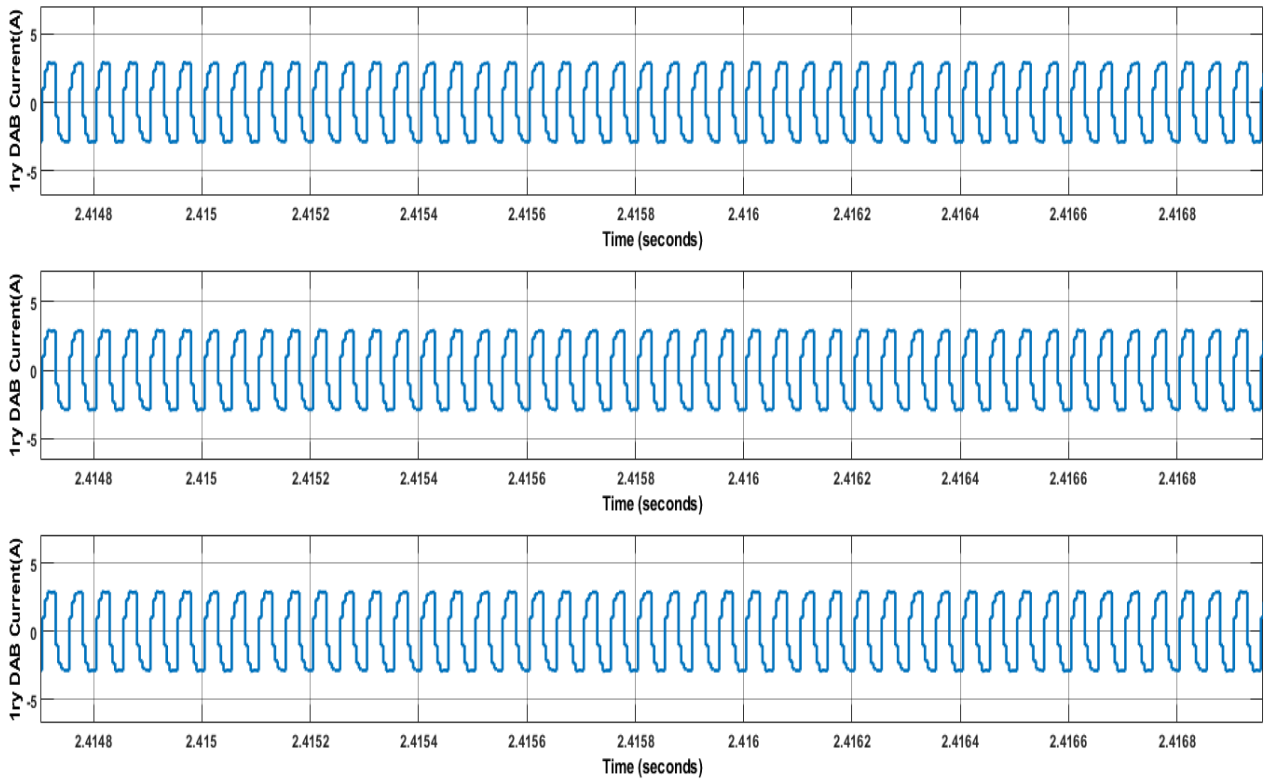


Fig3. 41 Primary DAB-ISOP currents

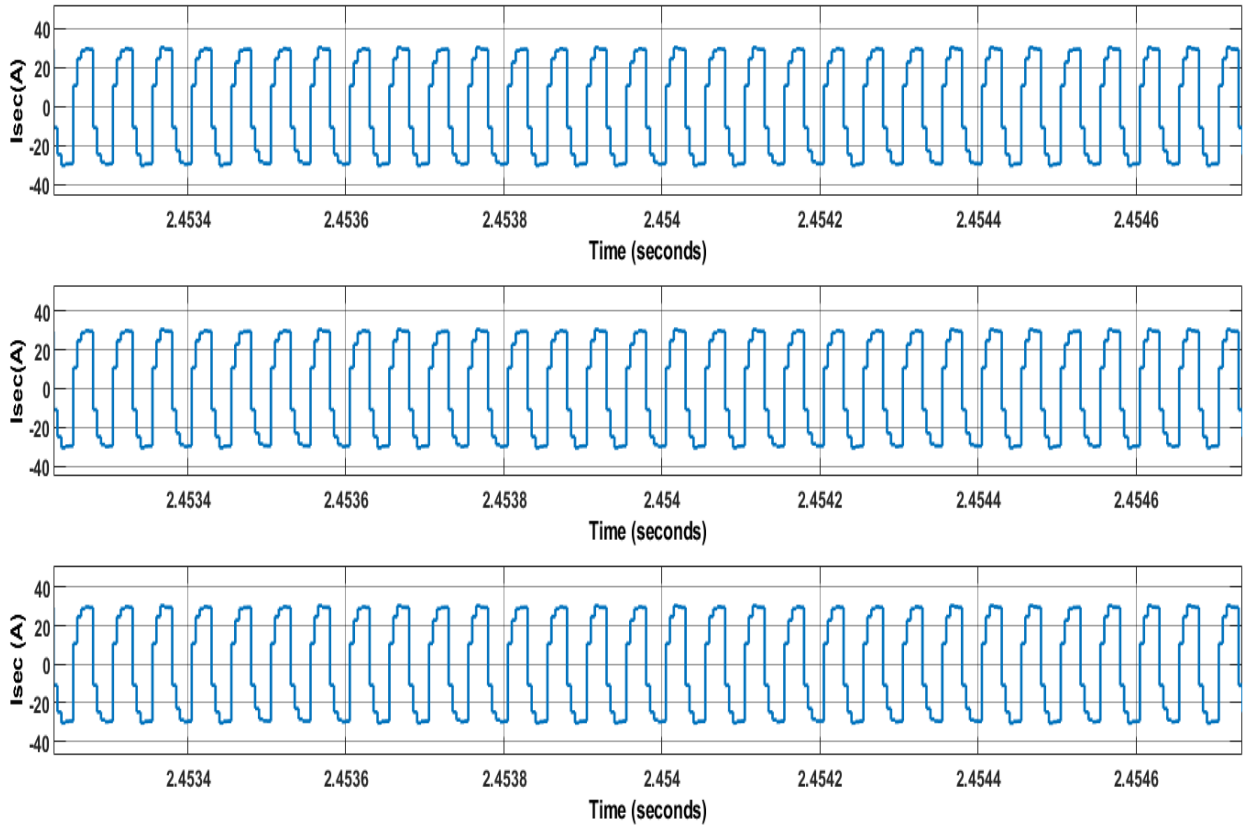


Fig3. 42 Secondary DAB-ISOP current

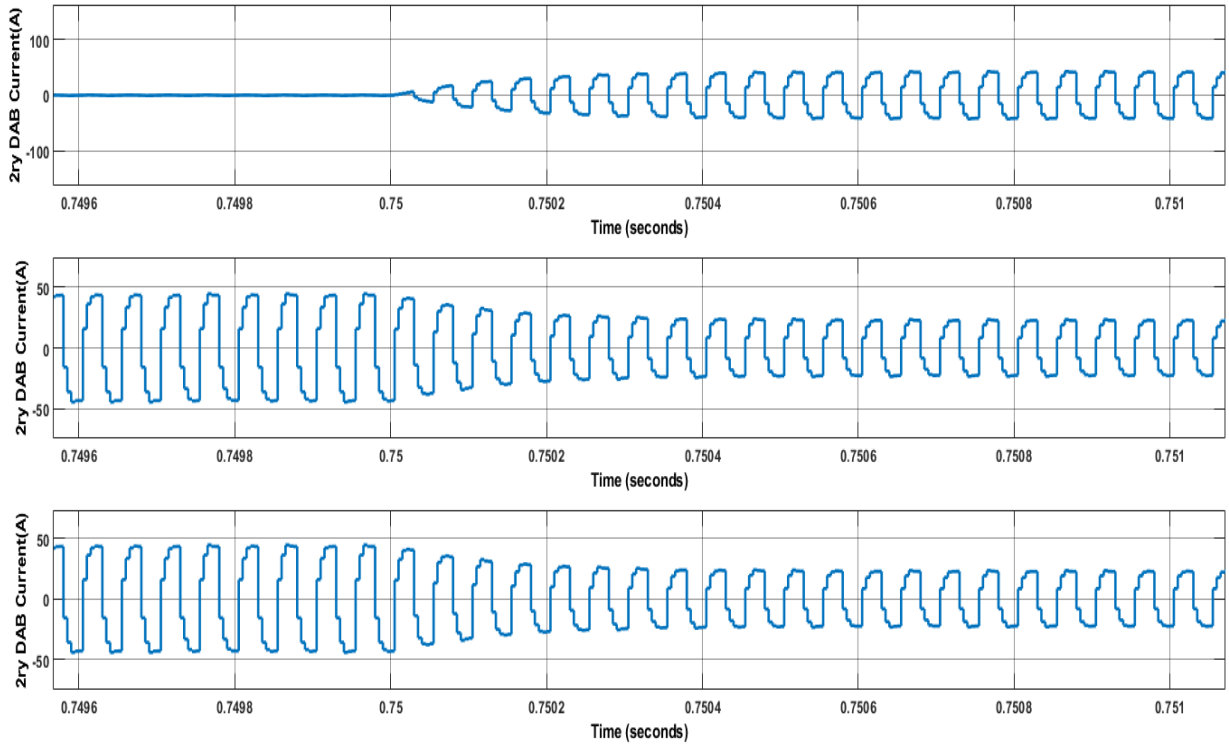


Fig3. 43 Secondary DAB-ISOP currents during fault at DAB_1

Remark: As shown from Fig.3.41 to Fig.3.43, the three primary and secondary DABs share the load current equally when all are active. But, when there is fault in one of the DAB in secondary side, the load current is shared among the un-faulted DABs as shown in Fig.3.43. This fault tolerant feature of the system is very important in increasing the reliability of the overall system and reducing switching loss during light load condition or partial loading condition

B) For AQAB Topology

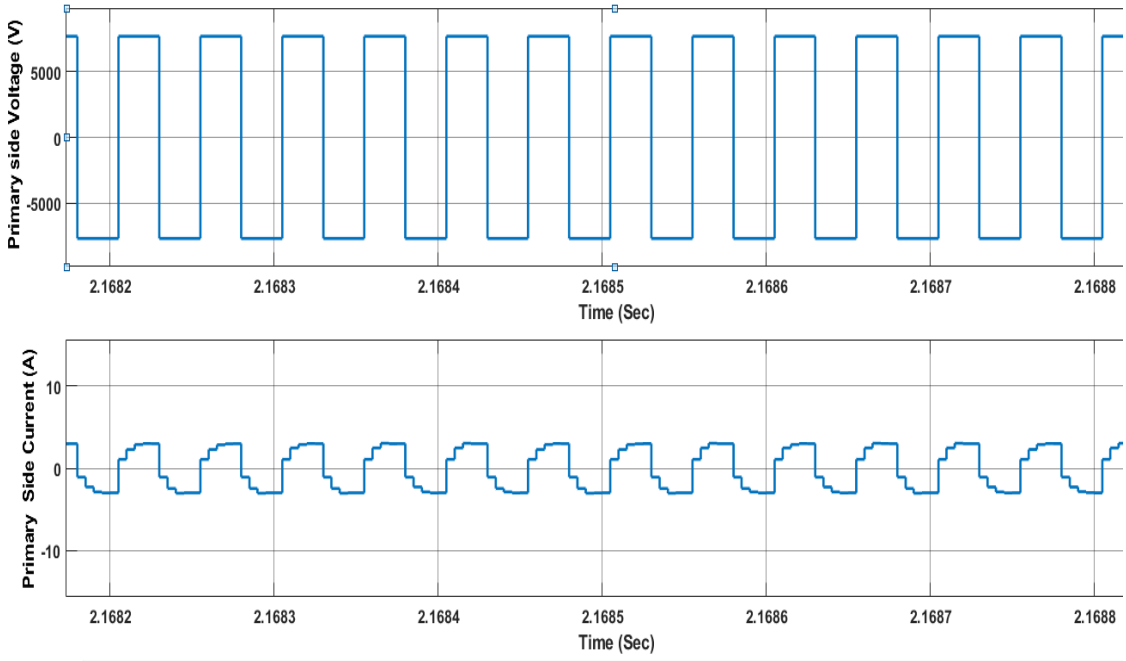


Fig3. 44 Primary side V-I Wave shape for AQAB

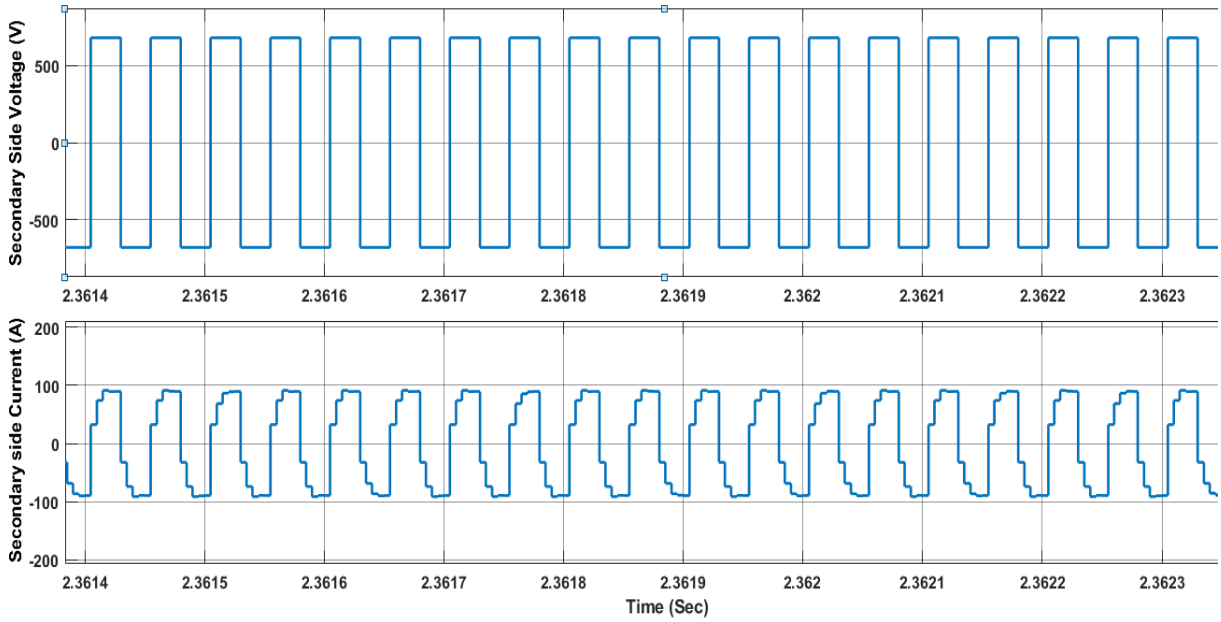


Fig3. 45 Secondary side V-I wave shape for AQAB

Remark: As shown in the Fig.4.44 and 4.45 the primary and secondary side MFT voltages are of square wave shape with peak vales of 8000V for primary and 700V for secondary side. The primary side current is about 3.5A and secondary side current is peak is about 100A when supplying 50kVA load.

C) For SMAB Topology

This topology is almost same in operation with that of DAB_ISOP. Their difference is that the DAB_ISOP uses three single phase MFT whereas the SMAB uses a multi-winding single transformer.

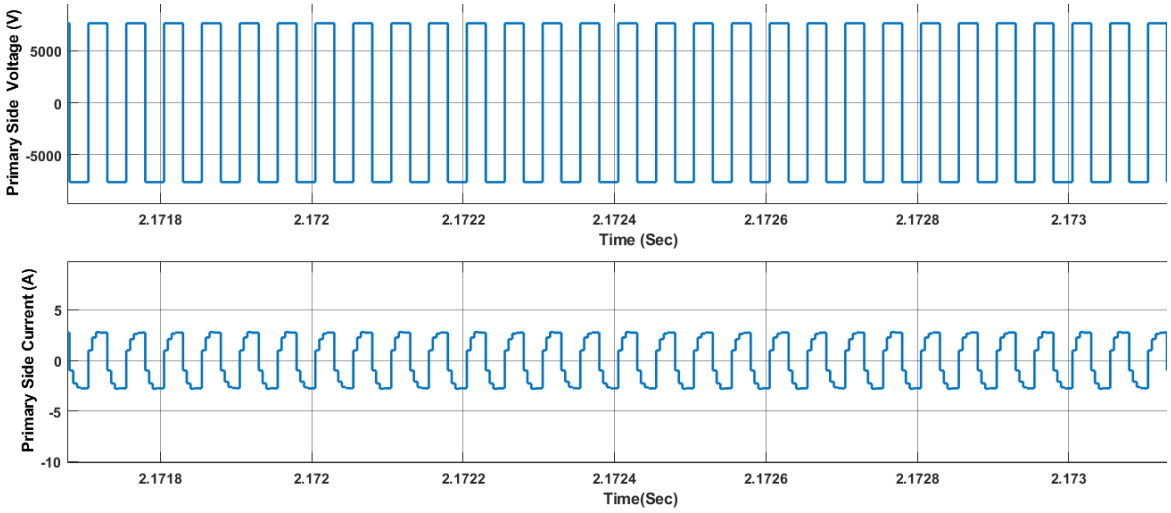


Fig3. 46 Primary side V-I wave shape for SMAB

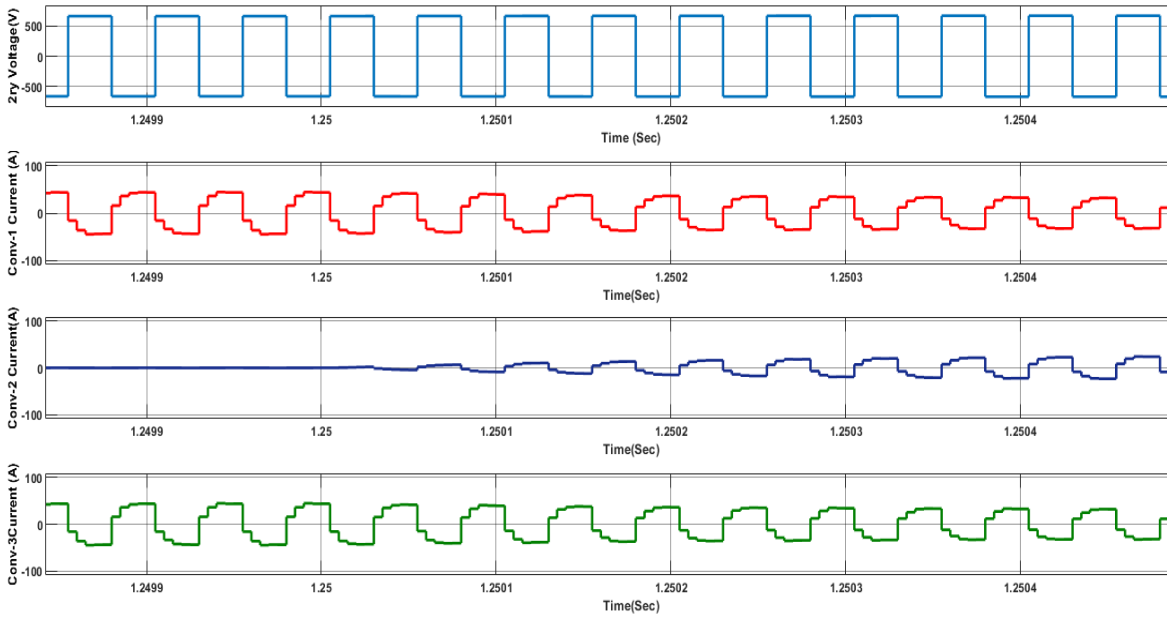


Fig3. 46 Secondary sides V-I wave shape for SMAB

As shown on the V-I wave shape diagram shown in Fig.3.45 and Fig.3.46, the peak primary side voltage is about 8300V and secondary side peak voltage is about 650V. The secondary side current waves show that if one of the converters fails because of fault or deactivated because of partial loading, the load current will be shared among the active converters.

Summary

The DC-DC stage with MFT is implemented for three different converter topologies. The first converter configuration is DAB –ISOP. In this topology, three converters at primary side are connected in series whereas three secondary side active bridges are connected in parallel. This configuration uses three separate MFT and one of the converters can be deactivated during partial loading condition to thereby reducing the semiconductor losses. The second type of converter configuration used is SMAB which utilizes single multiple winding transformer and three active bridges in the primary and secondary sides. This configuration is almost same in operation to DAB-ISOP except use of single multi-winding transformer which can reduce the core loss. The third type of configuration is AQAB which uses three active bridges on the primary side and single active bridge in the secondary side. For this type of configuration, the converters in secondary side should carry full load current. All three configurations are viable for the DC-DC stage with selection criteria based on the cost and availability

3.3 Design and Modeling of Back-End Stage of Modular ST

3.3.1 Introduction

At present time, electric distribution system is constantly changing in its configuration because of the prevalent utilization of renewable energy sources (RES) and hybrid micro grid with modern distributed energy infrastructures. The conventional low frequency distribution transformer is highly challenged by the extra requirements of present time distribution systems. These extra requirements of today's distribution system include bidirectional power and data flow, easy connection to distributed energy resources, energy storage, load compensation, improved power quality and reliability. A smart transformer (ST) can be taken as competent choice to link AC and DC systems running at medium and low voltage levels. The three stage smart transformer is among many configurations of smart transformer that fulfills all extra functionalities demanded by modern distribution system. Back-End converter of the smart transformer (ST) is a voltage source inverter (VSI) interfaced to low voltage (LV) power distribution system or loads. It converts a low DC link voltage at output of DC-DC stage to sinusoidal AC voltage having 220 V (P-N) or 415 V (L-L), 50Hz specification. Because this stage is frequently vulnerable to LV grid disturbances, a careful design of its output filter (common mode and differential mode filter) is required. Use of mature converter topologies, with readily available semiconductors having low blocking voltage (1.2 kV, 1.7kV, 3.3kV) is a well-established and industrially accepted way for converting conventional grid voltage. This stage suffers from challenges of high current and EMI filter design. In order to handle the high current demand, PWM with interleaved approach can be used. Design of EMI filters should be carried out with a great care to minimize injection of a high-frequency disturbance into the input source side. Availability of the neutral conductor is another requirement of this ST stage because low voltage distribution network is based on the configuration of Terra-Terra (TT). Furthermore, this stage is also exposed to load unbalancing and non-linearity, which creates zero sequence current that must be properly handled by the three phase three wire or three phase four wire voltage source inverter (VSI). But the four wires VSI is the most appropriate one with regard to choice of freedom and control of neutral current. Topologies which are most appropriate for back-end converter stage of ST include a typical two-level voltage source inverter (VSI), a three-level neutral point clamp (NPC), and T-type topologies (Mahammad A,et'al.,2020).

However, the conventional two level and three level voltage source inverter used in low voltage systems suffers from high conduction loss, switching (turn-on and turn-off) loss and high dV/dt stress because of its high frequency operation requirement. Moreover, the high harmonic content (THD) of the output voltage and current in conventional two level and three level inverters causes various adverse effects such as additions of harmonic loss, reduction in system efficiency, interference with communication devices, oversizing of neutral conductors in three phase four wire system, mal operation of protection devices and damage to motor loads as a result of sequence currents. As the result of the above mentioned shortcomings, the two and three level inverters are not used for high power medium/high voltage application. The solution to above cited problem is using multilevel inverters which can be of diode clamped type, flying capacitor type, CHB or MMC. The neutral point diode clamped multilevel inverter can produce high voltage levels with good THD values, but active power control and modularity is difficult. The flying capacitor multilevel inverter is similar in operation as diode clamped, but has large number of storage capacitors. Although control of active and reactive power is possible in this type of inverter, modularity and scalability is a problem (Gautam Ghosh, et'al., 2017; Alex Ruderman 2014). For developing highly efficient inverters, cascaded H-bridge (CHB) and modular multilevel converter (MMC) based modular inverters having low switching frequency operation are the focus of this study. Although CHB and MMC based modular converter have more parts than a non-modular solution, they have many advantages over other topologies. These advantages include cell and phase modularity, simple voltage and power scaling by combing identical cells, possibility of using single capacitor as a means of energy storage for modules, easy bypass of faulty cells during faults (fault ride through capability), low dV/dt, reduced electromagnetic interference (EMI), cost effectiveness, good transient response and possibility of using readily available low voltage power switches.

Literature survey shows that different PWM techniques have been discussed in to operate a BEC (LI Wei, et'al., 2011). Sub-module capacitor voltage unbalancing is a common problem in BEC.

Design and performance evaluation of CHB and MMC based nine level back-end converters applied to 0.415kV; 50kVA low voltage distribution system will be focused in this section.

3.3.2 Configuration of modular converter for BEC

The two-level and three-level VSI suffers from high dV/dt, di/dt and lack intelligent operation (activation and deactivation of modules) in the time of partial loading of distribution grid. A possible solution to these problems is to use different types of multilevel inverters which utilize low voltage switches and low switching frequency as discussed in [164]. The CHB and MMC shown in Fig1 and Fig.2 are proposed modular back-end converter for low voltage distribution system The basic building block of CHB based modular back end converter is the full bridge sub-module made of four power electronic switches connected in H-bridge shape as shown in Fig.3(b). One of draw backs of the CHB based modular BEC is that it uses a separate voltage source for each sub-module. For the MMC based modular BEC many topologies can be used as basic building blocks, but the half bridge sub-module shown in Fig.3 (a) is selected as it has low switch count and hence low switching and conduction losses (Marcelo A,et'al.,2021; Keerthi Gopal,et'al.,2022).

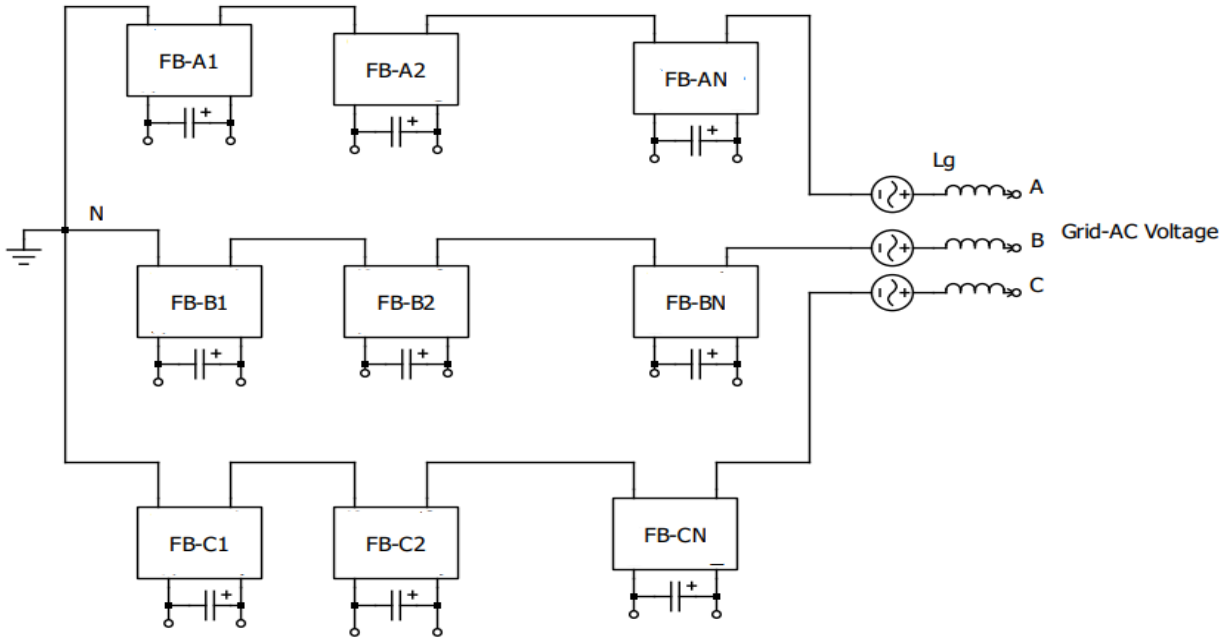


Fig3. 47 CHB based modular converter

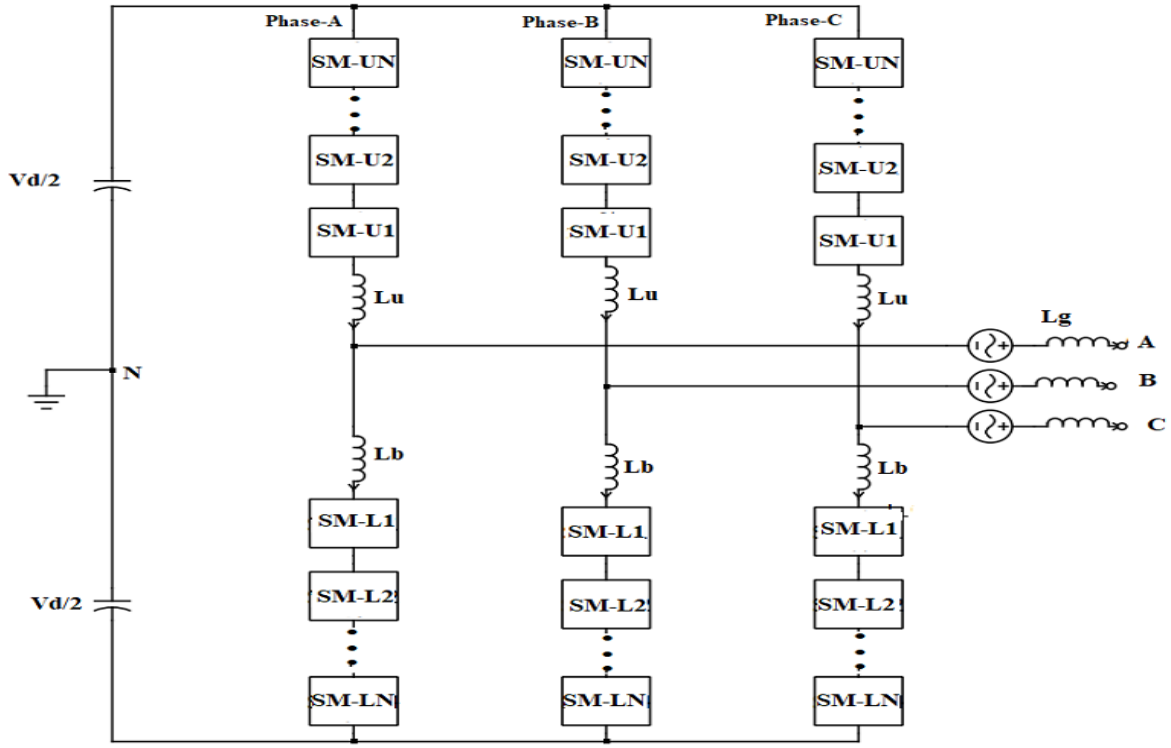


Fig3. 48 MMC based modular converter

3.3. 3 Design and analysis of modular converter

For design of back-end converter, issues such as converter building block, output voltage magnitude and quality, input DC magnitude and load type to be served should be taken in to consideration. With respect to power electronic building block (PEBB), half bridge (HB) and full bridge (FB) utilizing IGBT or MOSFET technology as shown in Fig.3.49 can be used in the modeling of back-end converter of smart transformer

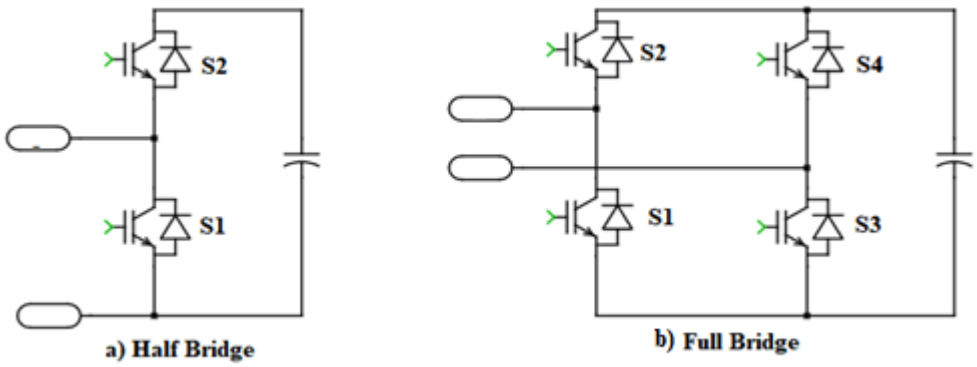


Fig3. 49 Converter basic building block

The half bridge IGBTs power sub-module from which MMC is built is operating in complementary mode and depending on states of the upper and lower switches and current direction, the sub-module can be in one of four states described in Fig.3.50

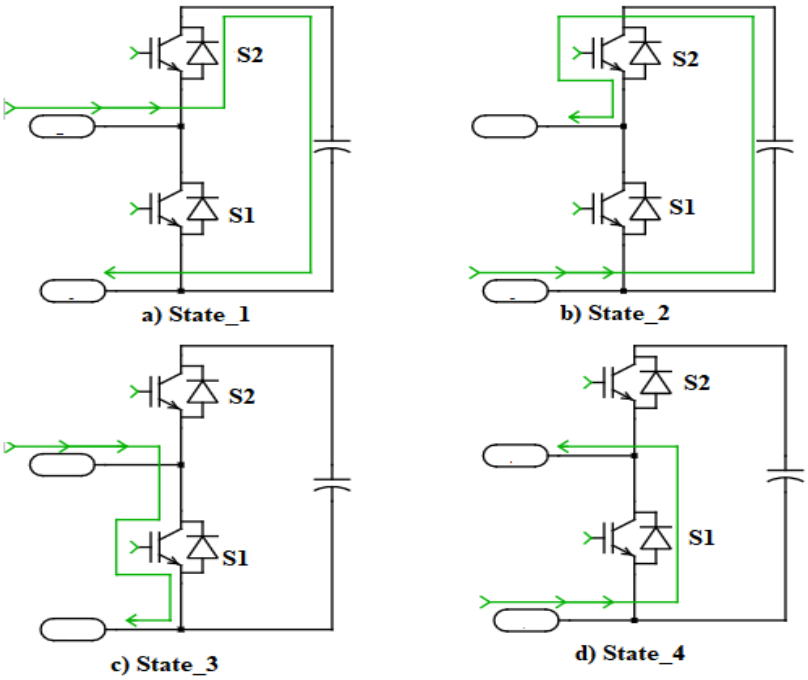


Fig3. 50 Half- bridge sub-module switch transition states

As shown in fig.4, when the sub-module (SM) is in state one, the SM capacitor is inserted and charging through upper clamping diode, giving SM voltage equals capacitor voltage. When the SM is in state-two, its capacitor is inserted and discharging through the upper IGBT, having SM voltage equal to capacitor voltage. When the SM is either in state-three or state-four, its capacitor is bypassed, hence the SM voltage equals zero.

The smallest integrated power module used to implement back-end converter is selected based on the type of application and maximum load current and voltage requirement. Based on the power distribution system specification, the maximum load current is 70A, and line-to-line AC voltage is 415V with lagging power factor ranging from 0.95 to 1. Therefore, IGBTs /MOSFET having blocking voltage rating of 200V or greater and current rating of 80A or greater will be considered from device manufacturers such as CREE, Infineon, ROHM, etc. Sufficient safety factor of two (1.1) is used to de-rate the device ratings so that operation in the transient condition is safe. Based on the DC link voltage and SM blocking voltage, four (4) SMs are required to construct the BEC. Nine levels (9-level) back-end converter based on CHB and MMC topology are considered in this dissertation work.

After evaluation of semiconductor device manufacturer's data sheet, the following semiconductor power switches are chosen for design and analysis and simulation purpose

Table3.5 Chosen Semiconductor power switches for system

(https:// www.rhom.com; https://assets.wolfspeed.com)

Device part number	Voltage rating (V)	Current rating(A) @25^{0}C	Manufacturer
SiC-power MOSFET (IRFP4668PbF)	200	130	IR
SiC-Power MOSFET (IRF200P223)	200	100	Infineon

For analysis of three-phase back end converter of smart transformer based on MMC, a single phase equivalent circuit illustrated **in Fig.3.51 below** is derived from Fig.3.48

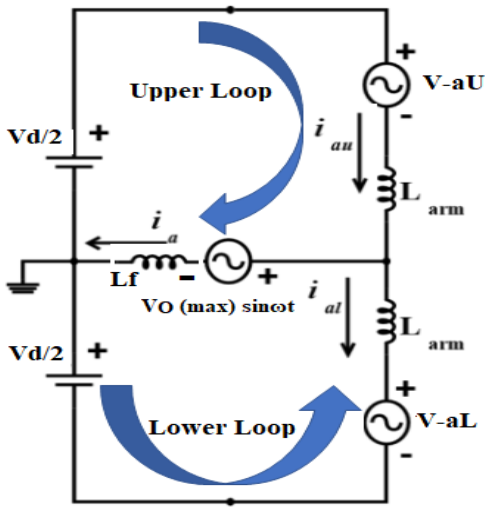


Fig3. 51 Single phase equivalent circuit of MMC

Based on equivalent circuit on Fig.5.51, the currents through switches and diodes in the upper and lower arms of phase leg are given as follows (Y. Zhang, et'al., 2012).

$$I_{av\,US} = \frac{1}{2\pi}(mI_{dc}\cos\alpha - \frac{1}{2}I_{pp}) \quad (3.35)$$

$$I_{av\,UD} = -\frac{1}{2\pi}(mI_{dc}\cos\alpha - \frac{1}{2}I_{pp}) \quad (3.36)$$

$$I_{av\,LS} = \frac{1}{2}I_{dc} + \frac{1}{2\pi}(mI_{dc}\cos\alpha + \frac{1}{2}I_{pp}) \quad (3.37)$$

$$I_{av\,LD} = \frac{1}{2}I_{dc} - \frac{1}{2\pi}(mI_{dc}\cos\alpha + \frac{1}{2}I_{pp}) \quad (3.38)$$

$$I_{rms\,US}{}^2 = \frac{1}{2\pi}\left[\frac{1}{2}\left(\frac{1}{8}I_{pp}{}^2 - I_{dc}{}^2\right) - \frac{5}{6}I_{dc}I_{pp} + m\cos\alpha\left(I_{dc}{}^2 + \frac{1}{8}I_{pp}{}^2\right)\right] \quad (3.39)$$

$$I_{rms\,UD}{}^2 = \frac{1}{2\pi}\left[\frac{1}{2}\left(\frac{1}{8}I_{pp}{}^2 - I_{dc}{}^2\right) + \frac{5}{6}I_{dc}I_{pp} - m\cos\alpha\left(I_{dc}{}^2 + \frac{1}{8}I_{pp}{}^2\right)\right] \quad (3.40)$$

$$I_{rms\,LS}{}^2 = \frac{1}{2\pi}\left[\frac{1}{2}\left(\frac{1}{8}I_{pp}{}^2 + 3I_{dc}{}^2\right) + I_{dc}I_{pp} + m\cos\alpha\left(I_{dc}{}^2 + \frac{1}{6}I_{pp}{}^2\right)\right] \quad (3.41)$$

$$I_{rms\,LD}{}^2 = \frac{1}{2\pi}\left[\frac{1}{2}\left(\frac{1}{8}I_{pp}{}^2 + 3I_{dc}{}^2\right) - I_{dc}I_{pp} + m\cos\alpha\left(I_{dc}{}^2 + \frac{1}{12}I_{pp}{}^2\right)\right] \quad (3.42)$$

$$I_{dc} = m\cos\alpha\left(\frac{Ipp}{4}\right) \quad (3.43)$$

where, m is index of modulation, I_{PP} is phase current peak to peak value, **Cosα** is load power factor, **Idc** is the phase leg DC current, $\mathbf{I}_{av\,US}$, $\mathbf{I}_{av\,LS}$, $\mathbf{I}_{av\,UD}$, $I_{av\,LD}$ are the average currents flowing in switches and diodes at upper and lower arm of phase leg.

$\mathbf{I}_{rms\,US}$, $\mathbf{I}_{rms\,LS}$, $\mathbf{I}_{rms\,UD}$ and $\mathbf{I}_{rms\,LD}$ are the RMS current values of switch and diode in the upper and lower side respectively.

The input DC power and output AC power can be related by:

$$P_{dc} = V_{dc}I_{dC} = P_{ac} + losses = 0.5m\frac{Vdc}{2}I_{pp}\cos\alpha + Losses \quad (3.44)$$

The losses produced in power electronic system are caused by intrinsic components such as power electronic devices and ohmic resistors (stray resistance). Power electronic devices dissipate losses due to their non-ideal nature. These losses can be grouped in to conduction losses, switching losses and blocking losses. Blocking loss, which is caused by small leakage current, can be ignored in most analysis without causing much inaccuracy. For power electronic devices integrated with diode such as the IGBT/MOSFET with freewheeling diode, losses should be individually specified for both the semiconductor switch and diode.

The losses that happen while the IGBT or fast recovery diode is turned-on and conducting current are referred to as conduction losses. Conduction power loss is determined by product of the on-state voltage and the on-state current. However, multiplying the total conduction loss by duty factor is the requirement in applications where PWM is used.

The total conduction loss dissipated by the IGBT integrated with freewheeling diode is given by the following equation.

$$\mathrm{Pcond(tot)} = \mathrm{Pcond(IGBT)} + \mathrm{Pcond(Diode)} \quad (3.45)$$

$$\mathrm{Pcond(IGBT)} = \frac{1}{\mathrm{T}}\int_{0}^{\mathrm{T}} [\mathrm{V_{CE}(t)} * \mathrm{I_C(t)}]\mathrm{dt} \quad (3.46)$$

The average conduction loss of IGBT can be computed by the following equation:

$$\mathrm{Pav}(cond) = V_{CE(S)} * I_C * \delta \quad (3.47)$$

Where, δ refers to device duty cycle

The transitions of IGBTs/MOSFETs and FRD from on-state to off-state and vice versa do not occur instantly which results in switching losses. Both the current flowing through and the voltage across the device during transition interval are remarkably greater zero which results in large instantaneous power losses.

Equations to determine the switching power losses for an IGBT/MOSFET and FRD are given bellow:

$$\mathrm{Psw(IGBT/MOSFET)} = (\mathrm{E_{ON}} + \mathrm{E_{OFF}}) * \mathrm{f_{SW}} \quad (3.48)$$

$$\mathrm{Psw(FRD)} = \mathrm{E_{rec}} * \mathrm{f_{SW}} \quad (3.49)$$

The turn-on energy (Eon), the turn-off energy (Eoff) in the IGBT and the reverse recovery energy in the FRD (Erec) are functions of collector current, collector voltage, gate resistance and junction temperature.

Normalization of the switching losses with the conditions provided for any application with the nominal values from the datasheet is essential.

$$\mathrm{Psw(IGBT/MOSFET)} = \left(\frac{\mathrm{E_{ON}} + \mathrm{E_{OFF}}}{\pi}\right) * \mathrm{f_{SW}} * \frac{\mathrm{I_{pk}}}{\mathrm{I_{nom}}} * \frac{\mathrm{V_{DC-link}}}{\mathrm{V_{nom}}} \quad (3.50)$$

$$\mathrm{Psw(FWD)} = (\mathrm{E\_rec}/\pi) * \mathrm{f\_SW} * \mathrm{I\_pk/I\_nom} * \mathrm{V\_(DC - link)/V\_nom} \quad (3.51)$$

From determination of the switching and conduction losses of IGBT/MOSFET and FRD, it is possible to obtain total loss for determining efficiency of the system and the junction temperature of the devices.

$$\mathrm{P(tot)} = \mathrm{P_{Cond}(IGBT/MOSFET)} + \mathrm{P_{SW}(IGBT/MOSFET)} + \mathrm{P_{Cond}(FRD)} + \mathrm{P_{SW}(FRD)} \quad (3.52)$$

Piecewise linear electronics circuit system (PLECS) uses Look up table, formula or combination of lookup table and formula approach to determine conduction and switching losses. Lookup approach uses interpolation and extrapolation methods to find the device loss values based on the set of data points taken from datasheet. The novelty of this research work is justified by the integration of device thermal models and efficiency calculation models of converter. Thermal implementation model for single and multiple IGBT/MOSFET integrated with FWD is given in section 2.9. As shown in the diagram**,** for power electronic system containing multiple switches, the same approach used for single IGBT can be used with a common heat sink shared among all semiconductor switch packages

Based on the thermal data collected from device manufacturer, switching loss and conduction loss models of the selected semiconductor switches are generated as shown in Fig.3.52(a to c)

For efficiency calculation of power electronic system, periodic average for conduction losses and periodic impulse average for switching losses obtained from probe output are summed up as described in Fig.3.53 (http://www.plexim.com, user manual).
Converter efficiency calculation model described in Fig.3.53 uses these thermal loss models for loss and efficiency calculation of the system.

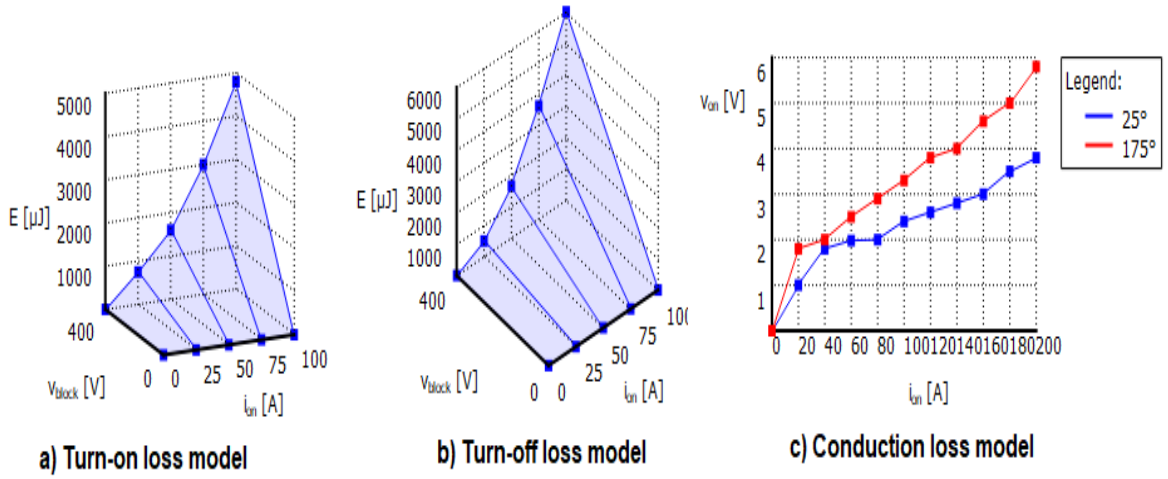


Fig3. 52 Loss model of IGBTs/MOSFET with FRD

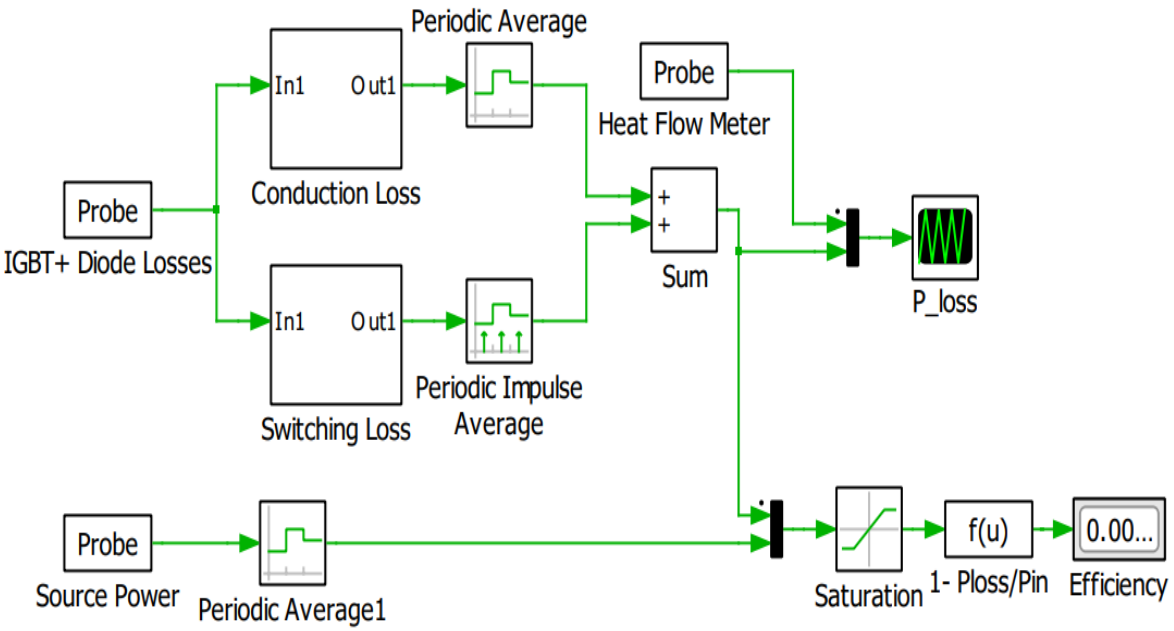


Fig3. 53 Efficiency calculation model

3.3.4 Modulation strategy

Numerous modulation strategies for the MMCs have been proposed by many researchers such as, nearest level control (NLC), Level Shifted Carrier based PWM and phase shifted pulse width modulation (PSPWM) and space vector modulation (SVM) which have been discussed in section 2.6

Due to its ease of use in low-voltage modules, multi-carrier pulse width modulation strategies are frequently employed for MMC-based modular converter. Multi-Carrier PWM is classified as Phase shifted PWM and level shifted and techniques (Keerthi Gopal , et'al.,2022). Level shift PWM creates complexity in modulation circuit as the number of voltage levels increases and hence a phase shift modulation is used in this project.Using PS-PWM maintains SM capacitor voltage with a PI controller, and there is no need of using a sorting algorithm as in LS-PWM. The superior performance of PS-PWM over LS-PWM is revealed when the level size of output voltage is large, To create the switching signals for a PS-PWM multilevel converter, multiple carriers are needed. Over the course of the switching cycle, multiple carriers exist simultaneously. Typically, a multilevel converter will need as many carriers as there are voltage levels in the output voltage, excluding the one. If N is the number of sub-modules in each arm, then the phase difference between the carriers can be found using equation below (D. A. Guzman, 2013).

$$\theta = 360/N \qquad (3.53)$$

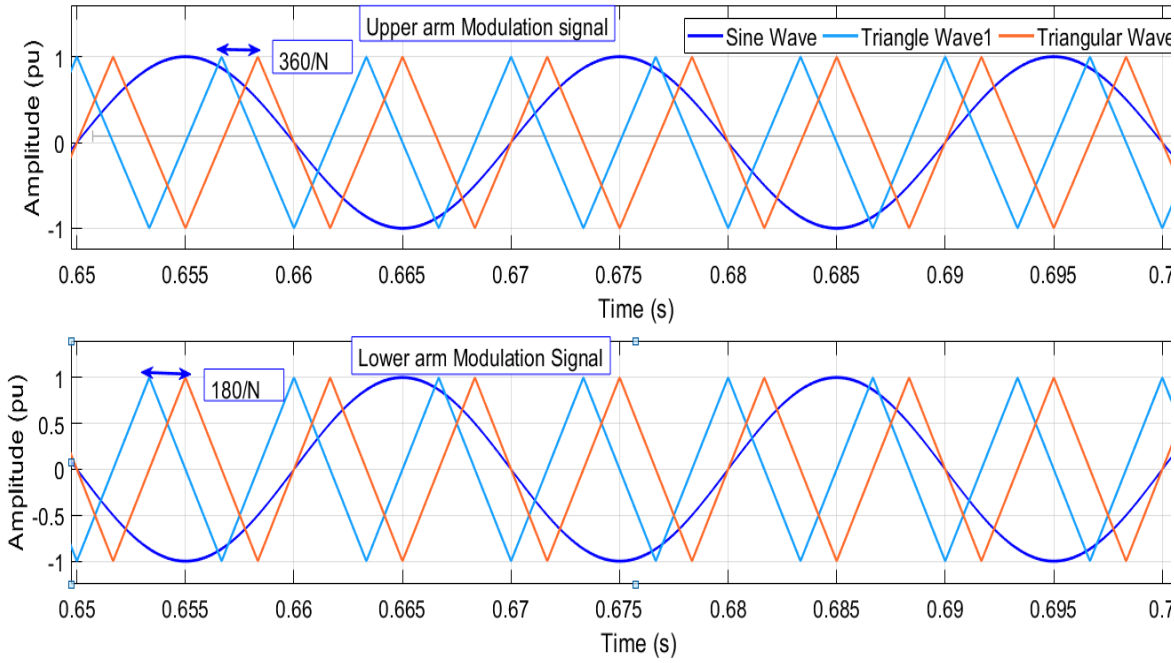


Fig3. 54 Interleaved phase shift modulation

Use of MMC based back end converter gives a chance to scale up the number of levels in output voltage by factor of 2 for the same structure, by using interleaved phase shift modulation having π phase angles between the upper and lower arm carriers. This feature of MMC based BEC gives output voltage with better THD values (Thenmalar Kaliannan, et'al., 2021; Harin.M.Mohan, et'al., 2017). In order to utilize the above advantage, interleaved phase modulation technique is applied in this project work

3.3.5 Simulation result of BEC and discussion

For simulating the models of BEC of smart transformer based on CHB and MMC topologies, three phase star connected inductive load(R-L load) with power factor ranging from 0.95 to 1 has been used. The load has a maximum rating of 50kVA and its selection is based on real distribution transformer supplying three phase loads of small village. A steady state system analysis is used to see evaluate the performance of modeled systems

In Table.3.7, the parameter values of distribution system and converters are listed according to the actual load demand in the distribution system. These absolute values were incorporated into the PLECS/Simulink modeling to create the system.

Table3.6 Technical design parameters of the BEC System

Parameters	Value
Output AC Line Voltage(Vg)	415V
Maximum Power(S)	50kVA
Load Power factor	0.95 to 1 lagging
MMC arm inductance (L_arm)	10mH
MMC arm resistance (R_arm)	0.1 Ω
Sub-module capacitance (C_{SM})	1000µF
Distribution system frequency(f_g)	50Hz
Carrier frequency (f_c)	1kHz
Modulation index	0.9 - 1
Type of Modulation	Interleaved Phase shift PWM
Input DC Voltage	700V for MMC and 85V for CHB
No of Sub-module per arm (SM)	4

Note that the load is treated as a constant PQ type having apparent power of 50kVA and drawing a current of 69A in 415 V (L-L).

A) Results for CHB based BEC

A.1 Performance for R-L load

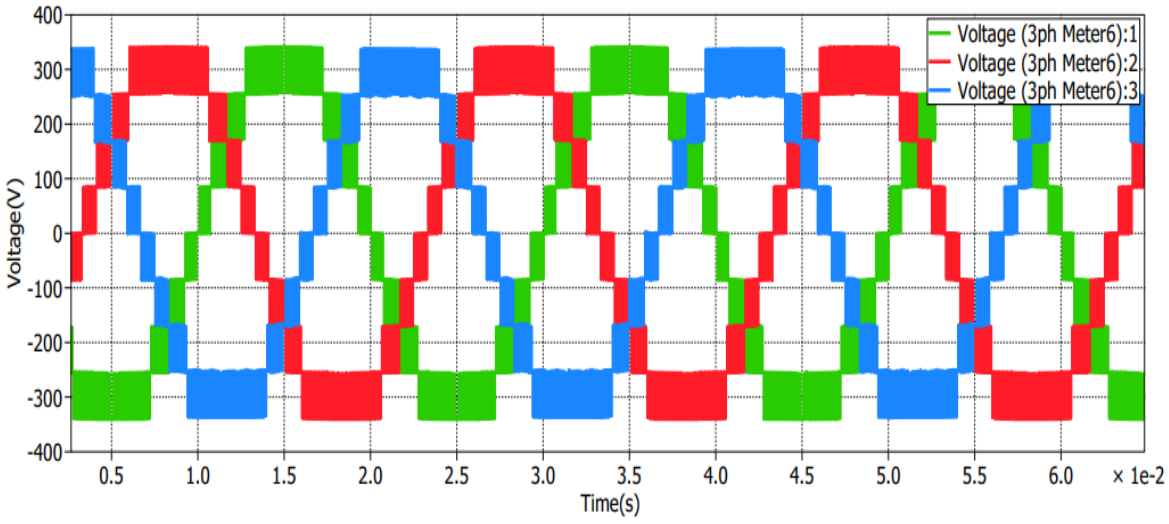


Fig3. 55 Three phase voltage wave form

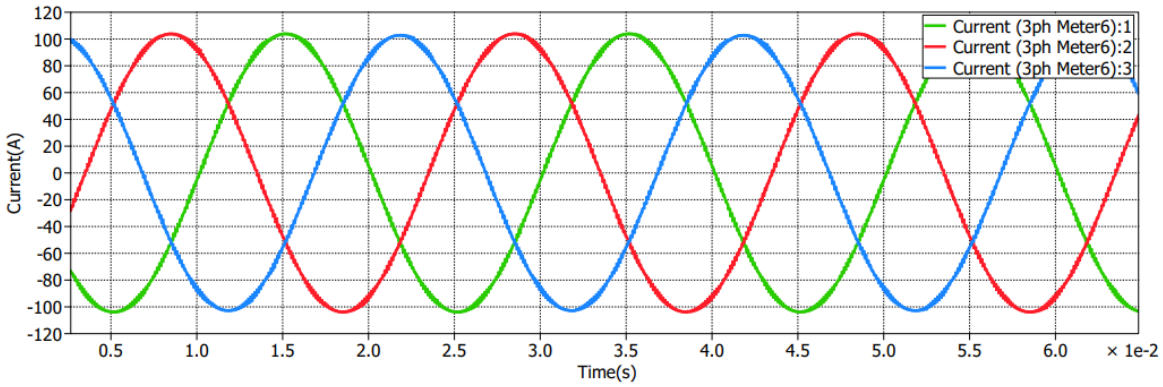


Fig3. 56 Three phase current wave form

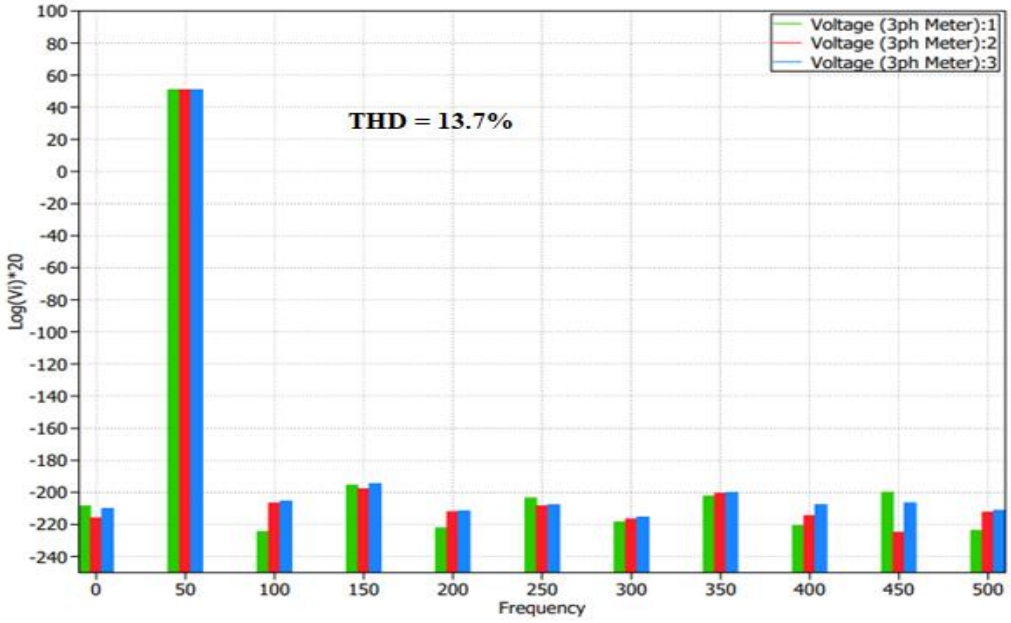


Fig3. 57 Fourier spectrum of phase voltages for N= 10 (N refers to integer multiplying fundamental frequency)

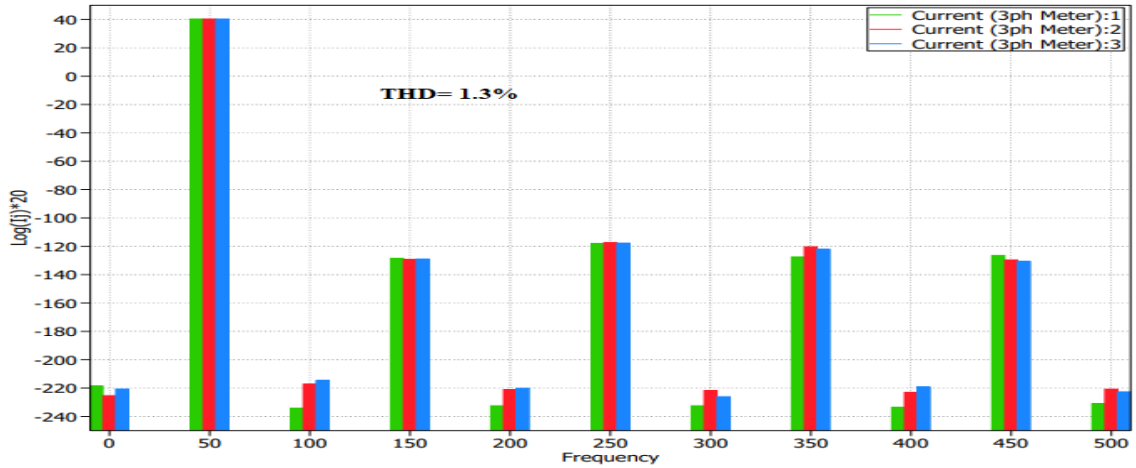


Fig3. 58 Fourier spectrum of phase currents for N=10

As shown from Fig.3.55 to Fig.3.58, CHB based BEC yields nine level output voltage with

THD value of 13.7% while its load current for R-L load is about 73A(RMS) with THD value of 1.3% . The THD value for N-harmonic order is expressed as common logarithm multiplied by 20.

A.2 Performance for load change (from 25kW to 50kW)

The demand of the load in distribution system changes dynamically as a result of changes in daily activities. The performance of the system for demand changes from 25kW to 50kW is shown below:

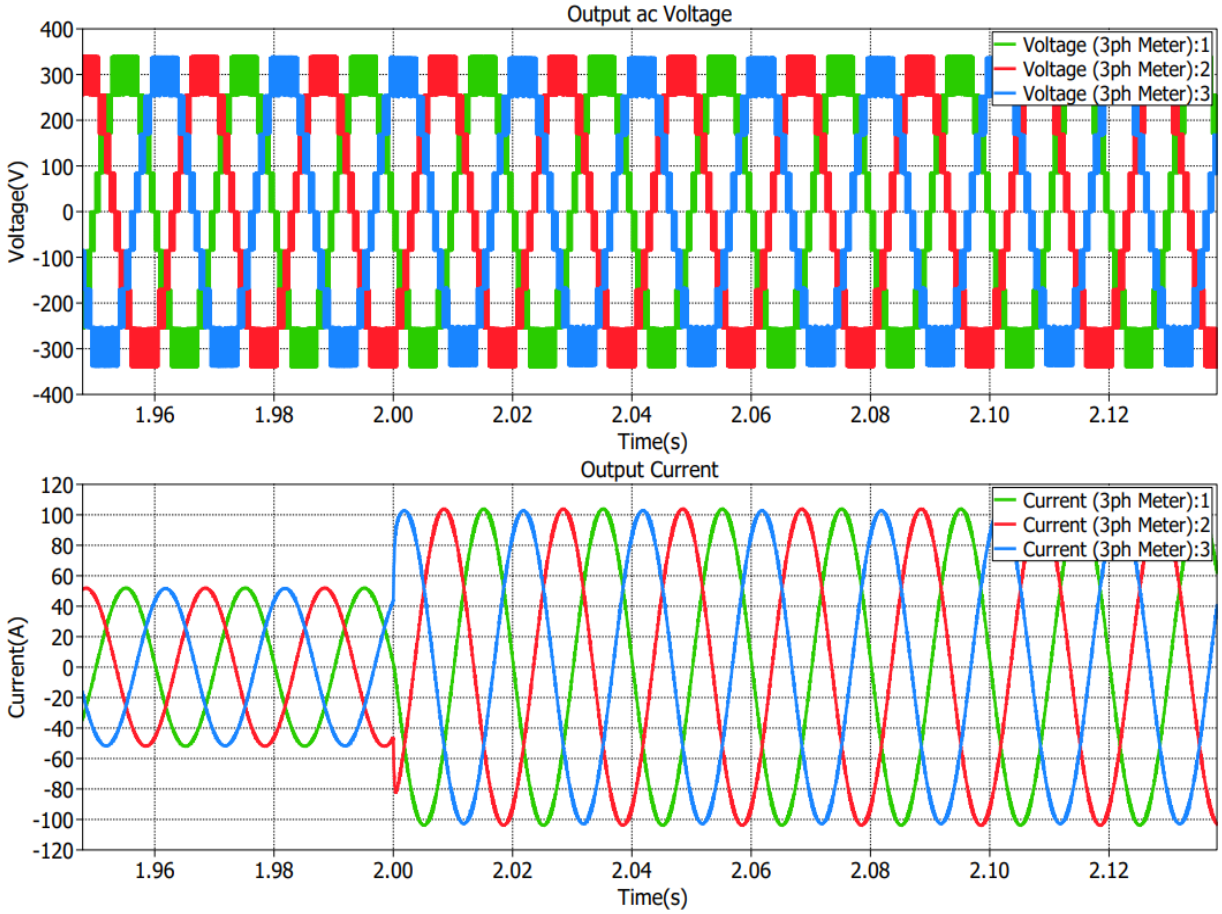


Fig3. 59 Performance for Load changes

As shown in the Fig.3.59, when load demand steps from 25kW to 50KW, the current magnitude is doubled while there is no change in the voltage magnitude.

A.3 Performance for changes in carrier frequency and modulation index

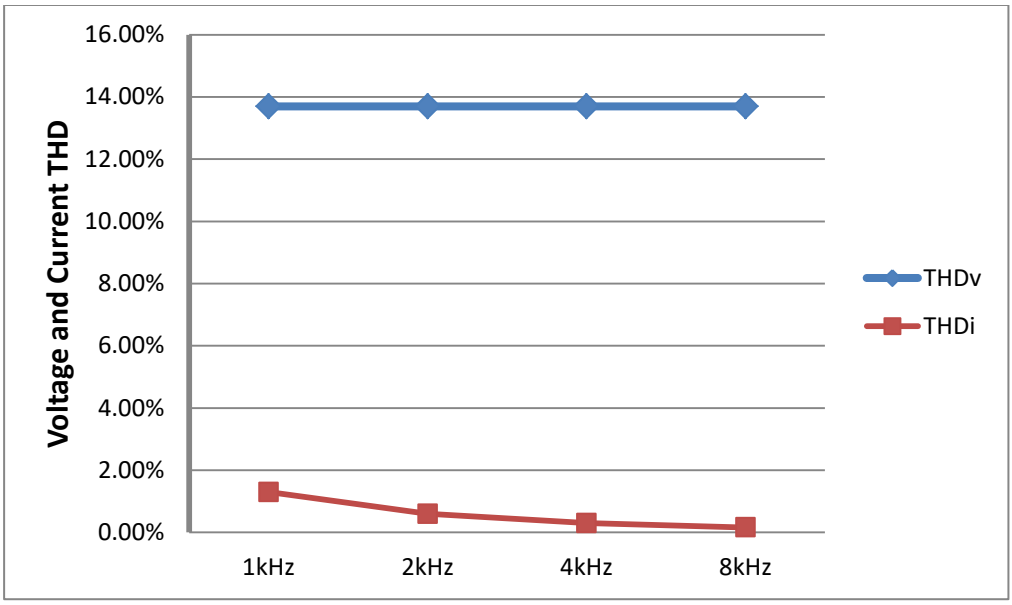


Fig3. 60 Changes in THD as function of carrier frequency

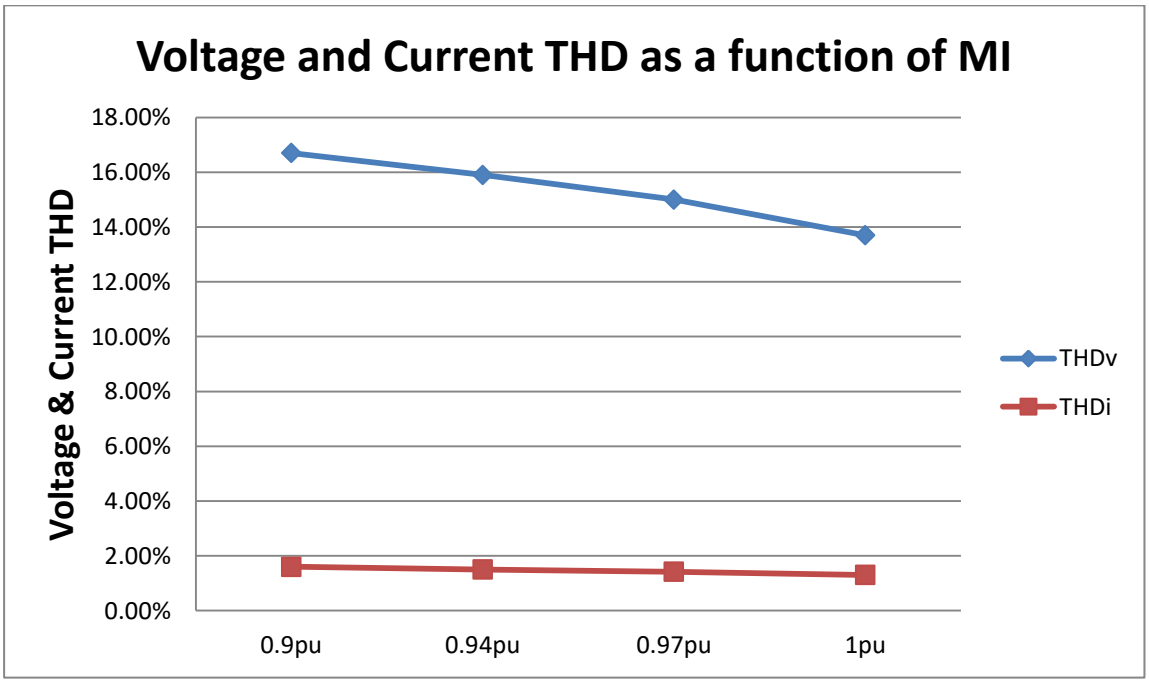


Fig3. 61 Changes in THD as function of modulation index

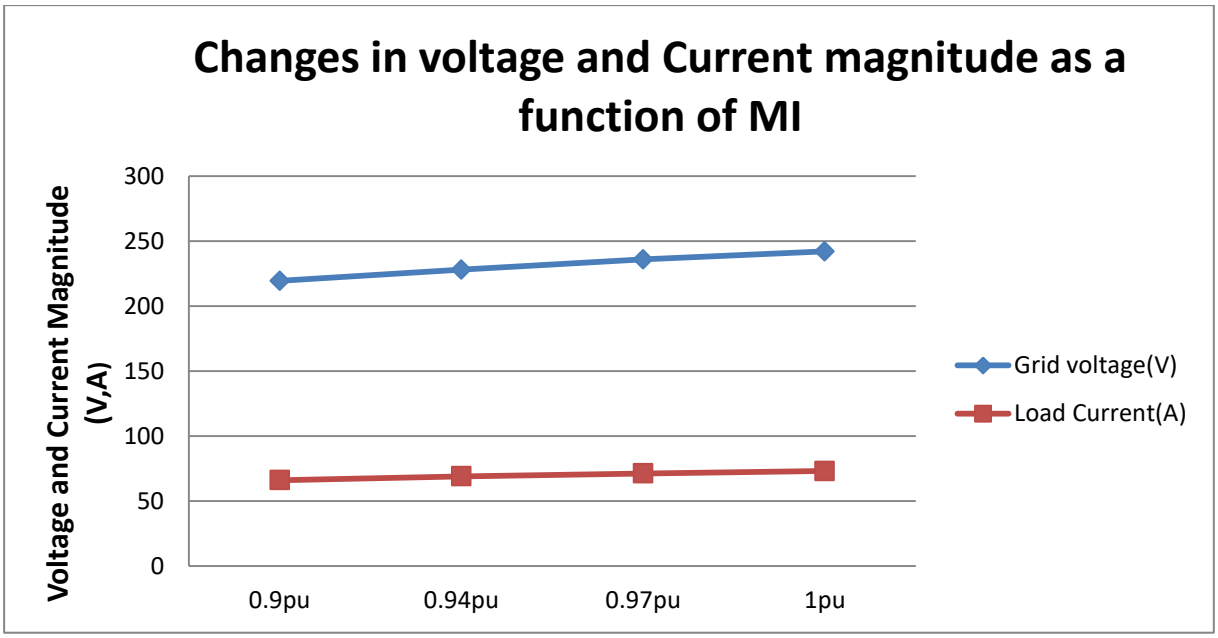


Fig3. 62 Changes in Voltage and Current magnitude as a function of modulation index

The results shown from Fig.3.60 to Fig.5.62 show that an increase of carrier frequency from 1 kHz to 8 kHz causes a decrease in the current THD values while the voltage THD value is not affected. Increase in modulation index (Mi) from 0.9pu to 1pu cause a substantial decrease of the voltage THD value while the decrease in current THD value is small. Decrease in modulation index from 0.9pu to 1pu increases the magnitudes of both voltage and current.

B. Simulation result for MMC based BEC

B.1 Output voltage and current for R-L load

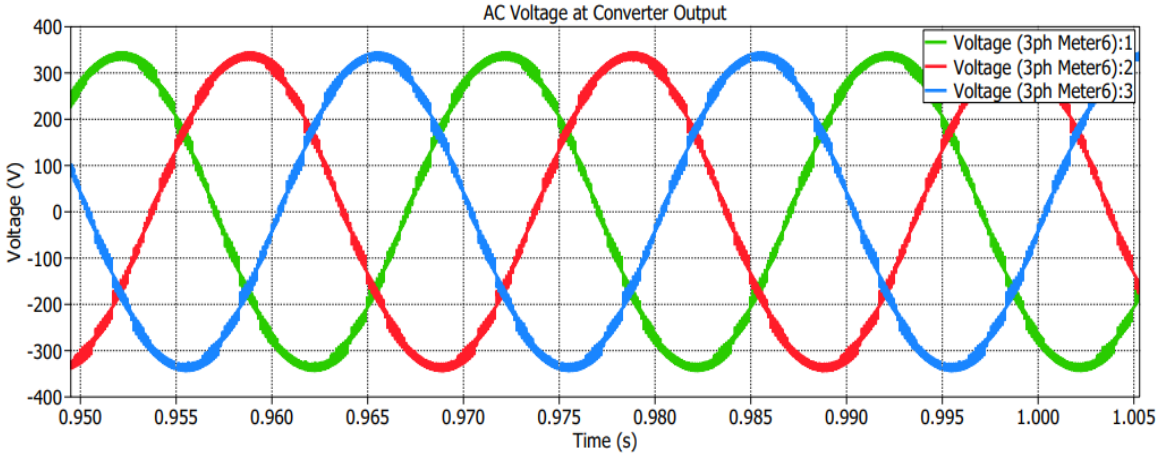


Fig3. 63 AC Voltage Wave form of BEC based on MMC

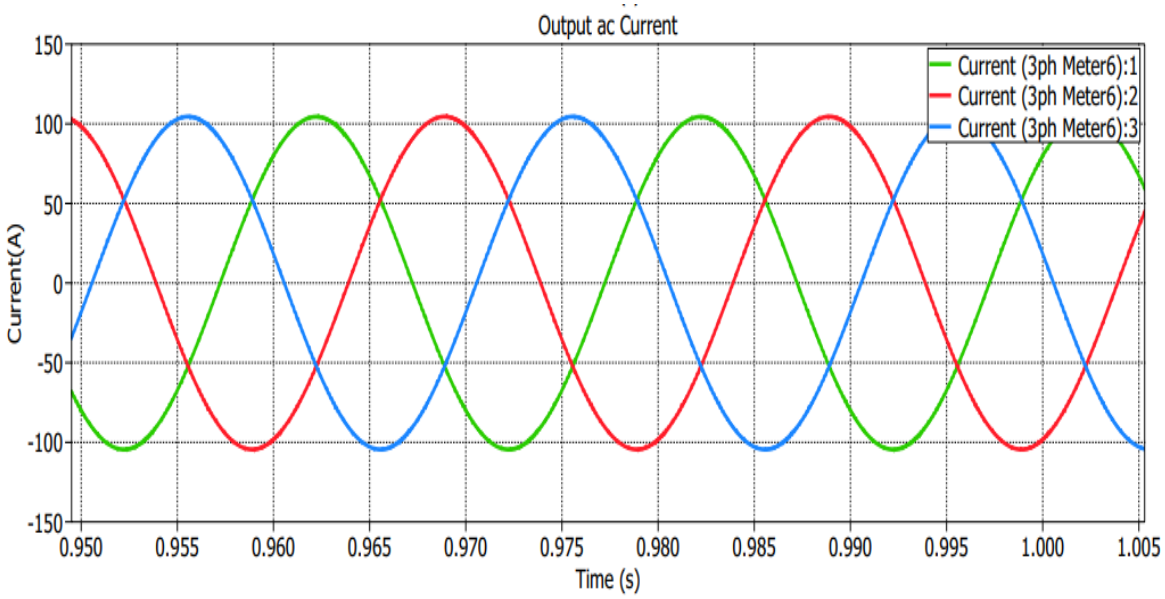


Fig3. 64 Load Current Wave form of BEC based on MMC

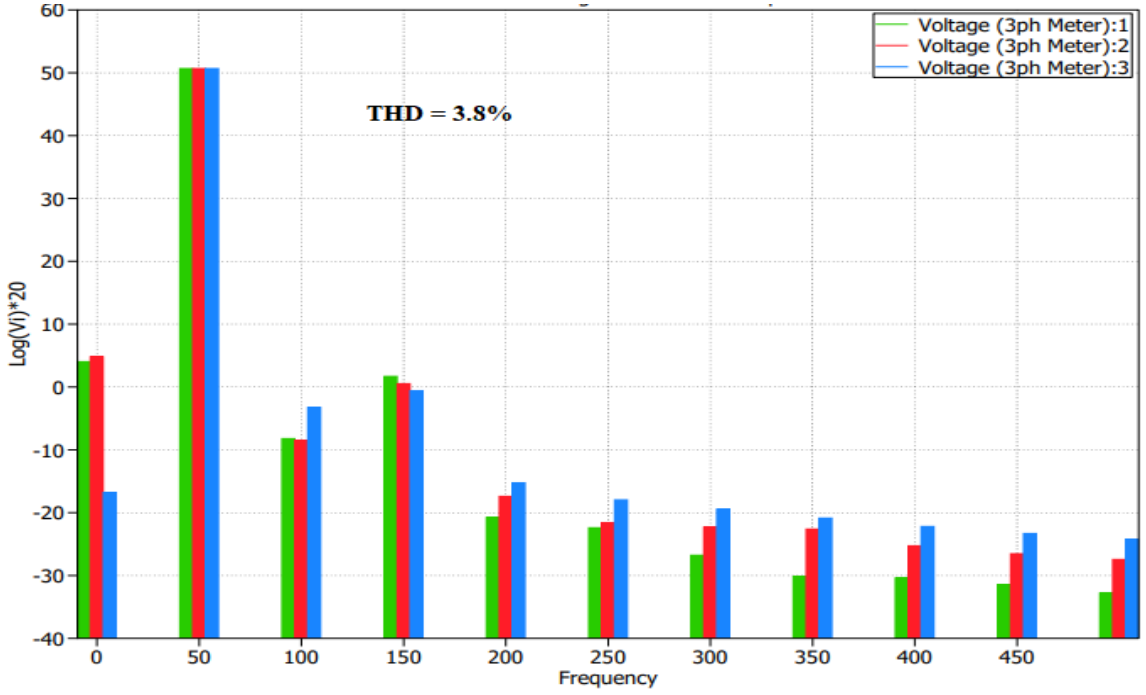


Fig3. 65 Fourier Spectrum of AC voltage of BEC based on MMC

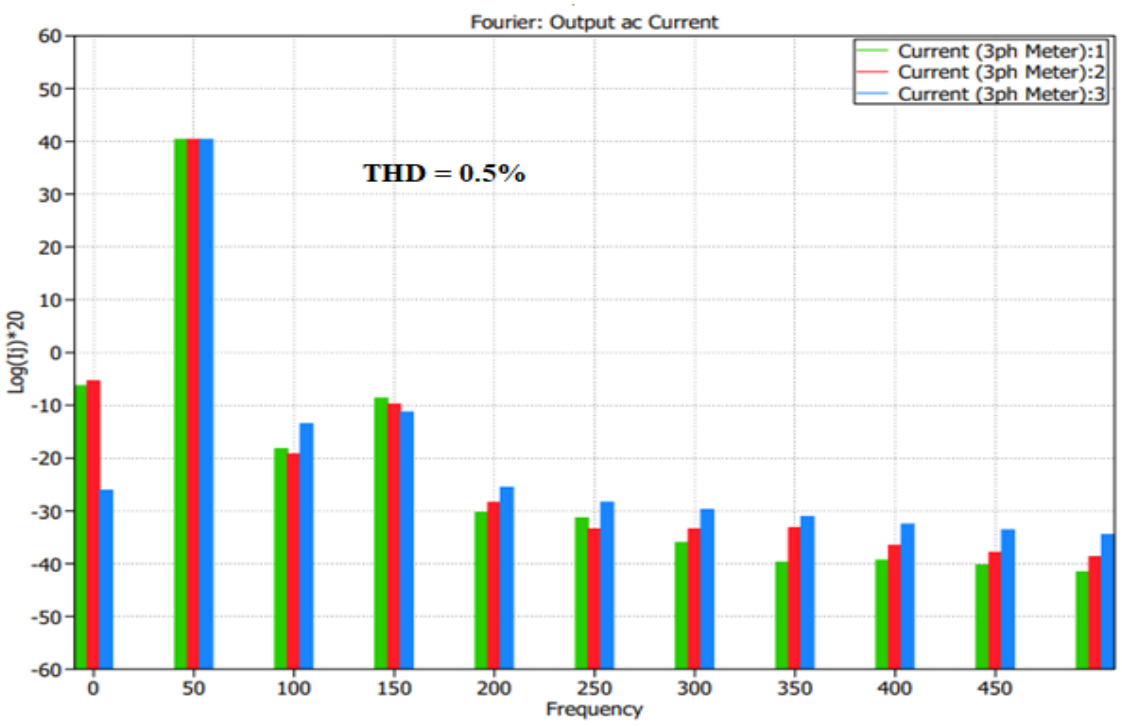


Fig3. 66 Fourier Spectrum of load current of BEC based on MMC

As shown from Fig.3.63 to Fig.3.66, MMC based BEC yields output voltage and current with lower THD values of 3.8% and 0.5% respectively.

C. Efficiency analysis for different SM types

For efficiency analysis, two silicon carbide power MOSFETs are chosen and analysis is done is carried out for MMC converter by using combination of look table and formula for maximum load current and case temperature of 100^0C. All thermal parameters are gathered from device manufacturer's datasheet (https:// www.rhom.com; https://assets.wolfspeed.com). Switching loss, conduction loss and total semiconductor loss of the converter for the selected sub-modules is obtained by using the efficiency calculation model presented in Fig.7. The converter system efficiency as shown in the model is calculated as follows:

$$\eta = \frac{P_{out}}{P_{in}} \qquad (3.54)$$

$$\eta = \frac{P_{in} - P_{loss}}{P_{in}} \qquad (3.55)$$

Dividing the numerator and denominator of equation (21) by P_{in} gives the following expression for efficiency

$$\eta = 1 - \frac{P_{loss}}{P_{in}} \qquad (3.56)$$

Where P_{loss} is total loss in the converter obtained by summing switching and conduction losses, and P_{in} is the input power obtained by product of input DC voltage and current.

The overall losses and efficiency of the MMC based converter is presented in Table.3.7 below.

Table3.7 Semiconductor losses

Device Name	Switching Loss(W)	Conduction Loss (W)	Total Loss (W)	Efficiency (%)
SiC MOSFET (SCT3017AL)	1029.54	818.69	1848.23	96.63
SiC MOSFET (C3M0015065D)	6987.3	390.9	7378.2	86.53

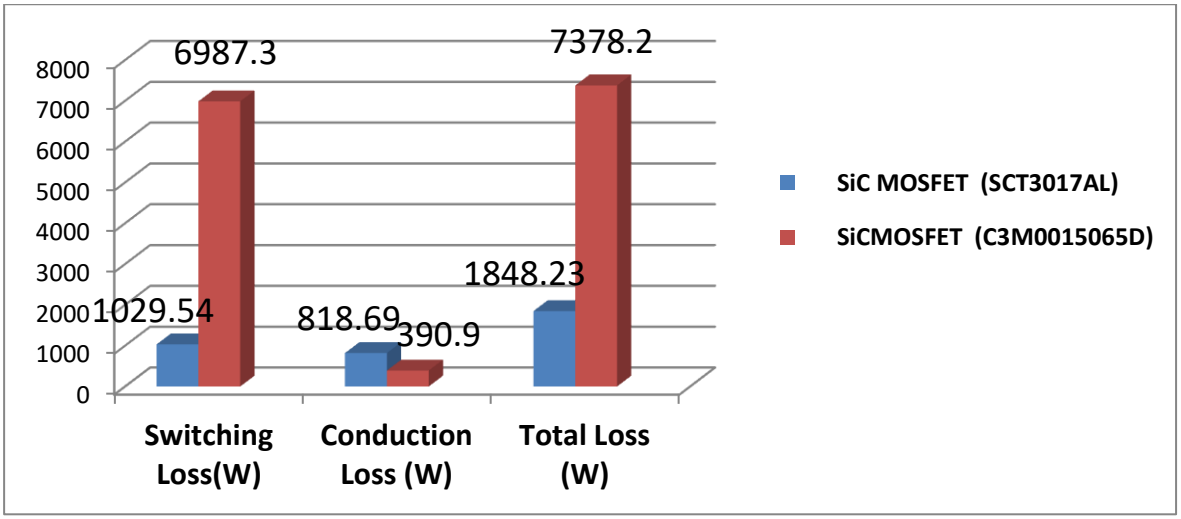


Fig3. 67 Switching and conduction losses

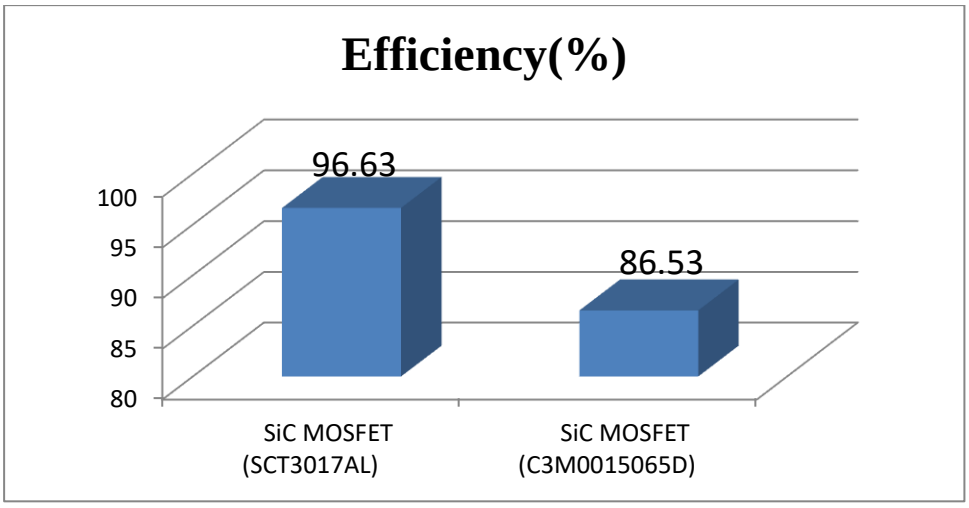


Fig3. 68 System efficiency for different sub-modules

D. Performance comparison of CHB and MMC based modular converter

Table.3.8 shown below describes the comparisons of performance parameters of CHB and MMC based BEC for the same load type(R-L load) and same modulation index, frequency and thermal model of sub-module

Table3.8 Comparative performance analysis

Converter Topology	Voltage THD (%)	Current THD (%)	SM Current Stress (A)	Efficiency (%)
CHB based BEC	13.7	1.6	73	83
MMC based BEC	3.8	0.33	45(61%)	96.63

In comparison with IEEE 519-1992 bench mark, results illustrated in Table.3.8 show that modular converter based on MMC has better and acceptable performance (THD value) than CHB based converter. Moreover, MMC based modular converter has low sub-module (SM) current stress (61% of that in CHB), and as a result, the MMC based converter has better efficiency for the same sub-module type (SCT3017AL).

Summary

This research compares the performance of CHB and MMC-based back end converters (BEC) of smart transformer for 415V, 50Hz distribution network having 50kVA system loads. Four full bridge sub-modules (FBSM) are used to construct CHB based BEC and four half bridge sub-modules (HBSM) per leg arm are used to model an MMC based BEC.

Phase shift PWM with carrier frequencies ranging from 1 kHz to 8 kHz and a modulation index of one (1) to 0.9 was used. Simulation results show that for the same modulation index, load type and number of modules, MMC-based BEC has lower voltage and current THD, higher system efficiency than CHB based BEC. As the carrier frequency goes up, the THD of the current goes down, but the THD of the voltage stays the same. For a decrease in modulation index (Mi), both voltage and current THD must increase. The sub-module in CHB based modular converter is exposed to higher current stress than that in MMC based modular converter. When nonlinear loads, such as rectifiers, are used, current THD increases. The magnitude of grid-side voltage and load current decreases as the modulation index decreases. Semiconductor loss analysis shows that switching loss is greater than conduction loss for both selected switches (Fig. 3.67). From the two chosen power semiconductor switches, the SiC MOSFET (SCT3017AL) has a good efficiency of 96.63% (Fig. 3.68)

CHAPTER FOUR

INTEGRATION OF SMART TRANSFORMER IN TO EXISTING DISTRIBUTION SYSTEM

4.1 Introduction

This chapter deals with integration of smart transformer in to the existing distribution feeder for investigating its ancillary services such as reactive power support, loss minimization, fault ride through capability and reducing harmonic propagation in to nearby loads. The necessary data for simulation such as line data, transformer and load data on Secha feeder are collected from the substation and nameplates and used for load flow analysis.

4.2 Distribution System

Distribution system is a part of power system that links transmission or sub-transmission system with end users or loads. Power distribution is basically carried out on the medium-voltage level, in the range of 6.6–33 kV. Major components of distribution system include the distribution sub-station (secondary substation), primary distribution lines (feeder), secondary distribution lines, distribution transformer, voltage regulating equipment and protection equipment. Critical medium-voltage (MV) distribution substations are connected with two or more incoming supplies from different HV substations. Main distribution substations usually supply power to a clearly defined distribution network such as specific plant or factory, town or city (Jan de Kock ,et'al., 2004). The distribution level voltage is then transformed to low voltage (LV), 110V-120V 60Hz or 220V-240V, 50 Hz, which is used for residential, commercial or industrial loads.

4.3 Primary Distribution Structure

Primary distribution lines emerging from secondary substation is usually carried out by 3-phase 3-wire system with voltage range of 6.6kV to 33kV. For maximum load demand of 8 MVA, primary distribution line is carried out at 66 kV and the number of feeders originating from a secondary substation can be 6-8. Basically, there are 4 different types of primary distribution lines (feeder) layout: These are

i) Radial Distribution Feeder
ii) Parallel Distribution Feeder
iii) Loop Distribution Feeder

iv) Network Distribution Feeder

The radial feeder radiates from a distribution substation only in single direction and branches into sub feeders and laterals which extend into all vicinity of service area.

Distribution transformers (15kV/415V) are connected to the primary feeders, sub feeders and laterals through fuse cut-outs. Because of its simple structure and cost effectiveness, the radial feeder layout is the most commonly used. However, it suffers from a drawback of less availability as there is only one path between the substation and the customers. The radial feeder structure is shown in Fig.4.1 below

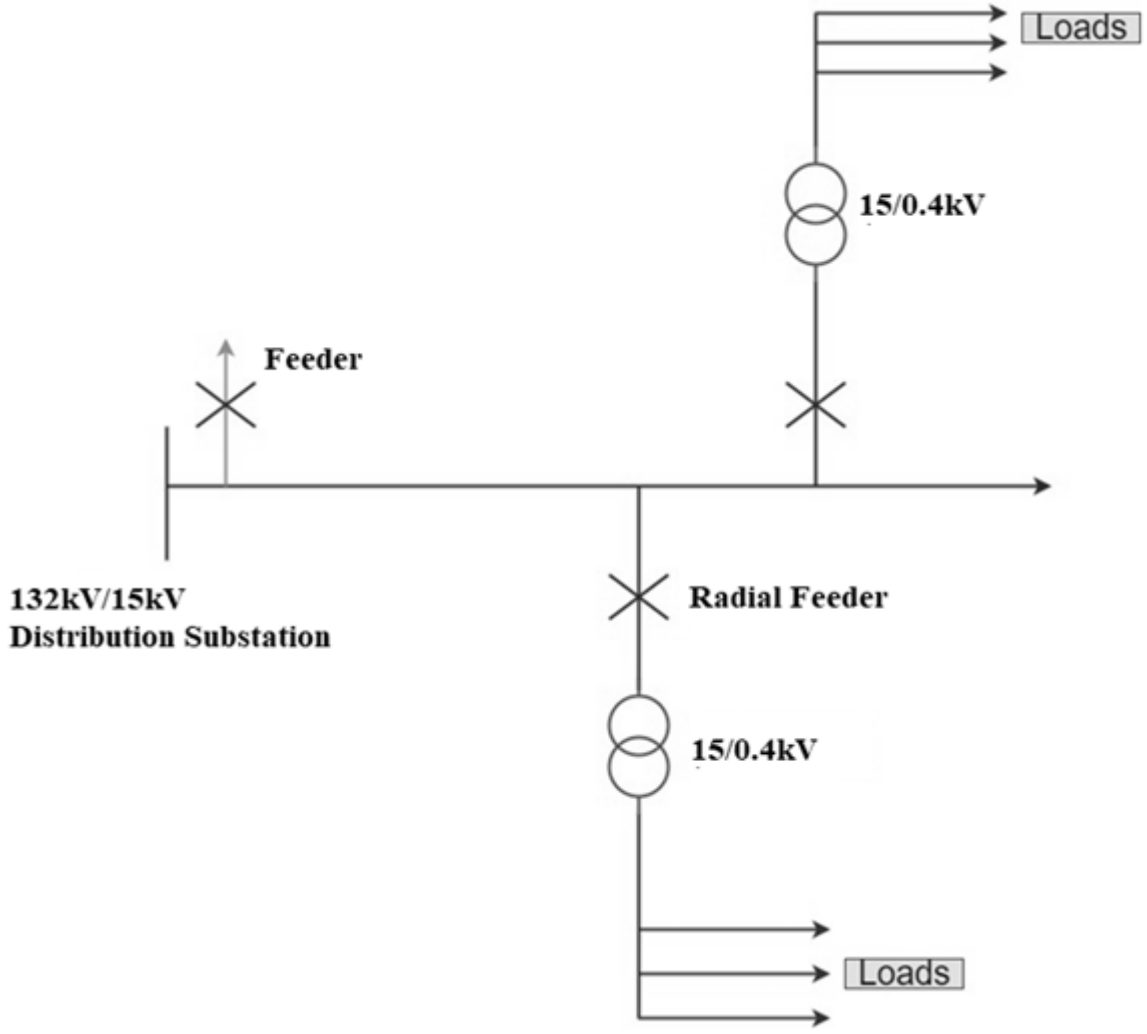


Fig4. 1 Radial feeder layout

The parallel feeder has two radial feeders that originate from the same or different distribution substation. Each feeder supports half of the total load and has capacity to carry full-load of the area during emergency.

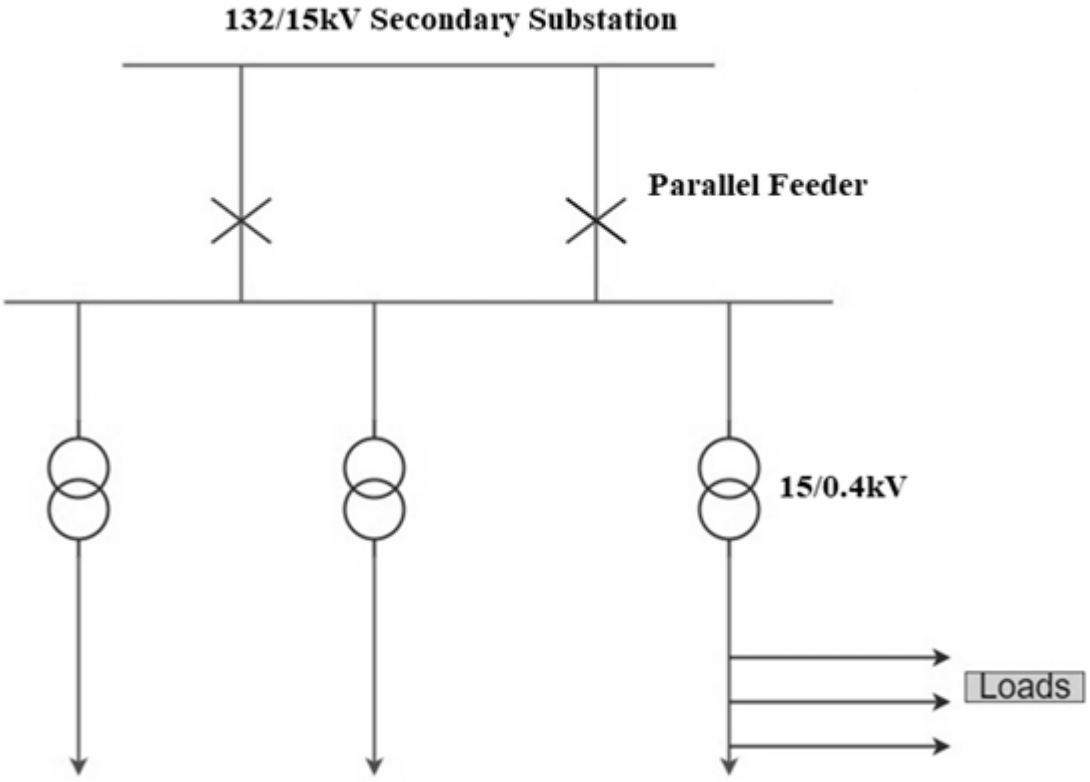


Fig4. 2 Parallel Feeder layout

The parallel feeder has benefits of improved reliability although it is expensive than radial feeder and employed when the supply continuity is of greater importance.

The loop system consists of two or more radial feeders originating from the same or different secondary substations. It has two paths between substation(s) and loads.

This kind of feeder is the most reliable for supply continuity and gives better voltage regulation and higher efficiency. Moreover, feeders and loop components have sufficient reserve capacity to serve the load. However, it is slightly more sophisticated than a radial system and needs higher cost.

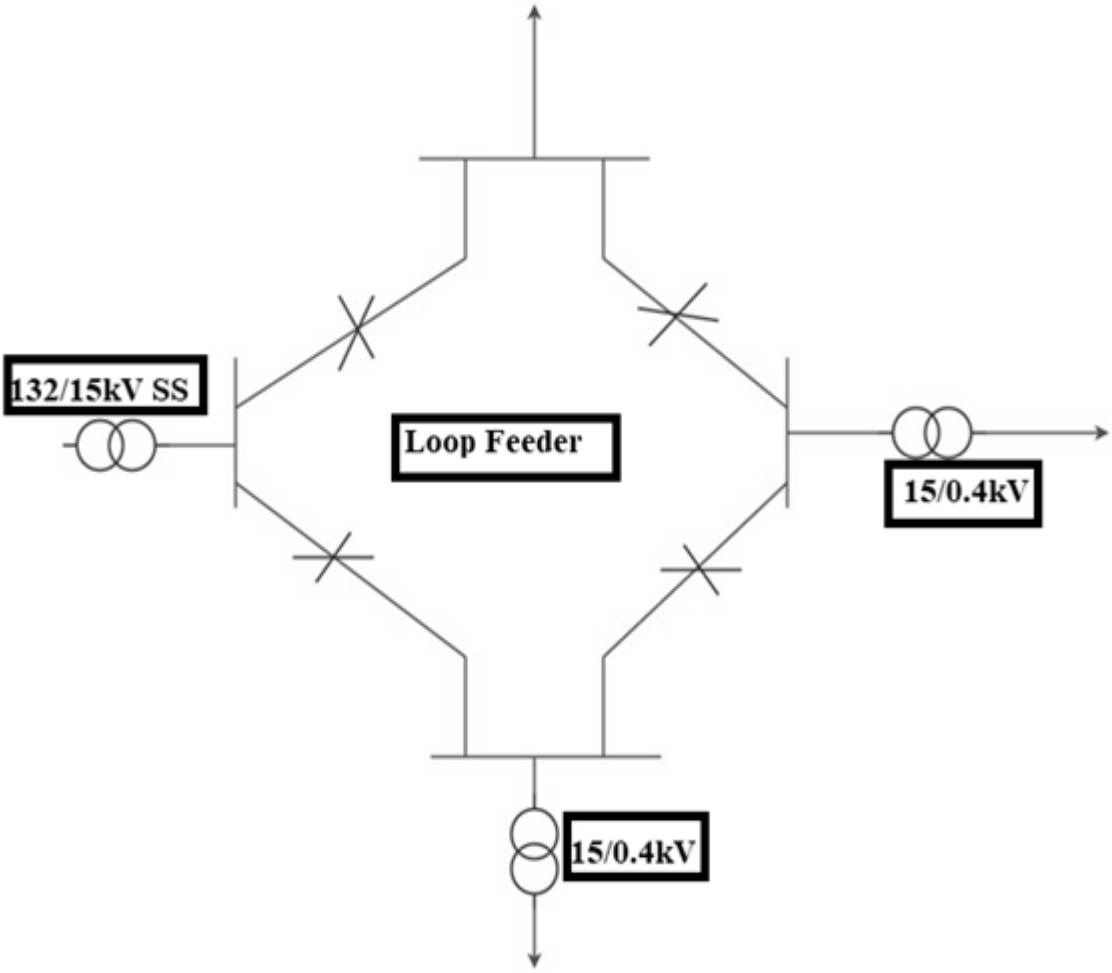


Fig4. 3 Loop system layout

In the network layout, energization of feeder ring-main from two or more than two generating stations or substations is needed. As a result power supply to all distribution transformers is possible even though a part of network may be out of service.

This kind of layout provides the better reliability and flexibility lest it is much more sophisticated than other forms of feeder layout. It is used in large metropolitan cities where continuity of supply is the most important.

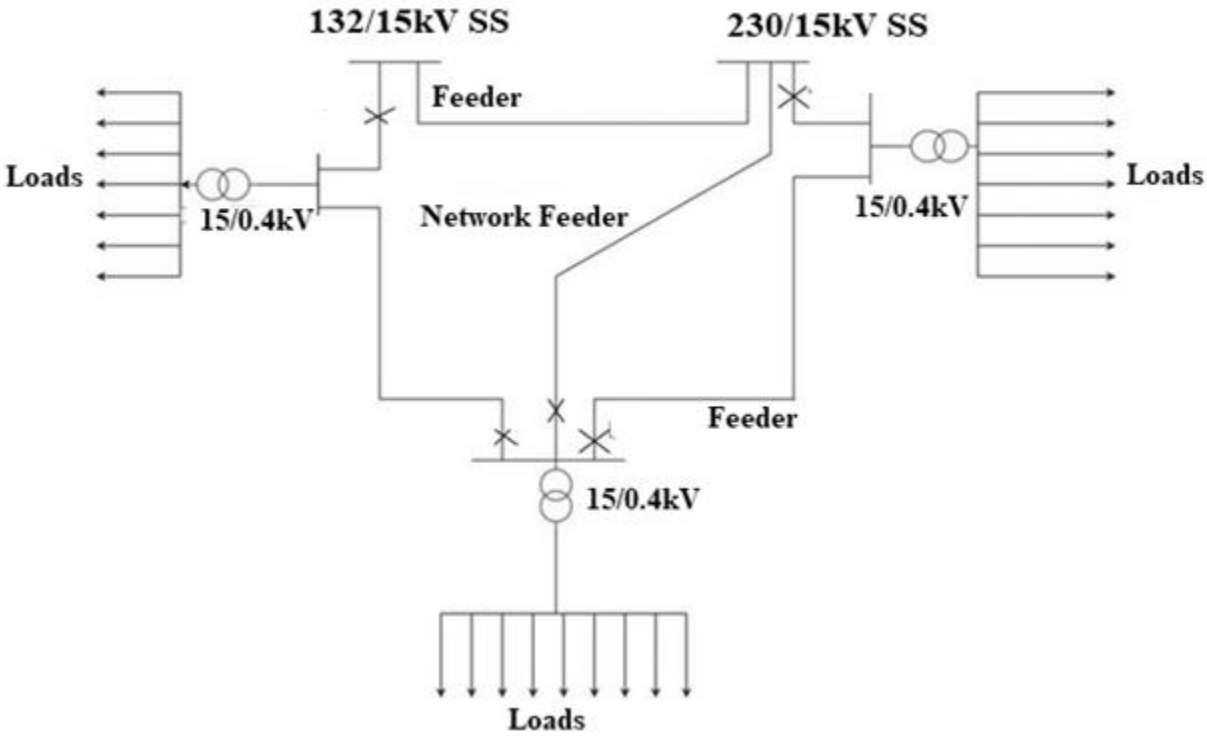


Fig4. 4 Network Feeder layout

4.4 Distribution line parameters and Modeling

Overhead distribution lines consist of series and shunt elements. The series elements are resistance and inductive reactance whereas the shunt elements are made of capacitive reactance and admittance. Since the distribution lines under study are of short length, effect of capacitance can be neglected and the line is only represented by its series element. In this research work, overhead lines are represented with their series resistance and inductive reactance and a balanced three phase system is assumed for modeling as shown below

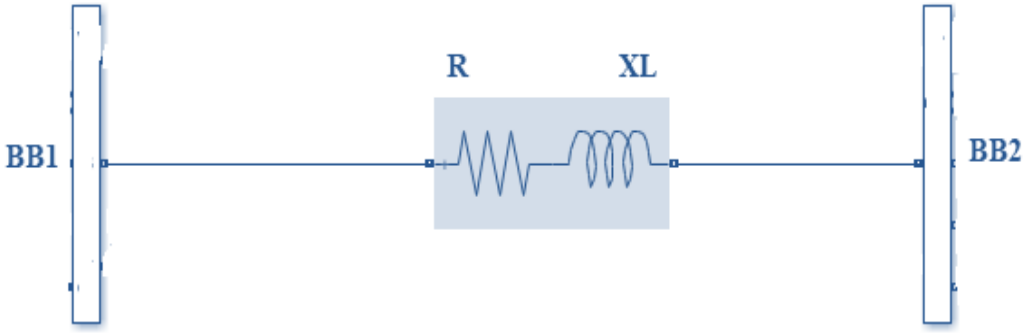


Fig4. 5 Distribution line model

4.4.1 Impedance calculation of overhead distribution Line

The unit inductance of overhead distribution line depends upon the material dimensions such as conductor diameter, strands and distance between conductors which in turn depend on its configuration such as horizontal flat, vertical flat, symmetrical and un-symmetrical arrangements. The AC resistance of a conductor is always higher than its DC resistance because the skin effects forcing more current flow near the outer surface of the conductor. The higher the frequency of the current, the more noticeable skin effect would be. Wire manufacturers usually supply tables of resistance per unit length at common frequencies (50Hz or 60Hz) to determine the total resistance from such tables. The conductor type used in the Secha feeder is All Aluminum Conductor (AAC) having overall area of 95 square mm and 50 square mm. The physical data of the standard bare All Aluminum Conductors (AAC) used in distribution construction as presented in (UNDP-ENRP, 2022) are given in Table 4.1.

Table4. 1 Basic Physical data of the standard bare All Aluminum Conductor (AAC)

Name of Conductor Parameter	**Conductor Type**	
	AAC95	AAC50
Nominal size (mm^2)	95	50
Mean cross section (mm^2)	93.27	49.48
Stranding (No / mm)	19/2.5	7/3.0
Overall diameter (mm)	12.5	9.0
Actual diameter (mm)	10.8975	7.9377
Modules of elasticity (kN/mm^2)	57	60
Ultimate tensile Strength (kN)	15.68	7.94
Conductor resistance at 20^0C (ohm/km)	0.3095	0.5786
Maximum Current Rating, at 35^0C (Amps)	324	219
Maximum Current Rating, at 50^0C (Amps)	245	168

If a balanced three-phase system ($I_A + I_B + I_C = 0$) is considered, the flux linkage of each conductor per unit length is given as

$$\lambda_A = \frac{\mu_o}{2\pi}\left[I_A * ln\left(\frac{Dm}{GMR_a}\right)\right] Wb/m \qquad (4.1)$$

where, $\mu_o = 4\pi*10^{-7}$H/m, Dm refers to geometric mean distance between conductors and GMR_a is geometric mean radius of conductor obtained as follows

$$Dm = \sqrt[3]{D_{ab} * D_{bc} * D_{ac}} \qquad (4.2)$$

Where, D_{ab}: Distance between conductors a and b in meter,

D_{bc}: Distance between conductor's b and c in meter and

D_{ac}: Distance between conductors a and c in meter

$$GMR_a = \sqrt[n^2]{\prod_{i=1}^{n}\prod_{j=1}^{n} D_{ij}} \qquad (4.3)$$

Where, n represents number of strands and the factor D_{ij} represents distance between strand conductor" i" and strand conductor" j"

Equation (4.3) can be put in more simple form as

$$GMR_a = K * r \qquad (4.4)$$

Where r represents conductor radius and K represents geometric mean radius factor obtained from the following table.

Table4. 2 Geometric mean radius factor for different strands

No of Strands	**GMR factor, k**
1	0.7788
3	0.6778
7	0.7256
19	0.7577
37	0.7678
61	0.7722

The GMR value for all three conductors is assumed to be same but the actual geometric mean distance of the feeder is obtained from the Ethiopian Electric utility (EEU) distribution engineer. The lines have horizontal flat configuration having minimum spacing between each of the three phases is given as:

- D_{ab}: Distance between conductors a and b: 0.64m
- D_{bc}: Distance between conductors b and c: 0.51m
- D_{ac}: Distance between conductors a and c: 1.15m

Using the above data, per phase inductance can be obtained as (J. D. Glover,et'al.,2017)

$$L = \frac{\mu_o}{2\pi} ln\left(\frac{D_m}{GMR_a}\right) H/m \qquad (4.5)$$

The inductive reactance per unit length is obtained as

$$X_L = 2\pi f * L = \mu_o f * ln\left(\frac{D_m}{GMR_a}\right) \Omega/m \qquad (4.6)$$

For expression of ohm per km,

$$X_L = 0.6283 * ln\left(\frac{D_m}{GMR}\right) \Omega/km \qquad (4.7)$$

The feeder inductive reactance for a given conductor length and frequency f = 50Hz is calculated using equation (4.7)

Since impedance is sum of resistance and reactance of the line, the line resistance per unit length for a specified conductor type is obtained from the following relations or from manufacturer's data (Appendix-C)

The AC resistance of a conductor in a distribution line is based on the calculation of its DC resistance. If DC current is flowing along a round cylindrical conductor, the current is uniformly distributed over its cross-section area and its DC resistance is evaluated by:

$$R_{DC} = \rho\left(\frac{l}{A}\right) \Omega/m \qquad (4.8)$$

where ρ is conductor resistivity at a given temperature (Ω -m) , ℓ is conductor length (m) and A is conductor cross-section area (m2)

However, the frequency of the AC voltage produces a non-uniform distribution of the current on the conductor, a phenomenon known as skin effect. As frequency increases, the current tends to go toward the surface of the conductor and the current density decreases at the center. Skin effect reduces the effective cross-section area used by the current, and thus, the effective resistance increases. Also, although in small amount, a further resistance increase occurs when other current-carrying conductors are present in the immediate vicinity due to proximity effect. At small frequency, skin and proximity effects can be neglected without loss of accuracy.

Other variations on the resistance of conductor is caused by temperature and bundling The resistivity of any conductive material varies linearly over an operating temperature, and therefore, the resistance of any conductor suffers the same variations. As temperature rises, the conductor resistance increases linearly, over normal operating temperatures, according to the following equation:

$$R_2 = R_2 \left(\frac{T + t2}{T + t1}\right) \Omega/m \qquad (4.9)$$

Where, R2 is resistance at second temperature t2, R1 is resistance at initial temperature t1 and T is temperature coefficient for the particular material (^{0}C)

Resistivity (ρ) and temperature coefficient (T) constants depend upon the particular conductor material and for Aluminum conductor it is given in Table 4.3 below (Manuel Reta-Herna´ndez, 2012).

Table4. 3 Resistivity and temperature coefficient of Aluminum

Material	Resistivity at 20^{0}C (Ω-m)	Temperature Coefficient(/^{0}C)
Aluminum	2.83* 10^{-8}	228.1

Based on the above information, the resistances of conductor at 50^{0}C for All Aluminum Conductor (AAC50 and AAC95) conductors are obtained as 0.63Ω/km and 0.35Ω/km respectively.

The conductor impedance is now computed by using the following equation:

$$Z_a = R_a + j0.06283 ln \frac{Dm}{GMR_a} \Omega/km \qquad (4.10)$$

$$\boldsymbol{Dm} = \sqrt[3]{D_{ab} * D_{bc} * D_{ac}} = \sqrt[3]{0.64 * 0.51 * 1.15} = \mathbf{0.72135m}$$

- **For AAC-95 conductor type**

For the AAC-95 type conductors, the number of strands is 19 with its k-value of 0.7577 having actual radius, r of 5.4487mm (Table 4.1). Thus, its GMR is calculated as:

$$\text{GMR}_{95} = 0.7577 * 5.4487\text{mm} = 4.129\text{mm} = 4.129 * 10^{-3}\text{m}$$

The self-impedance for AAC-95 type phase conductors is then calculated at temperature of 50 ^{0}C as:

$$Z_a = R_a + j0.06283\ln\frac{D}{GMR_a}\Omega/km$$

$$Z_a = 0.35 + j0.06283\ln\frac{0.72135}{4.129 * 10^{-3}}\Omega/km$$

$$Z_a = 0.35 + j0.32441\Omega/km$$

Then total impedance of the conductors is obtained by multiplying the unit impedance by its length.

- **For AAC-50 conductor type**

For the AAC-50 type conductors, the number of strands is 7 with its k-value of 0.7256 having actual radius, r of 3.9688mm (Table4.1). Thus, its GMR is calculated as:

$$GMR_{50} = 0.7256 * 3.9688mm = 2.88mm = 2.88 * 10^{-3}m$$

The self-impedance for AAC-50 type phase conductors is then calculated as:

$$Z_a = R_a + j0.06283\ln\frac{D}{GMR_a}\Omega/km$$

$$Z_a = 0.63 + j0.06283\ln\frac{0.72135}{2.88 * 10^{-3}}\Omega/km$$

$$Z_a = 0.63 + j0.34702\Omega/km$$

Table4. 4 AAC conductor parameters of the feeder

$A_{nominal}$ (mm^2)	A_{actual} (mm^2)	D_{strnd} (mm)	$D_{over\ all}$ (mm)	$D_{acttual}$ (mm)	GMR (mm)	R (Ω/km)	X (Ω/km)
50	49.5	7/3.0	9	7.9377	2.88	0.63	0.34702
95	93.5	19/2.5	12.5	10.8975	4.129	0.3085	0.324

Table4. 5 Secha main feeder data

Bus			Conductor				Transformer capacity and Load		
No	**From**	**To**	**Type**	**R(ohm)/km**	**X(ohm)/km**	**L(km)**	Equivalent Installed Capacity (MVA)	Actual (MW)	Actual (MVar)
1	SS	P1	AAC95	0.34702	0.324	3.5	3.18	1..46	1.1
2	P1	P2	AAC50	0.63	0.3470	0.8	3.5	1.65	1.2
3	P2	P3	AAC50	0.63	0.3470	0.9	2.5	1.65	1.2
4	P3	P4	AAC50	0.63	0.3470	1	3.8	1.65	1.2
5	P4	P5	AAC50	0.63	0.3470	0.5	2.9.	1.65	1.2
6	P6	P7	AAC50	0.63	0.3470	0.4	3.2	1.65	1.2
7	P7	P8	AAC50	0.63	0.3470	0.4	0.2	0.15	0.05
8	P7	P9	AAC50	0.63	0.3470	0.2	0.05	0.048	0.02
Total						**7.7**	**19.330**	**7.957**	**5.967**

4.4.2 Distribution line performance

Determination of voltage drop, line losses and efficiency of transmission are important considerations in the design and operation of a distribution line. Line constants such as R, L and C greatly influence the performance values of the distribution system. For instance, the voltage drop in the line depends upon the values of above three line constants. Similarly, the resistance of distribution line conductors is the most important cause of power loss in the line and determines the transmission efficiency. Distribution lines are short and operate at small voltage (up to 33kV) and hence capacitance effect is neglected for calculations. Therefore, while studying the performance of a distribution line, only resistance and inductance of the line are taken into account as shown in Fig4.6 below

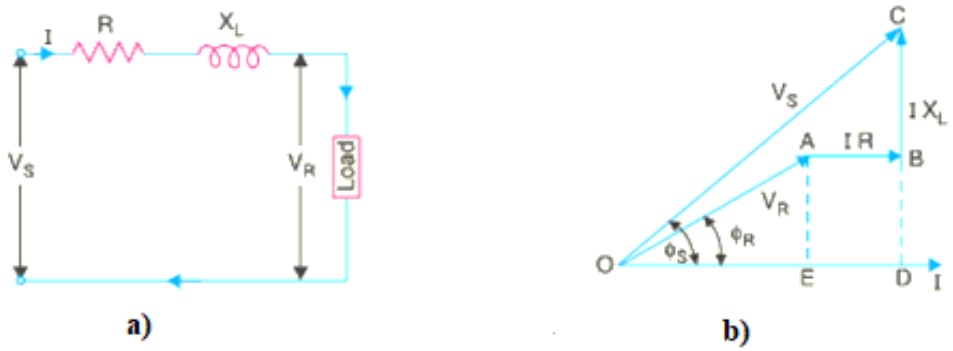


Fig4. 6 Single phase representation distribution line and its phasor diagram

Voltage regulation: When a distribution line is carrying current, there is a voltage drop in the line due to resistance and inductance of the line. The result is that receiving end voltage (V_R) of the line is generally less than the sending end voltage (V_S). This voltage drop ($V_S - V_R$) in the line is expressed as a percentage of receiving end voltage V_R and is said to be voltage regulation (V.R).

.

$$\%\text{age V.R} = \frac{(\text{VS} - \text{VR})}{\text{VR}} * 100 \qquad (4.11)$$

Looking at the phasor diagram given in Fig4.6 (b), the voltage regulation is dependable on load power factor. By using load power factor, the sending end voltage can be obtained by using the following method:

Let

I = load current

R = loop resistance i.e., resistance of both conductors

X_L = loop reactance

V_R = receiving end voltage

Cos Φ_R = receiving end power factor (lagging)

V_S = sending end voltage

cos Φ_S = sending end power factor

Then taking Triangle ΔODC gives the following relation:

$$\begin{aligned}(OC)^2 &= (OD)^2 + (DC)^2 \\ V_S^2 &= (OE + ED)^2 + (DB + BC)^2 \\ &= (V_R \cos\phi_R + IR)^2 + (V_R \sin\phi_R + IX_L)^2 \\ V_S &= \sqrt{(V_R \cos\phi_R + IR)^2 + (V_R \sin\phi_R + IX_L)^2}\end{aligned}$$

Distribution efficiency: Distribution efficiency is a measure of power sent out to the line and power delivered to the loads. The three phase power delivered the load is given by the following equation:

$$P_{\text{delivered}} = \sqrt{3}V_R * I * \cos\theta_R \qquad (4.12)$$

Power loss in the distribution lines due to the resistance when load current "I" flows through it is given by:

$$P_{Loss} = \quad 3 * I^2 * R \qquad (4.13)$$

Distribution efficiency is then given by

$$\text{Distribution Efficiency} = \left(\frac{Power\ Delivered}{Power\ Sent\ out}\right) * 100 \qquad (4.14)$$

$$\text{Distribution Efficiency} = \left(\frac{\sqrt{3}V_R * I * \cos\theta_R}{\sqrt{3}V_R * I * \cos\theta_R + 3 * I^2 * R}\right) * 100 \qquad (4.15)$$

4.5 Transformer modeling

Transformer is one of the essential devices in electrical AC power distribution system, which is used to transform medium level AC voltage magnitudes to low voltage (LV) magnitude for consumption. Like single phase transformer, the three-phase transformer also has primary and secondary windings, but the windings of each phase are separately wound and brought out for both primary and secondary with the primary terminals connected to the three-phase source. The most common arrangement of three windings of the primary and secondary sides is either star or delta with 120^0 phase displacement between each phase. Depending on the winding connection and phase relationship between high and low voltage sides, three phase transformer might be classified in to four groups: These are

i) Group number-I which means the phase difference between HV and LV windings is 0^0. Transformer with this group number can be labeled as Yy0 o or Dd0

ii) Group number -II which means the LV winding phases lag the HV winding phases by 180^0. Transformer with this group number can be labeled as Yd6 o or Dy6

iii) Group number-III which means the LV winding phases lag the HV winding phases by 30^0. Transformer with this group number can be labeled as Yd1 o or Dy1

iv) Group number-IV which means the LV winding phases lag the HV winding phases by 330^0 or leads by 30^0. Transformer with this group number can be labeled as Yd11 o or Dy11

Only transformers having the same group number, same %Z, same polarity, same voltage ratio and same phase sequence can be connected in parallel to share loads (Jan de Kock,et'al., 2004).

Power is dissipated in transformer when the magnetizing current passes through the core in the form of alternating cycles of flux, the cycles being determined by the system frequency. The loss dissipated in an open circuited transformer is referred to as the core loss or no-load loss (also referred as iron loss). The iron loss is always constant since it is dissipated whether a load is connected across the secondary winding or not. When a load is connected across the secondary terminal, the flow of load current in the secondary winding produces an equivalent increase in the primary load current and the mmf it produces. As a fundamental phenomenon, transformer windings also dissipate losses when currents flow in the windings with secondary winding being connected to a load, termed as load loss or copper loss. The magnitude of these losses in the primary and secondary windings depends upon the magnitude of the current and the resistance of the total system.

For any transformer, it is not practically possible to ensure that all of the flux produced by the primary winding source is linked to the secondary winding. Due to limitations in the materials used and in the design of transformer cores some flux 'leaks' out of the core and flows through the air and is termed leakage flux. It is convention to allocate half the leakage flux to both the windings, as it is difficult to quantify exactly the leakage flux contribution to the primary and the secondary windings. So the transformer can be said to possess leakage reactance due to imperfect transformation between primary and secondary windings. Practically this is expressed as transformer impedance, since transformer windings also have resistance and this impedance is normally expressed as a percentage voltage drop in the transformer at full load current.

The percentage voltage drop or impedance of transformer (Z%) is the obtained by short-circuiting the secondary side of transformer and increasing the primary voltage till the full load primary current flows through the winding expressed mathematically as shown below:

$$\%Z = \left(\frac{I_{FL} * Z}{E}\right) * 100 \qquad (4.16)$$

Where I_{FL} is full load current either primary or secondary, Z is transformer impedance obtained as vector sum of resistance (R) and leakage reactance (X) and E is the open circuit voltage.

Typical percentage impedance values for a medium-sized power transformer are about 9–10% though some may have higher values up to 22.5%.

Voltage regulation: The voltage regulation of a transformer is defined as the change in magnitude of terminal voltage or secondary voltage, when full load of specified power factor supplied, with primary voltage and frequency held constant, expressed as percentage of the rated terminal voltage.

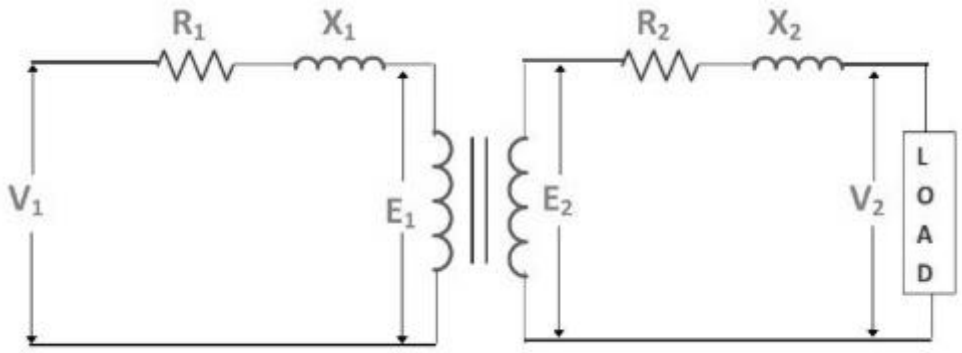


Fig4. 7 Transformer at loading condition

Based on the fig.4.6, voltage regulation is expressed as follows:

$$\text{Voltage Regulation} = \left(\frac{E_2 - V_2}{V_2}\right) * 100 \qquad (4.17)$$

For a lagging and leading power factor, the voltage regulation can be derived from the phasor diagram of E_2, V_2, and drop across resistance and reactance with V_2 selected as reference as shown below:

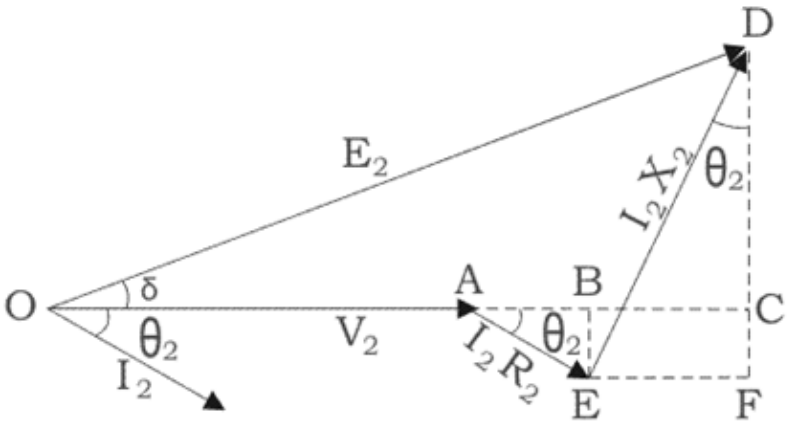


Fig4. 8 Phasor diagram of transformer for lagging power factor

From the above diagram, the following relations can be derived:

$$OA = V_2$$

From $\Delta\ ABE$

$$AB = AE\cos\theta_2$$

$$= I_2R_2\cos\theta_2$$

From ΔDEF

$$BC = DE\sin\theta_2 \quad = I_2X_2\sin\theta_2 \quad [BC = EF]$$

Angle between OC and OD may be small, so it can be neglected and $OD \cong OC$

$$OC = OA + AB + BC$$

$$E_2 = OC = OA + AB + BC$$

$$E_2 = OC = V_2 + I_2R_2\cos\theta_2 + I_2X_2\sin\theta_2$$

$$\text{Voltage regulation } (V.R) = \frac{E_2 - V_2}{V_2} * 100\%$$

$$\text{Voltage regulation } (V.R) = \frac{I_2R_2\cos\theta_2 + I_2X_2\sin\theta_2}{V_2} * 100\%$$

If the load power factor is leading, the expression for voltage regulation changes and can be derived from the following phasor diagram:

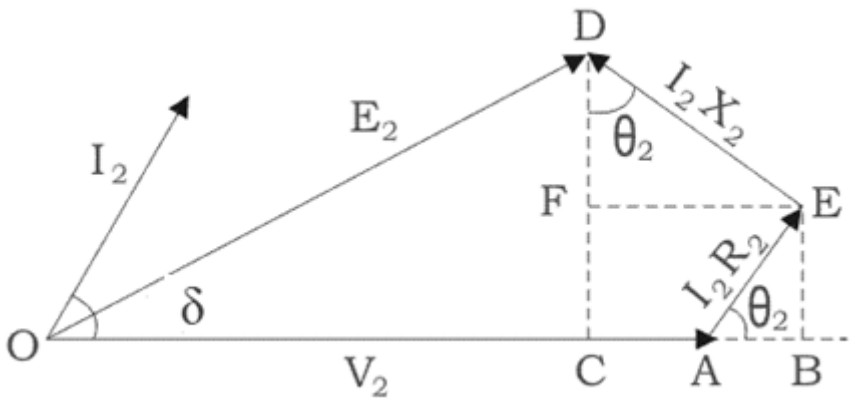


Fig4. 9 Phasor diagram of transformer for leading power factor

From the Fig.4.9 the following relations can be derived with the assumption that angle between E_2 and V_2 is small and neglected (OD≅OC)

$$OA = V_2$$

From Δ *ABE*

$$AB = AE\cos\theta_2$$

$$= I_2R_2\cos\theta_2$$

From Δ *DEF*

$$BC = DE\sin\theta_2 \quad = I_2X_2\sin\theta_2 \quad [BC = EF]$$

$$OC = OA + AB + BC$$

$$E_2 = OC = OA + AB + BC$$

$$E_2 = OC = V_2 + I_2R_2\cos\theta_2 + I_2X_2\sin\theta_2$$

$$\text{Voltage regulation } (V.R) = \frac{E_2 - V_2}{V_2} * 100\%$$

$$\text{Voltage regulation } (V.R) = \frac{I_2R_2\cos\theta_2 + I_2X_2\sin\theta_2}{V_2} * 100\%$$

Distribution transformer is modeled by its primary and secondary windings connected in either delta-star or star-star., shunt elements (R_M and L_M) and percentage impedance (Z%) as shown in Fig.4.9 below.

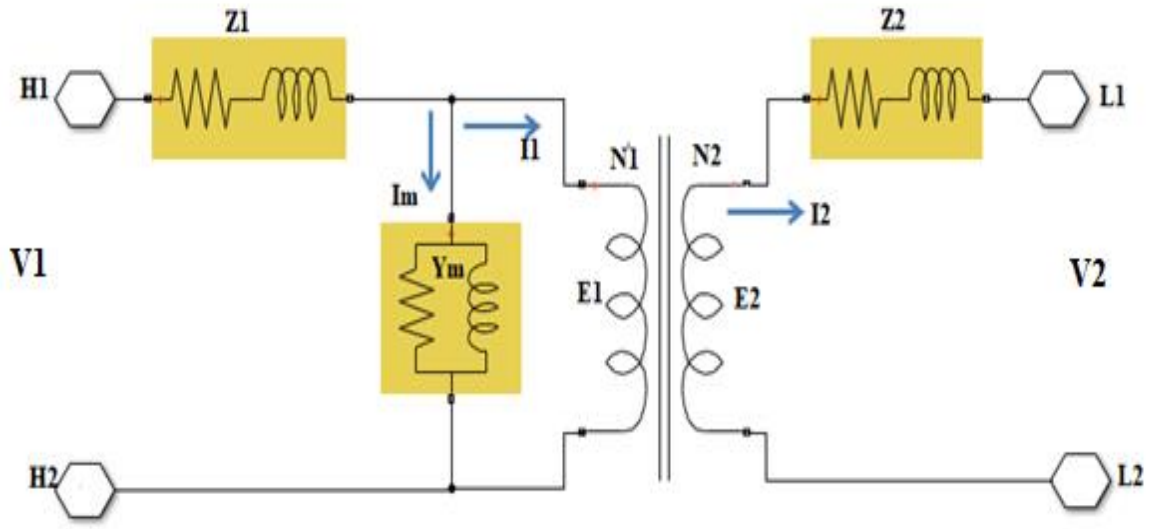


Fig4. 10 Equivalent model of transformer

The capacity of transformer is expressed in kVA or MVA which indicates the maximum apparent power the transformer can be loaded.

There are 72 distribution transformers connected with Secha feeder having the total installed capacity of 19.330MVA. However, the peak demand measured from the load points in the feeder are found as about 7.95708MW and 5.9679MVAr respectively.

The feeder under study consists of various distribution transformers ranging from 25kVA to 1250kVA as shown in Table 4.6 below.

Table4.6 Installed capacity of distribution transformer on Secha feeder

S/n	MVA Rating	Quantity	Total Installed MVA
1	0.025	2	0.05
2	0.05	14	0.70
3	0.10	5	0.50
4	0.20	19	3.80
5	0.315	22	6.93
6	0.40	1	0.40
7	0.50	1	0.50
8	0.630	5	3.15
9	0.80	1	0.80
10	1.250	2	2.50
Grand Total		72	19.33

All distribution transformers in the feeder under study are grouped in to eight (8) equivalent transformers based on their geographical location. The equivalent transformers are formed by arithmetic sum of all distribution transformers in that area. The simplified Secha feeder containing equivalent transformers is shown below in Fig. 4.7

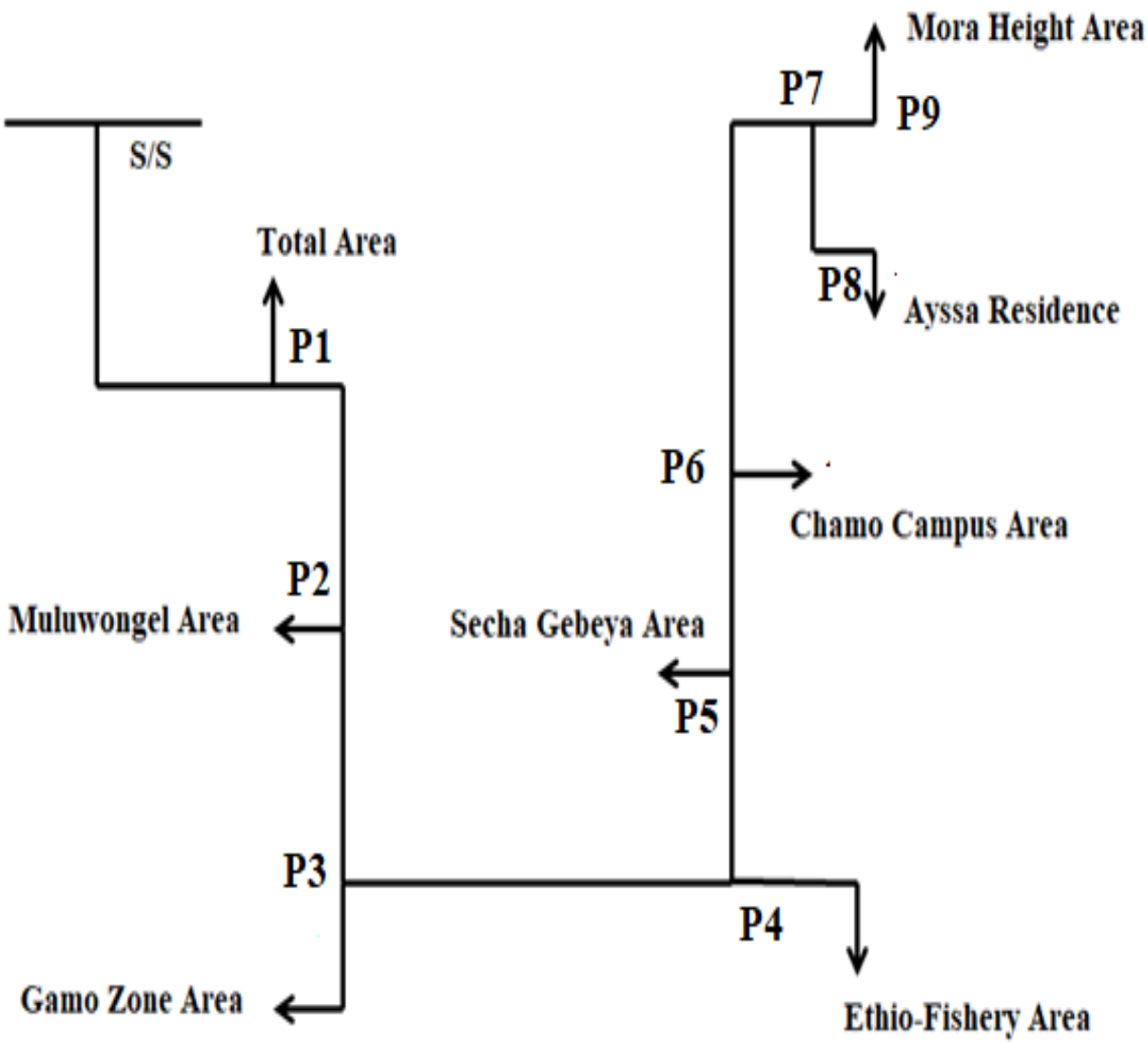


Fig4. 11 A Simplified Secha feeder layout

The points P1 to P9 in the above Fig.4.3 show the nodes from which branch networks are taken. Load flow analysis without ST application and with integration of ST at Point-8 in the feeder diagram is done for peak load condition in this section. Evaluation of changes in the performance of the feeder such as voltage profile, power loss, reactive power flow and harmonics propagation are analysed.

4.6 Simulation result without ST integration for peak loading Condition

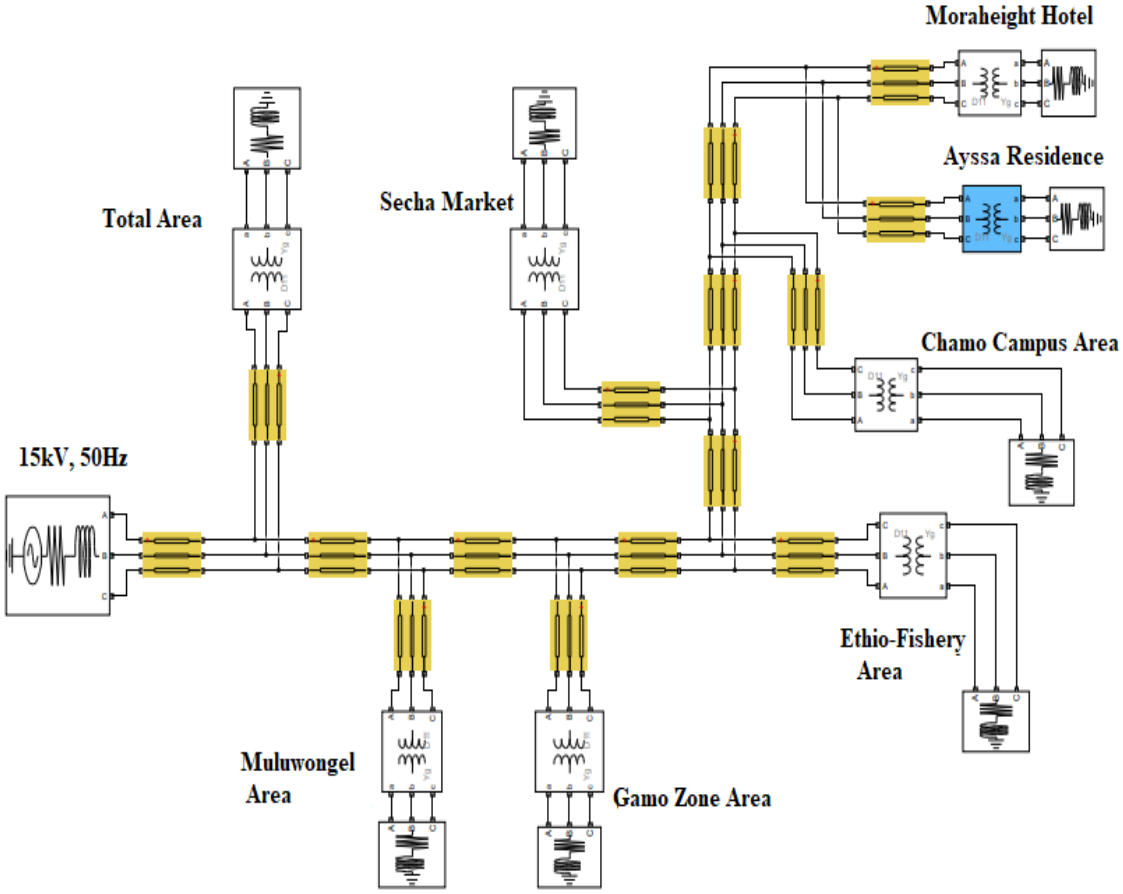


Fig4. 12 Matlab/Simulink model of Secha feeder

A. Main feeder power flow data

Table4.7 Current and power loss data

Current		Resistance		Loss(kW)-1phase	3phase loss (kW)
Branch current	Value	Resistance name	Value		
I1	433	R1	1.2	224.9868	674.9604
I2	365	R2	0.5	66.6125	199.8375
I3	291	R3	0.5	42.3405	127.0215
I4	218	R4	0.5	23.762	71.286
I5	149	R5	0.3	6.6603	19.9809
I6	77.8	R6	0.2	1.210568	3.631704
I7	7	R8	0.15	0.00735	0.02205
I8	2	R8	0.1	0.0004	0.0012
Total				365.580418	1096.741254

Remark: Based on the result in Table4.7, the power loss in the main feeder at peak load condition is about 1.1MW

Table4.8 Node voltage magnitudes

Bus name	Nominal node-voltage	Actual bus voltage(V)	V(pu)
P1	8660	8464	0.97736721
P2	8660	8248	0.95242494
P3	8660	8075	0.93244804
P4	8660	7948	0.91778291
P5	8660	7901	0.91235566
P6	8660	7880	0.90993072
P7	8660	7879	0.90981524

Remark: Based on the result in Table 4.8, nodes P4 to P7 experience low per unit voltage during peak loading

Table4. 9 Reactive power flow

Reactive power flow (MVAr)			Remark
From node	To node	Value(MVAr)	Total MVAr requirement for loads, transformers and line charging
SS	P1	6.9	

Remark: The total reactive power flow in the feeder is about 6.9MVAr, which is required for loads, transformers and line charging.

4.7 Simulation result with ST integration at Point-8 in the feeder

Table4. 10 Current and power loss data with ST applied

Current		Resistance		Loss(kW)-1-phase	3phase loss(kW)	Saving (kW)
Branch current	Value(A)	Resistance name	Value(Ω)			
I1	378	R1	1.2	171.4608	514.3824	
I2	316.4	R2	0.5	50.05448	150.16344	
I3	250.3	R3	0.5	31.325045	93.975135	
I4	137.2	R4	0.5	9.41192	28.23576	
I5	114.5	R5	0.3	3.933075	11.799225	
I6	135.3	R6	0.2	3.661218	10.983654	
I7	135.3	R8	0.15	2.7459135	8.2377405	
I8	135.2	R8	0.1	1.827904	5.483712	273.48019
Total				274.4203555	823.2610665	

Remark: As shown in Table 4.10, integration of ST in to the existing feeder (substituting 50kVA) at point P8 with ST reduces the line losses from 1.1MW to 823.3kW and a maximum power saving of 273.4kW is obtained only in the main feeder.

Table4. 11 Node voltage profile with ST applied

Bus name	Nominal bus Voltage(PN) (V)	Actual bus voltage(V)	V(PU)
P1	8660	8602	0.99330254
P2	8660	8451	0.97586605
P3	8660	8314	0.96004619
P4	8660	8220	0.94919169
P5	8660	8186	0.94526559
P6	8660	8189	0.94561201
P7	8660	8216	0.94872979

Remark: Application of ST in the existing feeder improves the voltage profiles of nodes

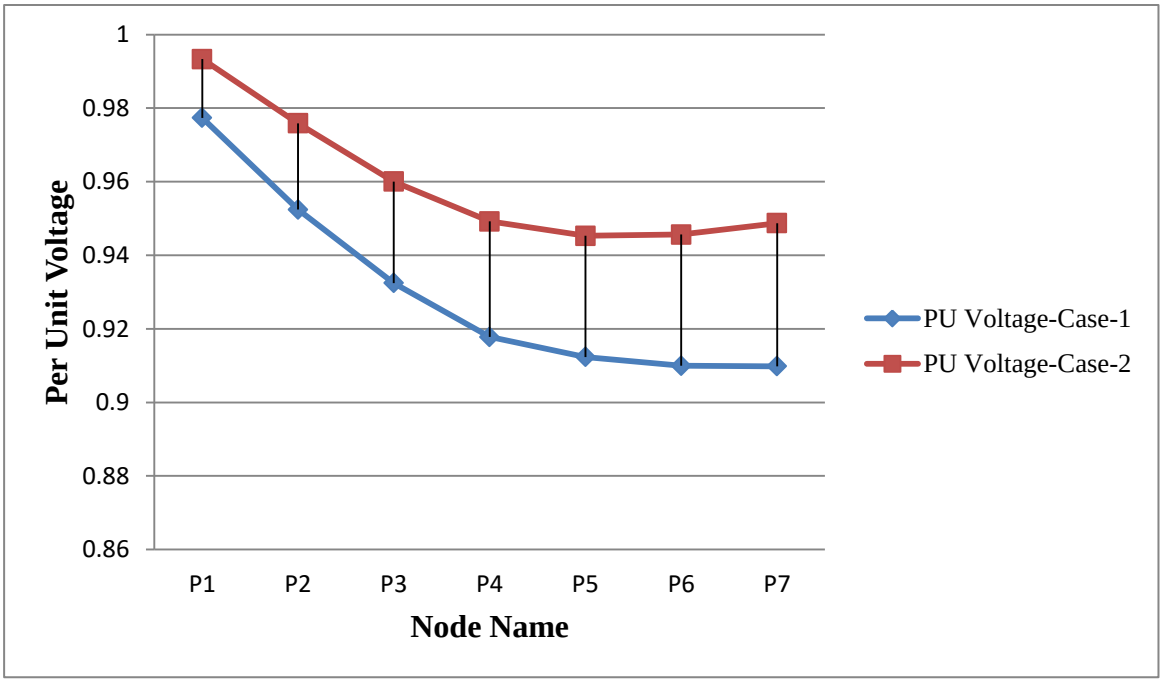


Fig4. 13 Node voltage of Secha feeder without ST and with application of ST

Table4.12 Reactive power flow with ST applied

Q-Flow- Without ST		MVAr -Flow- With ST		
From-To	Value(MVAr)	From-To	Value(MVAr)	MVAr-Support
SS-P1	6.9	SS-P1	3.49	3.41

Remark: Results in Table4.12 show that ST supplies reactive power to upstream of feeder, reducing the total reactive power flow from the source side by 3.41MVAr.

4.8 Simulation result with ST integration in the feeder for non-linear load

As a non-linear load, uncontrolled three phase diode rectifier connected with a maximum load of 24kW is used at ST in combination with linear loads having 24kW and 2kVAr. The propagation of current and voltage harmonics in to nearby loads or upstream feeder is assessed.

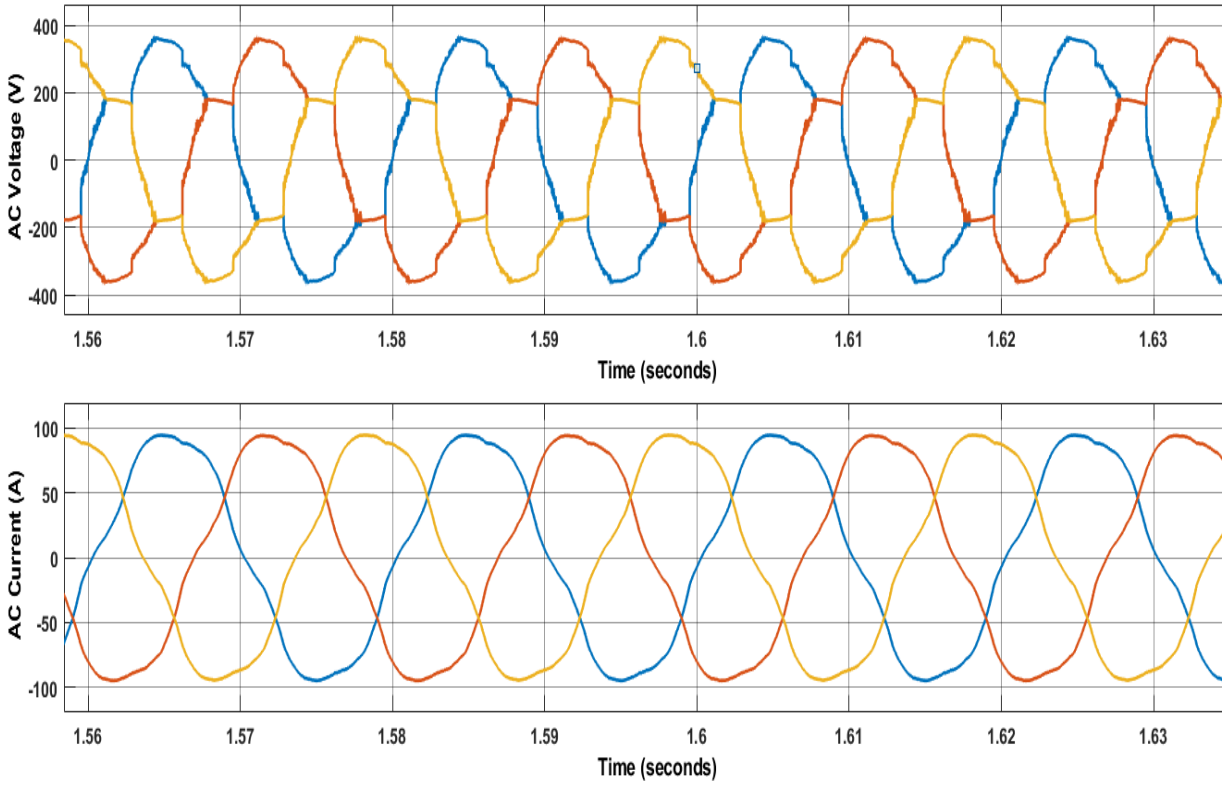


Fig4. 14 V-I wave shape at load terminal when ST is connected to non-linear load

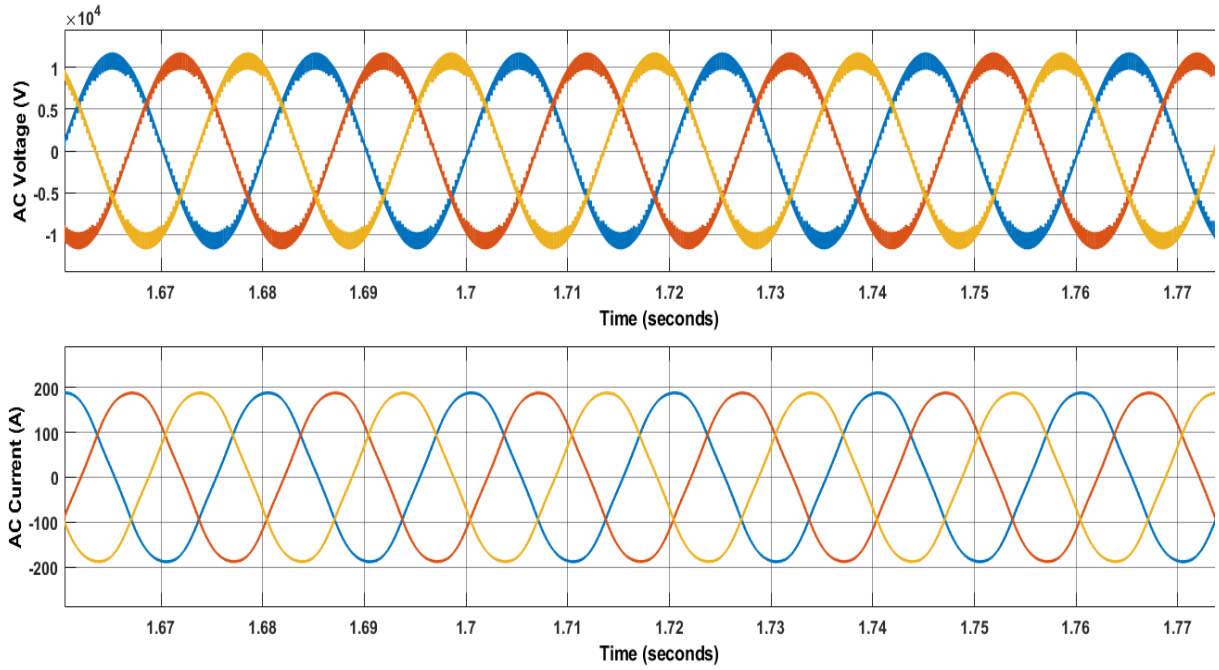


Fig4. 15 V-I wave shape at PCC when ST is connected to non-linear load

As shown in Fig.4.14 and Fig 4.15, use of non-linear loads at ST output terminal produce a current and voltage distortions which would not propagate in to PCC in the upstream.

Summary

Existing Secha main feeder containing 72 distribution transformers has been modelled and simulated for maximum loading. The simulation is carried out for balanced condition and line flows, losses and node voltages have been evaluated. Results of simulation showed that line a loss of 1.1MW can happen only in the main feeder from point P1 to point P8. This loss doesn't include loss in the laterals and service mains. The simulation result also showed that a maximum reactive power of 6.9 MVAr flows from distribution substation to the feeder supplying the requirement of transformers, loads and lines. The voltage profiles at different nodes is observed to be in the range of 0.977 p.u to 0.909 p.u

Integration of smart transformer (ST) in to the existing distribution system has improved the feeder performance in terms of voltage profile improvement, loss reduction and reducing the propagation of harmonics in to upstream. It is shown in the simulation result that reactive demand in the feeder is reduced from 6.9MVAr to 3.49 MVAr, main feeder loss is reduced from 1.1MW to 823.3kW. The voltage profiles at different nodes is improved and in the range of 0.99 p.u to 0.95 p.u. Moreover, capacity release of transformers and distribution lines and greater availability due to of possibility of using renewable energy sources are another benefits of using a multiport three stage ST.

OVERALL CONCLUSIONS AND RECOMMENDATIONS

5.1 Overall conclusions

The Smart transformer (ST) architecture composed by three power processing stages, i.e. MV stage, DC-DC stage and LV stage, with a constant DC link has been designed, modeled and analyzed with diverse controllers and modulation techniques. The designed multiport ST has been used to replace a 50kVA, 15/0.4kV, 50Hz distribution transformer in the Secha feeder and its impacts in improving the feeder performance have been evaluated. From the research carried out in this dissertation, the conclusions to be made can be divided into four parts: front stage converter, middle stage converter, back end converter and ST integration in to existing Secha feeder.

In the design and modeling of front stage converter of ST, a modular multilevel converter (MMC) configuration containing was used. The grid side MV is 15kV RMS (line value) and the desired MVDC voltage is 24.5kV for ensuring bidirectional operation of the converter in the time of grid outage. A half bridge semi-conductor power module is used as a building block to model the front side MMC. Based on the MV DC voltage requirement and the PEBB blocking voltage value (6.5kV), the number of sub-modules per phase leg was designed to be four (four in the upper arm and four in the lower arm). Multicarrier modulation technique such as phase shifted PWM and level shifted PWM were used to generate gate signals. The model was developed in MATLAB/SIMULINK, and its performance with respect to input side voltage harmonics, current harmonics and output DC voltage value has been tested by carrying out several case studies under different controllers such as proportional integrator(PI), fuzzy inference system (FIS) and adaptive –neuro fuzzy inference system (ANFIS) for obtaining reference signal for modulation. Level shifted PWM is used with PI, FIS and ANFIS whereas phase shift PWM with a technique of introducing DC bias is used with PI controller alone. From the simulation results it has been observed that better power system current quality of FS-MMC is obtained for PS-PWM (3.88%) than level shifted PWM (29.4%). Use of FIS and ANFIS with level shift PWM method substantially reduced the current THD values to 4.20% and 4.03% respectively. Also, a maximum output DC voltage of 24650 V is obtained for ANFIS with level shift PWM as compared to values obtained by PI with level shift PWM and PI with phase shift PWM.

In the design and modeling of DC//DC stage, three alternative configurations such as DAB-ISOP, AQAB and SMAB have been proposed with a phase shifted modulation having carrier frequency of 20 kHz. A SiC full bridge (FB) power switches with blocking voltage value of 10kV was used in this stage. In the case of DAB-ISOP configuration, three input side or primary active bridge converters were serially connected to share the input side MVDC of 24.5kV and the other three secondary active bridges were connected in parallel to share the power or current. Activation and deactivation of secondary converter of this configuration enables the power management during partial loading. Also, this configuration proved the availability of power when one of the secondary side converters is faulty. The AQAB configuration uses a multiple winding three primary side converters and one secondary side converter is used. Despite greater current loading of the power switches and reduced availability, this configuration is also a viable alternative for this DC//DC stage of ST. The SMAB configuration uses a multiple winding transformer with three primary and three secondary active bridges are used. Except from the fact that a multi-winding single MFT has been used, this configuration has same operation as that of DAB-ISOP configuration.

In the design and modeling of back-end converter stage, two potential modular converters such as MMC and CHB have been designed and modeled with interleaved phase shifted modulation having carrier frequency of 1 kHz. A half bridge sub module (HBSM) and full bridge sub module (FBSM) were used for MMC and CHB configurations respectively. This stage was designed to have input DC voltage of 700V and output AC phase voltage of 415V (line-to line), 50Hz. The converter was designed to supply 50kVA load and different operation scenarios such as change in the modulation index, change in carrier frequency and change in load demand have been used to assess the performance of the converter. Simulation results showed that for the same modulation index, load type and number of modules, MMC-based BEC has lower voltage and current THD and higher system efficiency than CHB based BEC. If the carrier frequency goes up, the THD of the current goes down, but the THD of the voltage stays the same. With decrease in modulation index (Mi), both voltage and current THD must increase. The sub-module in CHB based modular converter is exposed to higher current stress than that in MMC based modular converter. When nonlinear loads, such as rectifiers, are used, current THD increases. Semiconductor loss analysis showed that switching loss was greater than conduction loss for both selected switches. From the two chosen power semiconductor switches, the SiC MOSFET having part number (PN) SCT3017AL has a good efficiency of 96.63%

At the last, the designed ST has been integrated in to the existing distribution system model in ArbaMinch town and its impacts have been assessed. Existing Secha main feeder containing 72 distribution transformers has been modelled and simulated for maximum loading. The simulation is carried out for balanced peak load condition and line flows, losses and node voltages have been evaluated. The simulation results showed that line a loss of 1.1MW occurs only in the main feeder from point P1 to point P8. It has been also shown from the simulation result that a maximum reactive power of 6.9 MVAr flows from distribution substation to the feeder supplying transformers, loads and lines. The voltage profiles at different nodes are observed to be in the range of 0.909 p.u to 0.977 p.u to for peak load condition.

Integration of the smart transformer (ST) in to the existing distribution system model has considerably improved the feeder performance in terms of voltage profile improvement, loss reduction and reducing the propagation of harmonics in to upstream network. It was shown in the simulation result that reactive demand in the feeder has been reduced from 6.9MVAr to 3.49 MVAr, main feeder loss was reduced from 1.1MW to 823.3kW. The voltage profiles at different nodes were improved to be in the range of 0.95 p.u to 0.99 p.u. In addition to the above benefits, capacity release of transformers and distribution lines and greater availability as a result of the possibility of using renewable energy sources are another benefits of using a multiport three stage ST.

5.2 Recommendations

The following points are recommended from the research work. Trade-off between cost and reliability analysis of front side converter, middle side converter and back end converter should be made based on actual manufacturers' cost of power switches, MFT, control and modulation circuits. Use of SiC power switches can greatly reduce the number of modules per phase per leg for ST based on MMC configuration and future works can consider the latest SiC technology having larger blocking voltage. Also it is recommended that future works should include interfacing of RES in to the MV and LV port of ST for to improve the availability of overall system It can be strongly recommended for Ethiopian Electric Utility (EEU) to see emerging technologies such as smart transformer (ST) and integrate in to the existing distribution system to improve the system performance.

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Appendices

Appendix-A.1

Park and Inverse Park Transformation

Park Transform or the dq0 transform is one of the important tools used in the simulation to handle the input and the output power in the system. It is a space vector transformation which essentially an extension of Clarke transform where the three phase time domain signal (abc) on a stationary frame is converted in to a synchronous frame (dq0) with an angular velocity of ω with respect to abc frame. The d-axis is the direct axis and the q-axis is the quadrature axis. The symmetry of the system is described by 0-axis.

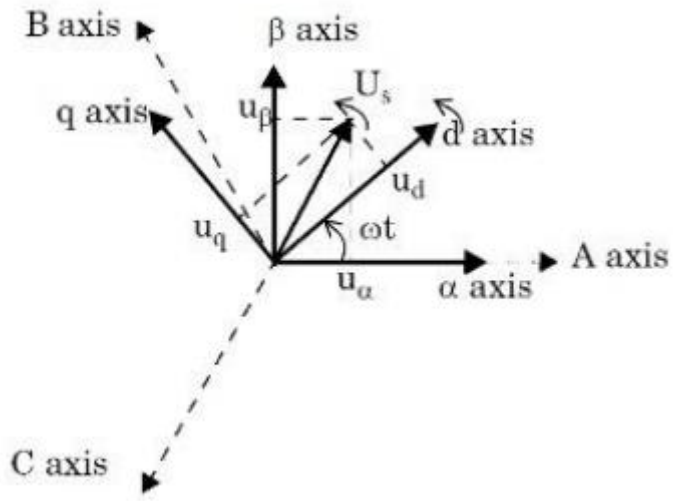


Fig. A. 1 Park transformation

In stationary ABC frame, active and reactive powers of a three-phase balanced system can be represented by [172]

$$P(t) = Re\left[\frac{3}{2} v_a(t) i_a^*(t)\right]$$
$$Q(t) = Im\left[\frac{3}{2} v_a(t) i_a^*(t)\right] \quad \textbf{(1)}$$

Where, Va, ia and ia∗ are the phase voltage, line current, and complex conjugate of the line current, respectively.

By using dq0 frame, the above equation can be put as follows

$$P(t) = \frac{3}{2}[v_{d\_grid}(t)i_{d\_grid}(t) + v_{q\_grid}(t)i_{q\_grid}(t)]$$
$$Q(t) = \frac{3}{2}[-v_{d\_grid}(t)i_{q\_grid}(t) + v_{q\_grid}(t)i_{d\_grid}(t)] \quad \textbf{(2)}$$

In steady-state conditions and considering, Vq(grid) = (0), equation (2) is reduced to :

$$P(t) = \frac{3}{2}[v_{d\_grid}(t)i_{d\_grid}(t)]$$
$$Q(t) = \frac{3}{2}[-v_{d\_grid}(t)i_{q\_grid}(t)] \quad \textbf{(3)}$$

This is called the power invariant form of dq0 transform because the instantaneous power calculated from this transform is equal to the power calculated in the normal stationary ABC frame.

The voltage and current in dq0 frame is obtained by multiplying the ABC vectors with the transform matrix as,

$$\begin{bmatrix} v_{d(t)} \\ v_{q(t)} \\ v_{0(t)} \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} \sin\omega_0 t & \sin\left(\omega_0 t - \frac{2}{3}\pi\right) & \sin\left(\omega_0 t + \frac{2}{3}\pi\right) \\ \cos\omega_0 t & \cos\left(\omega_0 t - \frac{2}{3}\pi\right) & \cos\left(\omega_0 t + \frac{2}{3}\pi\right) \\ \sqrt{\frac{1}{2}} & \sqrt{\frac{1}{2}} & \sqrt{\frac{1}{2}} \end{bmatrix} * \begin{bmatrix} v_{a(t)} \\ v_{b(t)} \\ v_{c(t)} \end{bmatrix} \quad \textbf{(4)}$$

The inverse of this transform to get back the ABC frame is given by

$$\begin{bmatrix} v_{a(t)} \\ v_{b(t)} \\ v_{c(t)} \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} \cos\omega_0 t & -\sin(\omega_0 t) & \frac{\sqrt{2}}{2} \\ \cos\left(\omega_0 t - \frac{2}{3}\pi\right) & -\sin\left(\omega_0 t - \frac{2}{3}\pi\right) & \frac{\sqrt{2}}{2} \\ \cos\left(\omega_0 t + \frac{2}{3}\pi\right) & -\sin\left(\omega_0 t + \frac{2}{3}\pi\right) & \frac{\sqrt{2}}{2} \end{bmatrix} * \begin{bmatrix} v_{d(t)} \\ v_{q(t)} \\ v_{0(t)} \end{bmatrix} \quad \textbf{(5)}$$

Park transformation has advantage that the current and voltage in three phase system is converted into three phase constant (DC) form such as d-axis, q-axis and 0-axis components which are controlled by proportional-integral controllers to assure zero steady-state error. The active power can be controlled by controlling the d-axis and the reactive power can be controlled by controlling the q-axis. The 0-axis component is at zero if the three phase system is symmetrical.

Appendix A.2

Inner Current Controller Design

The inner current control loop is built as shown in Figure 11. The reference converter current obtained from the outer control loop in the form of dq0 scale, is compared with the AC current output of the converter which is the current to be controlled. The three phase controller current is transformed to the dq0 scale using Park transform. In order to derive the control equation of the controller current and establish a relationship between the converter current and the voltage of the sub-module cluster, we consider each sub-module to be a voltage generator and simplifying it even more, the sub-modules on each phase arm are bunched up to represent a single voltage source as series connected voltage sources are added up according to Kirchhoff's law. Each of the arm voltage sources can be regulated to control the charge on the capacitors to impose the required current through the arm inductor. The phase currents on each phase leg need to be equal. The most simplified MMC model given on (Fig.3.5) and displayed below is used to derive the control equation.

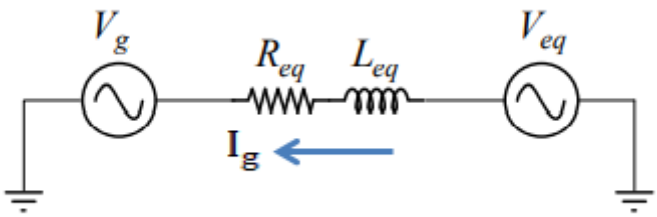


Fig. A. 2 MMC operating in inverter mode

Assuming that the converter is operating in inverter mode and applying Kirchhoff's voltage law yields:

$$V_{inv} = V_g + I_g R_{eq} + L_{eq}\left(\frac{dI_g}{d_t}\right) \qquad (A2.1)$$

Transforming (A2.1) in to dq0 and writing the equation for differential component gives the following equation

$$L_{eq}\left(\frac{dI_{d,g}}{d_t}\right) = V_{d,inv} - V_{d,g} - I_{d,g}R_{eq} + \omega o L_{eq}\, I_{q,g} \qquad (A2.2)$$

$$L_{eq}\left(\frac{dI_{q,g}}{d_t}\right) = V_{q,inv} - V_{q,g} - I_{q,g}R_{eq} - \omega o L_{eq}\, I_{d,g} \quad (A2.3)$$

Where, L_{eq} and R_{eq} represent the equivalent inductance and resistance of the system as expressed in equation (3.4), $V_{d,inv}$ and $V_{q,inv}$ represent the inverter voltage in dq0 frame, $V_{d,g}$ and $V_{q,g}$ represent the grid voltage in dq0 frame and ωo is angular frequency

The output of PI controller in Fig.A.3 below can be set as follows to improve system stability:

$$\vartheta_{d,} = V_{d,inv} - V_{d,g} + \omega o L_{eq}\, I_{q,g} \quad (A2.4)$$

$$\vartheta_{q,} = V_{d,inv} - V_{d,g} - \omega o L_{eq}\, I_{q,g} \quad (A2.5)$$

By substituting variables in (A2.4) and (A2.5) in to equations (A2.2) and (A2.3) and expressing in Laplace domain yields the following control equation:

$$\frac{I_{d,g}}{\vartheta_{d,}} = \frac{1}{L_{eq}S + R_{eq}} \quad (A2.6)$$

$$\frac{I_{q,g}}{\vartheta_{q,}} = \frac{1}{L_{eq}S + R_{eq}} \quad (A2.7)$$

The current controller block diagrams for control equations (A2.6) and (A2.7) are displayed below in Fig. A2.2

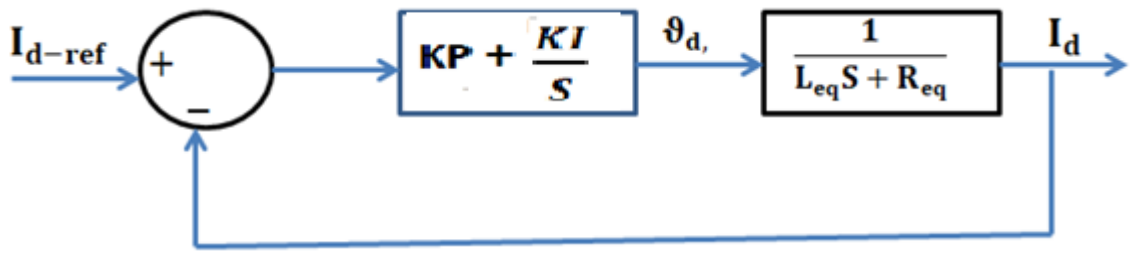


Fig. A. 3Direct Current Controller block diagram

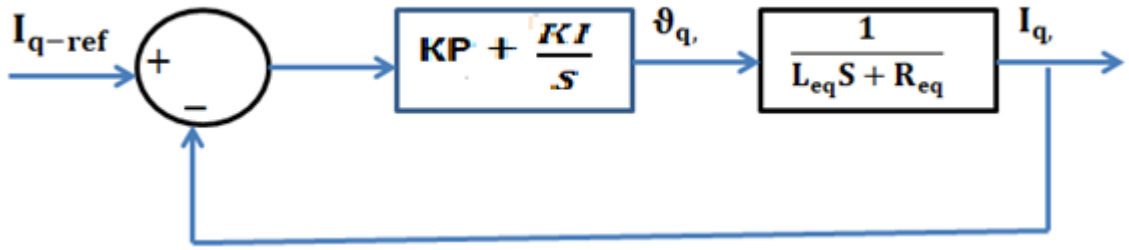


Fig. A. 4 Quadrature Current Controller block diagram

Considering the system to be of first order, the transfer function of the feedback system is given as

$$G_2(s) = \frac{C_2(s)H_2(s)}{1 + C_2(s)H_2(s)} \qquad \text{A2.8}$$

Where $C_2(S) = KP+KI/S$ and $H_2(S) = 1/(L\_eq\ S + R\_eq\ )$

If ωs is the band width of converter, the transfer equation can also be given by

$$G_2(s) = \frac{I_{c\,dq}}{I^{*}_{c\,dq}} = \frac{\omega_s}{s + \omega_s} = \frac{\frac{\omega_s}{s}}{1 + \frac{\omega_s}{s}} \qquad \text{A2.9}$$

Comparison of (A2.9) and (A2.8) shows that:

$$\omega_s = s\, C_2(s)H_2(s) \qquad \text{(A2.10)}$$

$$C_2(s) = \frac{\omega_s}{s}.H_2^{-}(s)$$

Substituting the expression of $H_2(S)$ in (A2.10) yields the following expression,

$$C_2(s) = \omega_s \mathbf{L_{eq}} + \frac{\omega_s \mathbf{R_{eq}}}{s} \quad \text{(A2.11)}$$

Using expression in (A2.11) for $C_2(S)$ and making use of general $C_2(S)$ gives the expression for of proportional control and integral constants as follows:

$$C_2(s) = \omega_s \mathbf{L_{eq}} + \frac{\omega_s \mathbf{R_{eq}}}{s} = \text{Kp} + \text{Ki/s} \quad \text{(A2.12)}$$

$$\text{Kp} = \omega_s \mathbf{L_{eq}}$$
$$\text{Ki} = \omega_s \mathbf{R_{eq}}$$

Where, $\boldsymbol{L_{eq} = L_g + \frac{L_{arm}}{2}}$ **and,** $\boldsymbol{R_{eq} = R_g + \frac{R_{arm}}{2}}$

The bandwidth of the controllers determines the system response speed. Thus, selection of the bandwidth is inter-related. Traditionally, the inner (current) loop response is selected ten times faster than the outer(voltage) loop and it is customary to have the bandwidth for the inner loop to be smaller than the one-fifth of the switching frequency which in this project work is set to 1000Hz. [6]. Therefore, the bandwidth of the current controllers is set at 1256 rad/s (200 Hz). For the given values of Leq and Req found in specification table.3.1 in page 70. , the values of Kp and Ki are 10 and 100 respectively.

Appendix A.3

DC voltage Controller (Outer loop control)

The DC voltage around the capacitor of the VSI must be kept constant. DC voltage control is important for controlling the power exchange. The DC voltage control designed at keeping the DC voltage at a defined value using the converter current as a control variable. Assuming the converter to be losses less the active power that enters the converter is the same to the active power that leaves the converter. To ensure the regulation of the dc capacitor voltage, a PI controller can be used. If we neglect the losses in the inverter and the output filter, the relation between the absorbed power by the filter and the voltage around the capacitor can be given by:

$$P_{dc} = \frac{d}{dt}\left(\frac{1}{2} C_{dc} V_{dc}^2\right) \quad \text{(A3.1)}$$

By using the Laplace transform, we can achieve:

$$P_{dc}(S) = \frac{1}{2} S C_{dc} V_{dc}^2(S) \quad \text{(A3.2)}$$

The voltage of the capacitor is then given by:

$$V_{dc}^2(S) = \frac{2P_{dc(S)}}{C_{dc}S} \quad \text{(A3.3)}$$

From the equation (A3.3) above and considering the use of PI controller, the dc voltage control loop can be represented by in Figure below.

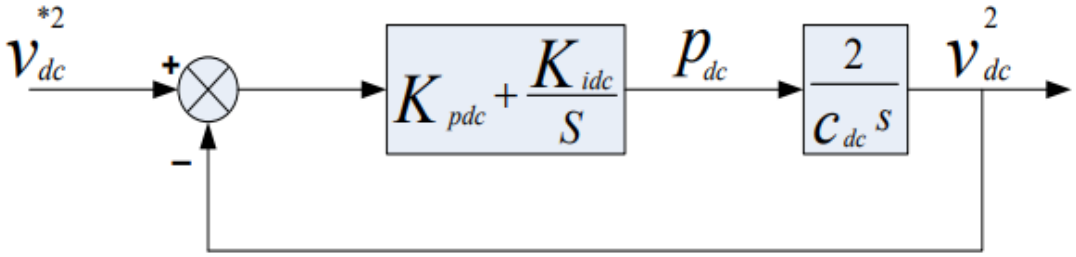


Fig.A.5: DC voltage control loop

The closed loop transfer function of the system with the controller can be given by

$$G_{CL} = \frac{\left(1+\frac{K_{pdc}}{K_{idc}}S\right)}{s^2+2\frac{K_{pdc}}{C_{dc}}S+2\frac{K_{idc}}{C_{dc}}}$$

From where we can find the different parameters of the controller as:

$$K_{idc} = \frac{1}{2}C_{dc}\omega_c^{\,2} \quad , \quad K_{pdc} = \xi\sqrt{2C_{dc}K_{idc}}$$

where the damping coefficient ξ is set to 0.707 for good dynamic response.. For C_{dc} value of 15mF so as to allow enough energy storage and natural frequency of 200Hz, the values of K_{pdc} and K_{idc} becomes 15 and 11850 respectively

Appendix B.1

AAC conductor parameters

CONDUCTOR DATA SHEET

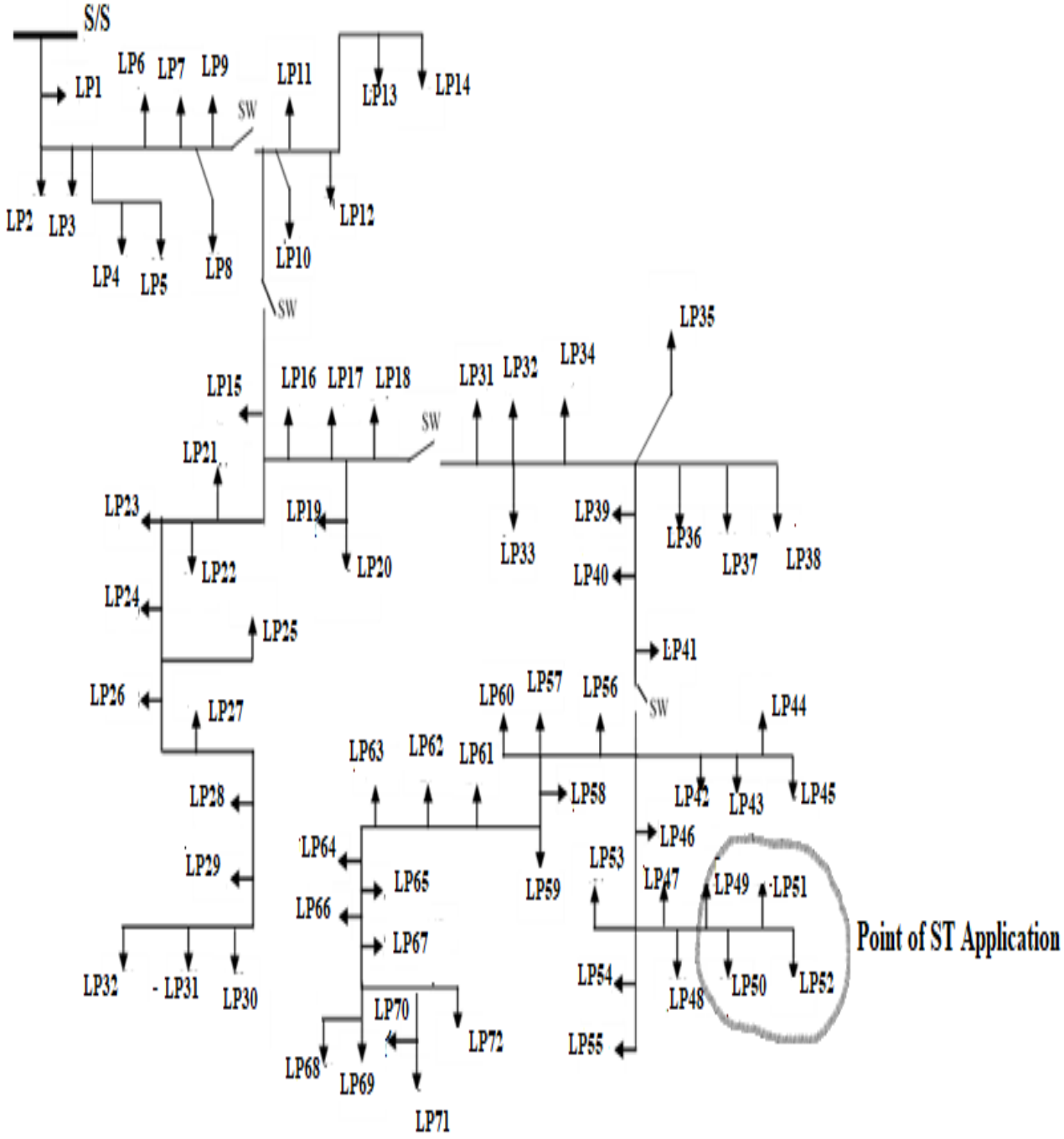
ALL ALUMINUM STRANDED CONDUCTORS (AAC)

British Sizes

Code Name	Nominal Aluminum area	Equivalent Copper Area	Stranding and wire diameter	Overall Diameter	Total Area	Weight	Rated Stength	Maximum DC resistance at 20 °C
	mm²	mm²	mm	mm	mm²	kg/km	kN	Ω /km
Midge	22	14.2	7/2.06	6.2	23.3	64	3.99	1.227
Aphis	25	16.1	3/3.35	7.2	26.4	73	4.12	1.081
Gnat	25	16.1	7/2.21	6.6	26.8	73	4.59	1.0662
Weevil	30	19.4	3/3.66	7.9	31.6	86	4.86	0.9082
Mosquito	35	22.6	7/2.59	7.8	36.9	101	6.03	0.7763
Ladybird	40	25.8	7/2.79	8.4	42.8	117	6.99	0.6687
Ant	50	32.3	7/3.10	9.3	52.8	145	8.28	0.5419
Fly	60	38.7	7/3.40	10.2	63.6	174	9.90	0.4505
Bluebottle	70	45.2	7/3.66	11.0	73.7	202	11.33	0.3887
Earwig	75	48.4	7/3.78	11.4	78.5	215	11.94	0.3645
Grasshopper	80	51.6	7/3.91	11.7	84.1	230	12.78	0.3405
Clegg	90	58.1	7/4.17	12.5	95.6	262	14.53	0.2994
Wasp	100	64.5	7/4.39	13.2	106.0	290	16.00	0.2700
Beetle	100	64.5	19/2.67	13.4	106.4	293	17.38	0.2703
Bee	125	80.6	7/4.90	14.7	132.0	361	19.94	0.2167
Cricket	150	96.8	7/5.36	16.1	157.9	432	23.80	0.1812
Hornet	150	96.8	19/3.25	16.3	157.6	434	25.70	0.1825
Caterpillar	175	113.0	19/3.53	17.7	186.0	512	28.62	0.1547
Chafer	200	129.0	19/3.78	18.9	213.2	587	32.40	0.1349
Spider	225	145.0	19/3.99	20.0	237.6	652	36.11	0.1211

Appendix B. 2

Detail layout diagram of Secha feeder



Appendix B. 3

Secha feeder detail data

Bus			Conductor				Load at receiving end		
No	**From**	**To**	**Type**	**R(ohm)**	**X(ohm)**	**L(m)**	Installed (kVA)	Actual (kW)	Actual (kVAr)
1	SS	1	AAC95	0.1959	0.206	635	630	191.67	143.75
2	2	3	AAC50	0.199	0.1194	344	200	159.84	119.88
3	3	4	AAC50	0.0648	0.0389	112	50	26.28	19.71
4	4	5	AAC50	0.0544	0.0326	94	200	88.77	66.58
5	3	6	AAC50	0.1435	0.0861	248	315	131.24	98.43
6	6	7	AAC50	0.3072	0.1843	531	315	195.53	146.65
7	7	8	AAC50	0.1475	0.0885	255	315	111.78	83.84
8	7	9	AAC50	0.4038	0.2422	698	315	103.33	77.5
9	9	10	AAC50	0.3783	0.227	654	315	134.13	100.6
10	9	11	AAC50	0.4715	0.2828	815	315	116.49	87.37
11	11	12	AAC50	0.2702	0.1621	467	50	25.73	19.3
12	12	13	AAC50	0.1759	0.1055	304	315	129.23	96.92
13	13	14	AAC50	0.2569	0.1541	444	315	130.22	97.67
14	9	15	AAC50	0.2204	0.1322	381	200	91.22	68.42
15	15	16	AAC50	0.3014	0.1808	521	50	16.33	12.25
16	16	17	AAC50	0.1701	0.102	294	100	38.91	29.18
17	17	18	AAC50	0.0729	0.0437	126	200	95.96	71.97
18	17	31	AAC50	0.2204	0.1322	381	315	108.31	81.23
19	31	32	AAC50	0.4327	0.2596	748	100	56.31	42.23
20	15	19	AAC50	0.0798	0.0479	138	100	39.55	29.66
21	19	20	AAC50	0.1134	0.068	196	50	17.43	13.07
22	20	21	AAC50	0.2146	0.1287	371	315	148.78	111.59
23	21	22	AAC50	0.2626	0.1575	454	200	83.85	62.89
24	22	23	AAC50	0.2985	0.1791	516	200	107.02	80.27
25	23	24	AAC50	0.1845	0.1107	319	315	176.71	132.53
26	24	25	AAC50	0.3645	0.2186	630	315	151.16	113.37
27	25	26	AAC50	0.0573	0.0344	99	315	125.06	93.8
28	26	27	AAC50	0.1585	0.0951	274	50	23.14	17.36
29	27	28	AAC50	0.1313	0.0788	227	500	288.14	216.11
30	29	30	AAC50	0.1932	0.1159	334	315	149.26	111.95
31	18	33	AAC50	0.2036	0.1222	352	200	85.62	64.22
32	33	34	AAC50	0.2453	0.1471	424	200	87.15	65.36
33	34	35	AAC50	0.247	0.1482	427	200	86.17	64.63
34	34	36	AAC50	0.2846	0.1707	492	50	17.32	12.99
35	35	37	AAC50	0.269	0.1614	465	100	73.44	55.08
36	37	38	AAC50	0.0498	0.0298	86	800	214.54	160.91

37	38	39	AAC50	0.1915	0.1149	331	315	137.03	102.77
38	39	40	AAC50	0.0353	0.0212	61	50	17.5	13.13
39	37	41	AAC50	0.096	0.0576	166	315	146.03	109.52
40	41	42	AAC50	0.1313	0.0788	227	630	191.53	143.65
41	42	43	AAC50	0.2378	0.1426	411	315	105.11	78.83
42	40	44	AAC50	0.2071	0.1242	358	315	114.24	85.68
43	44	45	AAC50	0.0729	0.0437	126	200	63.4	47.55
44	45	46	AAC50	0.1267	0.076	219	200	88.69	66.52
45	46	47	AAC50	0.2146	0.1287	371	200	75.64	56.73
46	40	48	AAC50	0.2615	0.1569	452	50	16.1	12.08
47	48	49	AAC50	0.1539	0.0923	266	50	10.37	7.78
48	49	50	AAC50	0.0486	0.0291	84	315	99.71	74.78
49	50	51	AAC50	0.2945	0.1766	509	200	117.51	88.13
50	49	52	AAC50	0.1036	0.0621	179	630	231.11	173.33
51	52	53	AAC50	0.0949	0.0569	164	315	149.5	112.13
52	53	54	AAC50	0.0509	0.0305	88	25	11.87	8.9
53	54	55	AAC50	0.5652	0.339	977	200	63.98	47.99
54	55	56	AAC50	0.0069	0.0042	12	50	21.61	16.21
55	56	57	AAC50	0.0989	0.0593	171	200	108.88	81.66
56	40	58	AAC50	0.1689	0.1013	292	400	240.32	180.24
57	58	59	AAC50	0.0897	0.0538	155	1250	434.53	325.9
58	60	61	AAC50	0.1707	0.1024	295	630	255.91	191.93
59	61	62	AAC50	0.0451	0.0271	78	315	151.45	113.59
60	62	63	AAC50	0.1186	0.0711	205	1250	492.64	369.48
61	63	64	AAC50	0.3228	0.1936	558	200	93.46	70.1
62	64	65	AAC50	0.0029	0.0017	5	200	82.01	61.51
63	66	67	AAC50	0.2655	0.1593	459	315	104.49	78.37
64	67	68	AAC50	0.0723	0.0434	125	200	102.61	76.96
65	54	55	AAC50	0.2401	0.144	415	50	20.56	15.42
66	40	58	AAC50	0.0787	0.0472	136	50	23.31	17.48
67	53	54	AAC50	3.0215	1.8125	5223	200	82.54	61.91
68	55	56	AAC50	1.6632	0.9977	2875	25	17.63	13.22
69	68	69	AAC50	0.0469	0.0281	81	50	21.86	16.4
70	69	70	AAC50	0.8284	0.4969	1432	50	11.89	8.92
71	70	71	AAC50	3.7522	2.2508	6486	630	181.85	136.39
72	71	72	AAC50	0.575	0.3449	994	100	44.59	33.44
Total						**38842**	**19,330**	**7957.08**	**5967.9**

Appendix B. 4

IGBT Data sheet

FF225R65T3E3
XHP™3 module

XHP™3 module with Trench/Fieldstop IGBT3 and emitter controlled 3 diode

Features

- Electrical features
  - V_{CES} = 6500 V
  - $I_{C\,nom}$ = 225 A / I_{CRM} = 450 A
  - High dynamic robustness
  - Low $V_{CE,sat}$
  - Trench IGBT 3
- Mechanical features
  - Package with CTI > 600
  - Package with enhanced insulation of 10.4 kV AC 60 s
  - AlSiC base plate for increased thermal cycling capability
  - Extended storage temperature down to T_{stg} = -55 °C
  - High creepage and clearance distances
  - Housing material compliant with the classification R23 (HL3) of the EN45545-2 "Fire protection of railway vehicles"

Potential applications

- Traction drives
- Medium-voltage converters

Product validation

- Qualified for industrial applications according to the relevant tests of IEC 60747, 60749 and 60068

Description

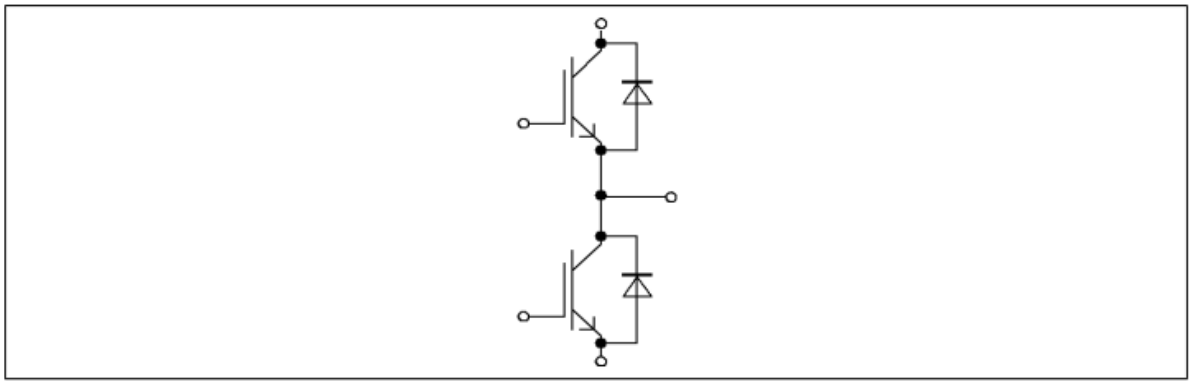


Table 3 **Maximum rated values**

Parameter	Symbol	Note or test condition		Values	Unit
Collector-emitter voltage	V_{CES}		T_{vj} = -50 °C	5900	V
			T_{vj} = 125 °C	6500	
Continuous DC collector current	I_{CDC}	$T_{vj\,max}$ = 125 °C	T_C = 80 °C	225	A
Repetitive peak collector current	I_{CRM}	t_p limited by $T_{vj\,op}$		450	A
Gate-emitter peak voltage	V_{GES}			±20	V